SY8502A

High Efficiency, 1.2A Continuous, 1.8A Peak, 85V Input Synchronous Step Down Regulator

General Description

The SY8502A develops a high efficiency synchronous step-down DC/DC converter capable of delivering 1.2A continuous, 1.8A peak current. The SY8502A operates over a wide input voltage range from 7V to 85V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY8502A always operates under continuous conduction mode. The device adopts the instant PWM architecture to achieve fast transient responses for high step down applications.

Ordering Information

SY8502 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8502AFCC	SO8E	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 500mΩ/240mΩ
- 7-85V Input Voltage Range
- 1.2A Continuous, 1.8A Peak Output Current Capability
- Adjustable Switching Frequency
- Instant PWM Architecture to Achieve Fast Transient Responses.
- Programmable Switching Frequency Range: 200~500 kHz.
- 2ms Internal Soft-start Limits the Inrush Current
- Precise ±2% 1.2V Reference
- RoHS Compliant and Halogen Free
- Compact Package SO8E

Applications

- Non-isolated Telecommunication Buck Regulator
- Secondary High Voltage Post Regulator
- Automotive Systems

Typical Applications

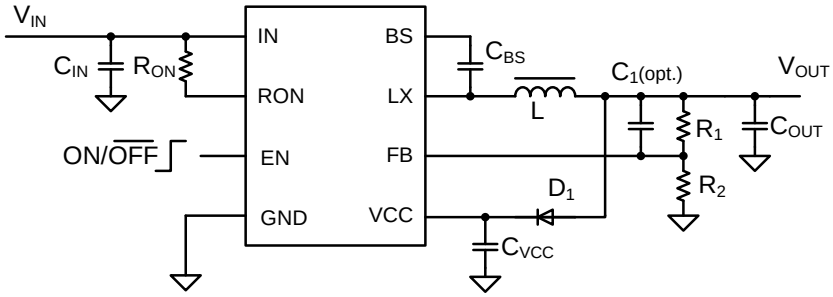


Figure 1. Schematic Diagram

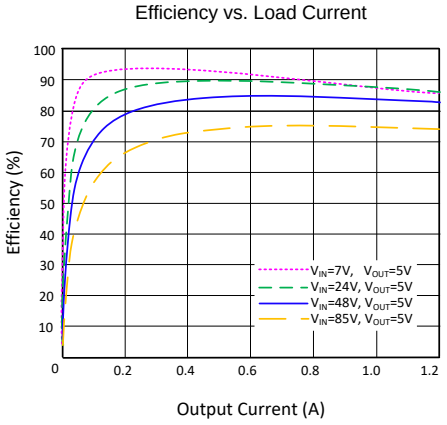
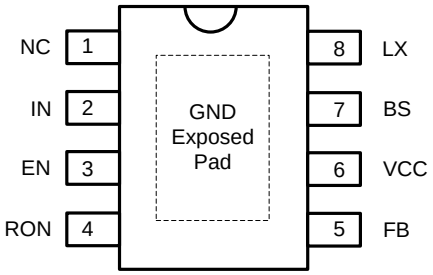


Figure 2. Efficiency

Pinout (top view)



(SO8E)

Top Mark: BWK***xyz*** for SY8502AFCC **(**Device code: BWK, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
NC	1	Not connected.
IN	2	Input pin. Decouple this pin to the GND with a low ESR ceramic capacitor.
EN	3	Enable control. The device has an accurate 1.2V rising threshold. This pin can also be used for programming the V_{IN} turn on voltage with the resistor divider.
RON	4	Connect a resistor from this pin to the IN to set the top switch ON time. The switching frequency can be calculated using the following equation: $f_s(kHz) = \frac{11 \times V_{OUT}(V) + 500}{R_{ON}(M\Omega)}$
FB	5	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=1.2\times(1+R1/R2)$
VCC	6	Supply input of the internal LDO.
BS	7	Boot-strap pin. Supply high side gate driver. Decouple this pin to the LX pin with a 0.1μF ceramic capacitor.
LX	8	Inductor pin. Connect this pin to the switching node of the inductor.
GND	Exposed Pad	Ground pin.

Block Diagram

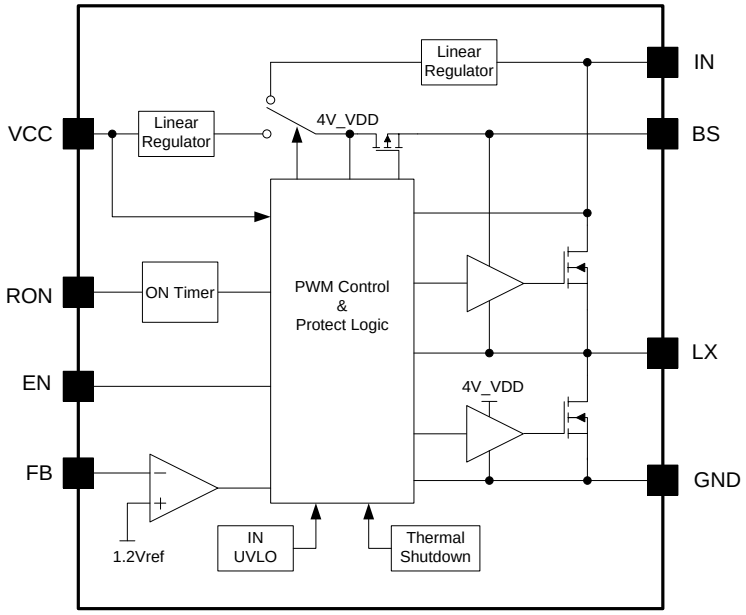


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 90V
EN, LX, RON Voltage ---------- -0.3V to VIN + 0.3V
BS Voltage ---------- -0.3V to LX + 6V
FB Voltage ---------- -0.3V to 6V
VCC ---------- -0.3V to 30V
Power Dissipation, P_D @ T_A = 25°C, SO8E ---------- 3.3W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 30°C/W
θ_{JC} ---------- 10°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX voltage in 10ns duration ---------- IN+3V to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 7V to 85V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN}=48V, V_{OUT}=5V, L=33μH, C_{OUT}=10uF, T_A=25°C, I_{OUT}=1.2A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		7		85	V
Input UVLO Rising Threshold	V_{UVLO}		5.8	6.3	6.8	V
Input UVLO Hysteresis	V_{HYS}			0.25		V
Shutdown Current	I_{SHDN}	EN=0		8	11	μA
Feedback Reference Voltage	V_{REF}		1.176	1.2	1.224	V
FB Input Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			500		mΩ
Bottom FET RON	$R_{DS(ON)2}$			240		mΩ
Top FET Peak Current Limit	$I_{LIM,Top}$			3.2		A
Bottom FET Valley Current Limit	$I_{LIM,Bottom}$		1.6			A
Negative Current Limit			-380	-540	-700	mA
EN Rising Threshold	V_{ENH}		1.11	1.21	1.31	V
EN Falling Threshold	V_{ENL}		1.08	1.18	1.28	V
Switching Frequency	f_{OSC}	V_{IN}=48V, R_{ON}=1.6MΩ		340		kHz
Min ON Time				80		ns
Min OFF Time				200		ns
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

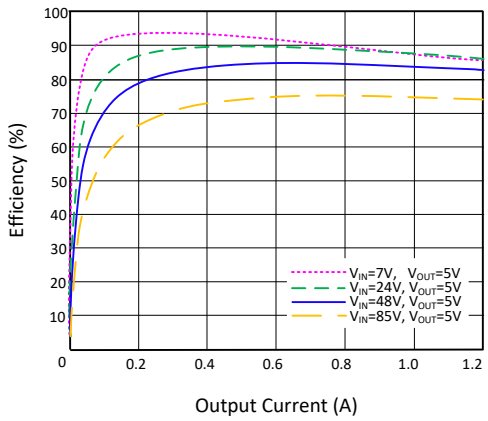
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective 4-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of SO8E package is the case position for θ_{JC} measurement.

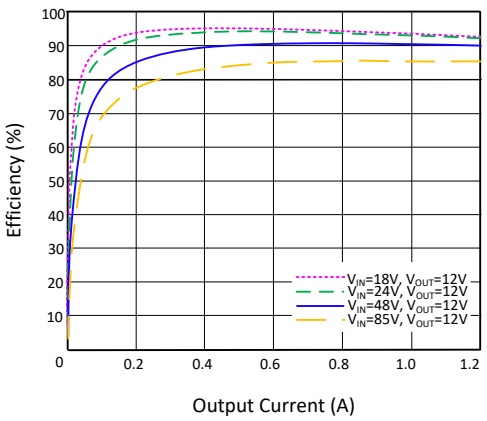
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

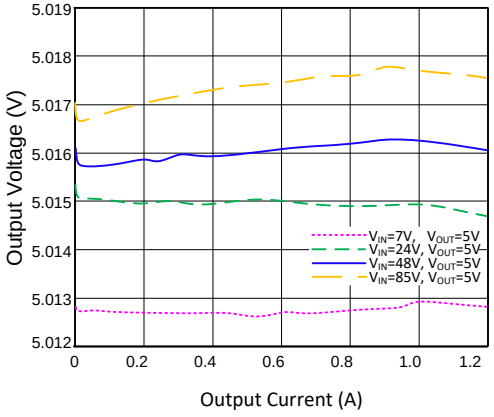
Efficiency vs. Load Current



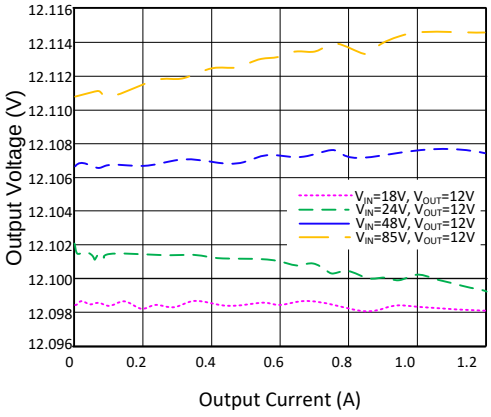
Efficiency vs. Load Current



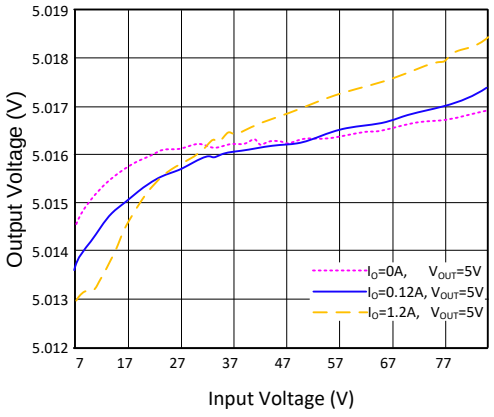
Load Regulation



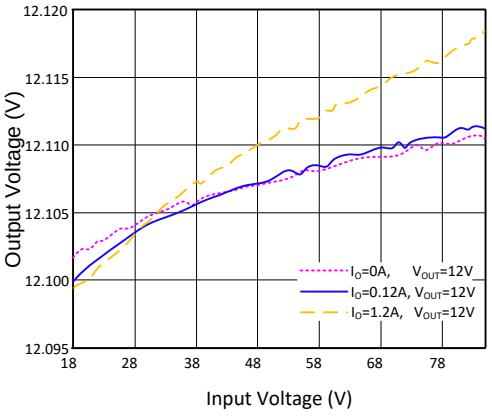
Load Regulation



Line Regulation

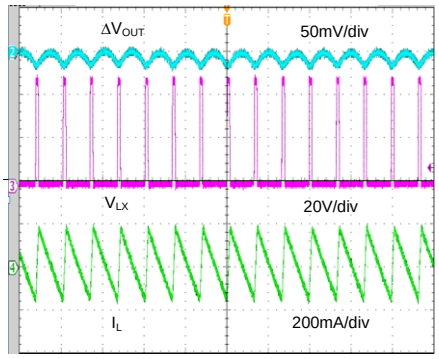


Line Regulation



Output Ripple

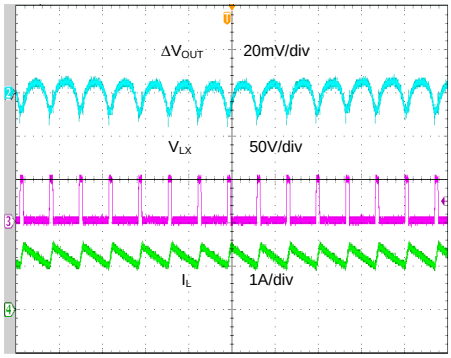
（48V_{IN},5V_{OUT},Io=0A）



Time (4μs/div)

Output Ripple

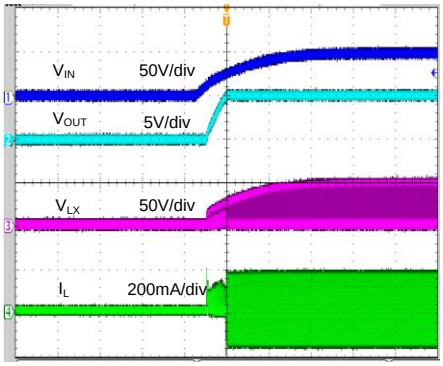
(V_{IN}=48V, V_{OUT}=5V, I_O=1.2A)



Time (4μs/div)

Start from V_{IN}

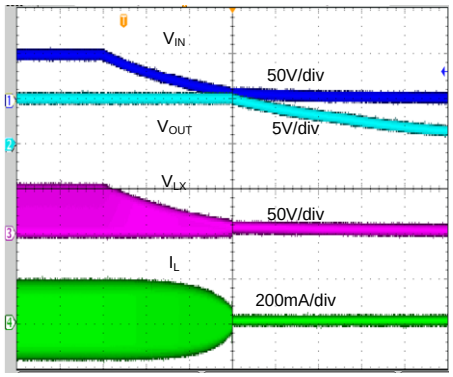
(48V_{IN},5V_{OUT},Io=0A)



Time (4ms/div)

Shutdown from V_{IN}

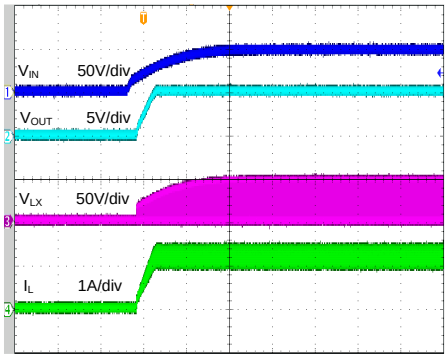
(48V_{IN},5V_{OUT},Io=0A)



Time (200ms/div)

Startup from V_{IN}

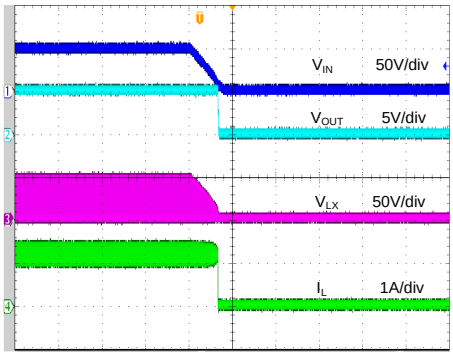
(V_{IN}=48V, V_{OUT}=5V, I_O=1.2A)



Time (4ms/div)

Shutdown from V_{IN}

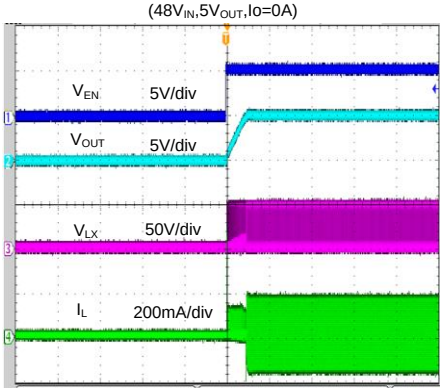
(V_{IN}=48V, V_{OUT}=5V, I_O=1.2A)



Time (4ms/div)

Startup from Enable

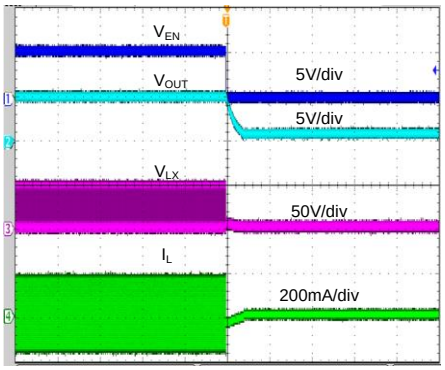
($48V_{IN}$,$5V_{OUT}$,Io=0A)



Time (4ms/div)

Shutdown from Enable

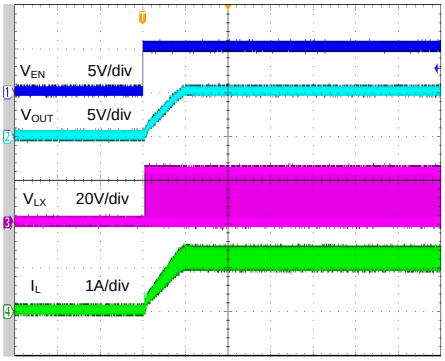
（$48V_{IN}$,$5V_{OUT}$,Io=0A）



Time (4ms/div)

Startup from Enable

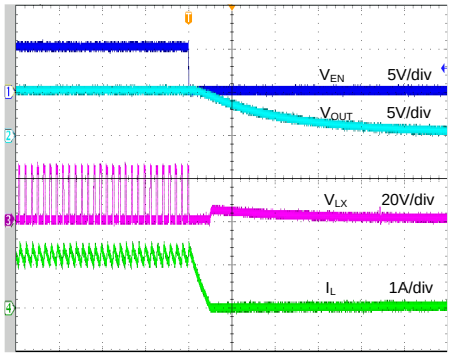
(V_{IN}=48V, V_{OUT}=5V, I_O=1.2A)



Time (2ms/div)

Shutdown from Enable

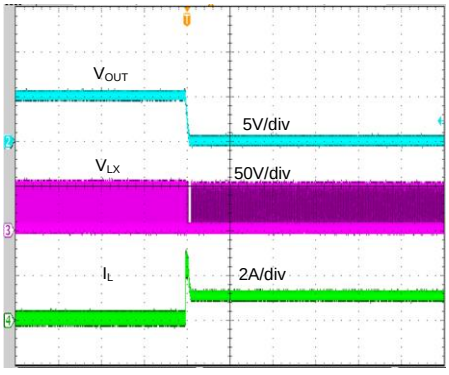
(V_{IN}=48V, V_{OUT}=5V, I_O=1.2A)



Time (20μs/div)

Short Circuit Protection

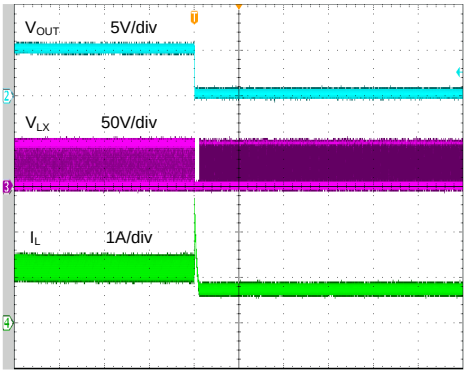
($48V_{IN}$,$5V_{OUT}$,Io=0A~Short)



Time (800μs/div)

Short Circuit Protection

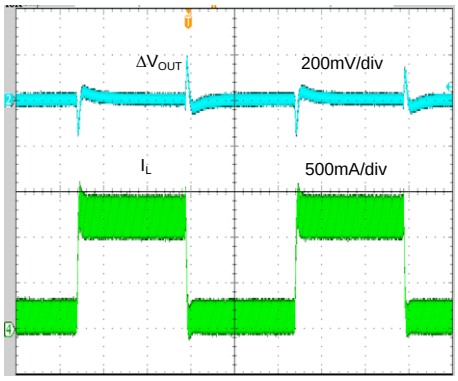
(V_{IN}=48V, V_{OUT}=5V, I_O=1.2A~ Short)



Time (800μs/div)

Load Transient Response

($48V_{IN}$,$5V_{OUT}$,Io=0.12A~1.2A)



Time (200μs/div)

Operation Description

The SY8502A operates over a wide input voltage range from 7V to 85V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. This regulator adopts the instant PWM architecture with an internal ripple control scheme using an on-time inversely proportional to V_{IN} to achieve fast transient responses for high voltage step down applications. This architecture requires no loop compensation. In addition, it operates at pseudo-constant frequency under continuous conduction mode to minimize the size of inductor and capacitor.

Applications Information

Because of the high integration in the SY8502A, the application circuit based on this regulator is rather simple. Only the on-timer resistor R_{ON}, the feedback resistors (R_1 and R_2), the input capacitor C_{IN}, the output capacitor C_{OUT} and the output inductor L need to be selected for the targeted applications specifications.

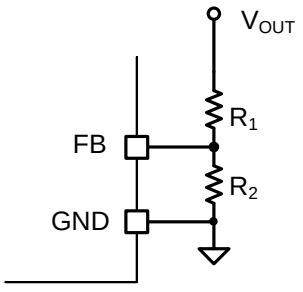
This regulator is well suited for 48V telecom and the new 42V automotive power bus ranges.

Output Voltage Program

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2.

$$V_{OUT} = (1+\frac{R_1}{R_2})\times V_{FB}$$

The typical V_{FB} is 1.2V.



Output Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L_1 = \frac{V_{OUT}\times(1-V_{OUT}/V_{IN\_MAX})}{f_S\times I_{OUT\_MAX}\times 40\%}$$

Where f_S is the switching frequency and I_{OUT_MAX} is the maximum load current.

The SY8502A is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected greater than the peak inductor current under full load conditions.

$$I_{SAT\_MIN} > I_{OUT\_MAX} + \frac{V_{OUT}\times(1-V_{OUT}/V_{IN\_MAX})}{2f_S\times L_1}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with smaller DCR to achieve a good overall efficiency.

Input Capacitor C_{IN}

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT\_MAX}\times\sqrt{D(1-D)}$$

The capacitance of input capacitor is calculated as:

$$C_{IN} = \frac{I_{OUT}\times V_{OUT}\times(V_{IN}-V_{OUT})}{\Delta V_{IN}\times f_S\times h\times V_{IN}^2}$$

ΔV_{IN} is desired input voltage ripple

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and the GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and the IN/GND pins. In this case, a 1μF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. It is recommended to use an X5R or better grade ceramic capacitor greater than 10μF capacitance.

On Time

The on-time for the SY8502A is determined by the R_{ON} resistor, and is inversely proportional to the input voltage, resulting in a nearly constant frequency as V_{IN} is varied over its range.

Frequency vs. Ron Resistor:

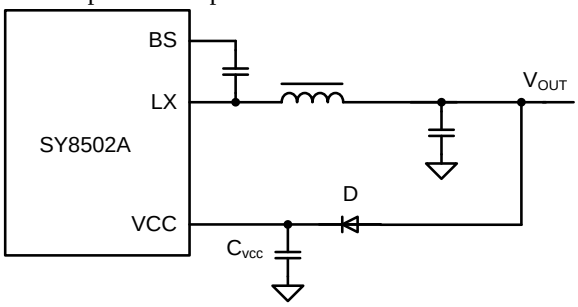
$$f_s(kHz) = \frac{11 \times V_O(V) + 500}{R_{on}(M\Omega)}$$

Notice: final switch frequency is not only affected by component tolerant but also minimum off and on time limit.

Internal LDO Regulator

The SY8502A consists of two internal LDOs for 4V_VDD from the IN pin and the VCC pin. Upon power up, the LDO regulator from the IN pin sources current to the capacitor on the internal 4V_VDD. When the voltage on the 4V_VDD reaches the under-voltage lockout threshold voltage, the Buck switch is enabled. After soft-start done and the VCC pin voltage is larger than 4.2V, the VCC side LDO is enabled and the IN side LDO is disabled. A 0.1μF ceramic capacitor is recommended for C_{VCC} at most applications.

In applications，the input pin (IN) can be connected directly to the line voltages up to 85 V, where power dissipation in the VCC regulator is a concern, an auxiliary voltage can be connected to the VCC pin via a diode. Setting the auxiliary voltage to 4.5 -28V will shut off the internal regulator from IN, reducing internal power dissipation.



Soft-start

The SY8502A has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during the IC start-up. The typical soft-start time is 2ms.

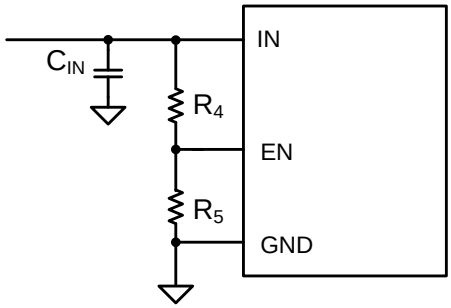
Enable Operation

Pulling the EN pin low will shut down the device. During shut mode, the SY8502A shutdown current drops to lower than 10μA. Driving the EN pin high will turn on the IC again.

Input UVLO can be programmed by EN rising threshold. Minimum V_{UVLO} value needs larger than 6.5V

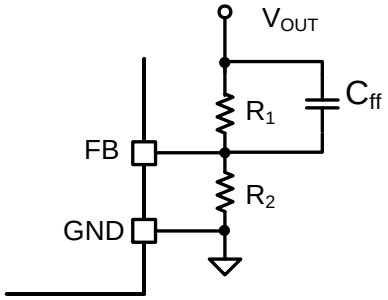
$$V_{UVLO}(V) = (1 + \frac{R_4}{R_5}) \times Vth$$

Vth is the EN rising threshold voltage, typical is 1.2V



Load Transient Considerations

The SY8502A adopts the instant PWM architecture to achieve good stability and fast transient responses. Adding a C_{ff} ceramic capacitor in parallel with R_1 is recommended.



External Boot-strap Capacitor

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.

Over Current Protection

The SY8502A provides cycle-by-cycle over current limit on both high side MOSFET and low side MOSFET. Under over current condition, if the output voltage drops below 33% of set-point, the device will fold back valley current limit to 0.5× typical value.

Layout Design

The layout design of the SY8502A is very important for proper operation. Following are the tips for good PCB layout.

1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to the pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) C_{VCC} should be placed close to the VCC pin and the GND pin.

4) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.

5) The feedback components R_{UP} and R_{DOWN} and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

6) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull-down 1MΩ resistor between the EN and the GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

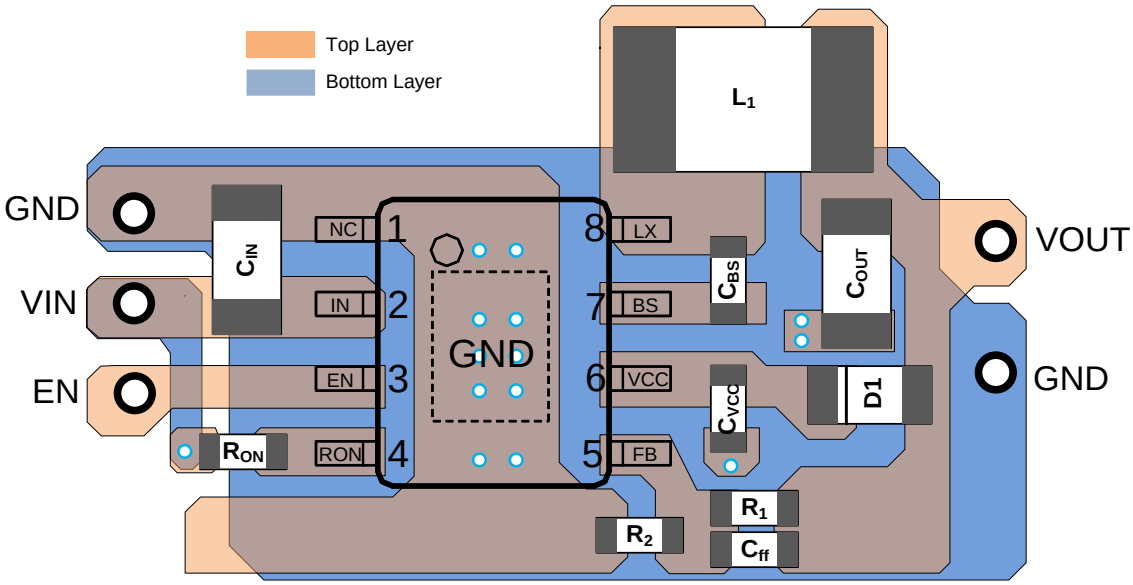
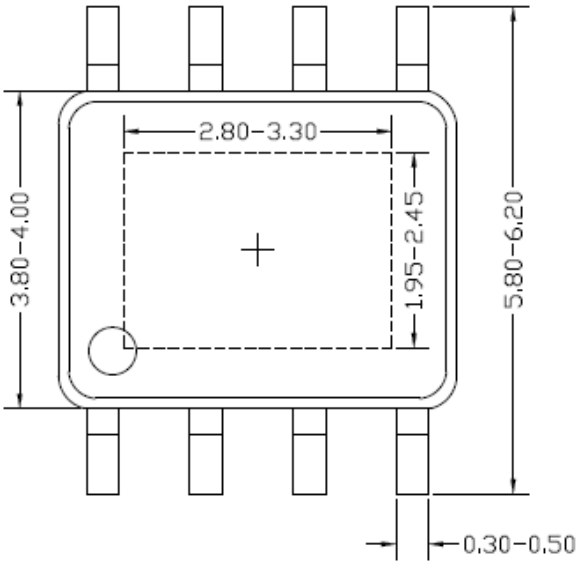
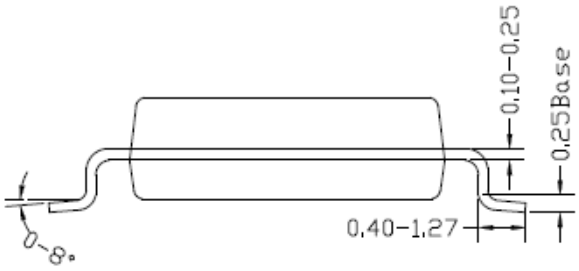


Figure4. PCB Layout Suggestion

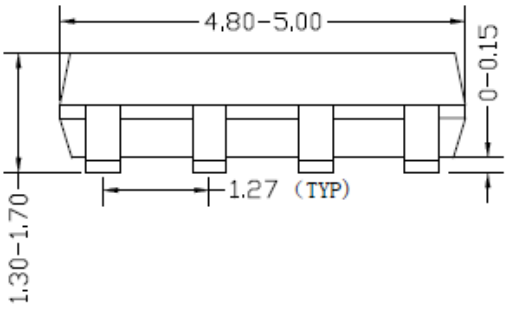
SO8E Package Outline & PCB layout



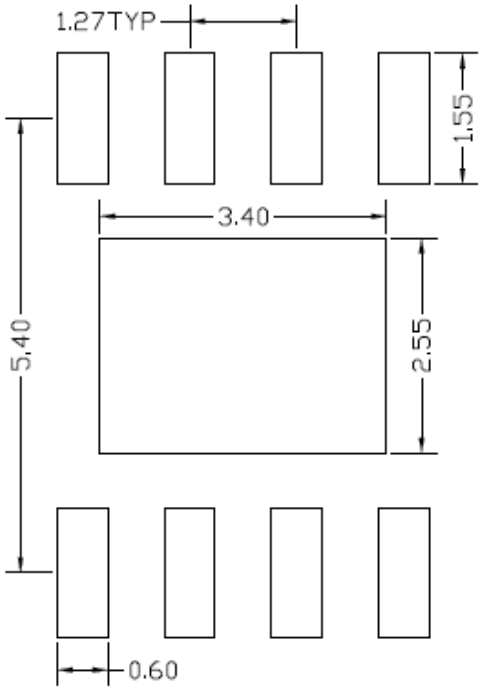
Top view



Side view



Front view



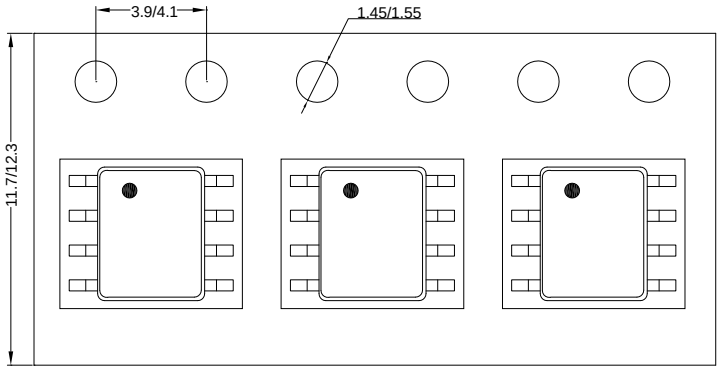
Recommended PCB Layout
(Reference Only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

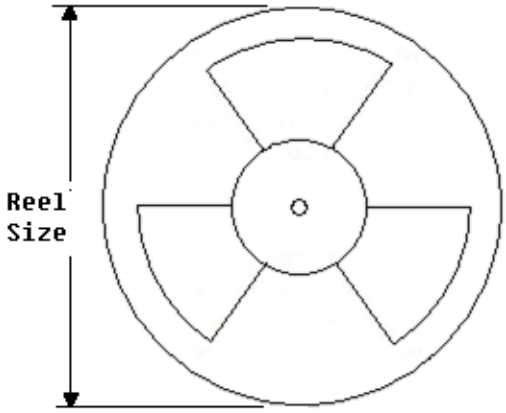
1. Taping orientation

SO8E



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8E	12	8	13"	400	400	2500

3. Others: NA

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