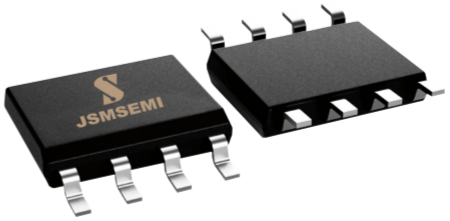
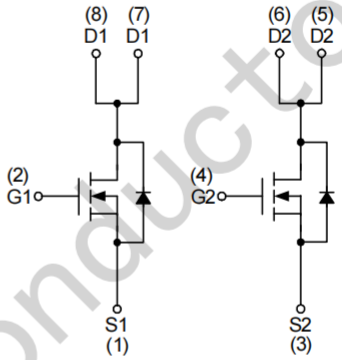
Features

- 40V/12A,
  $R_{DS(ON)}$ = 7 mΩ (max.) @ V_{GS} = 10V
  $R_{DS(ON)}$ = 1 0 mΩ (max.) @ V_{GS} = 4.5V
- 100% UIS + R_g Tested
- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)



Applications

- Power Management in Note book.
- Battery Powered System.
- DC/DC Converter.
- Load Switch.



N-Channel MOSFET

Absolute Maximum Ratings(T_A = 25°C unless otherwise noted)

Symbol	Parameter		Rating	Unit
Common Ratings				
V_{DSS}	Drain-Source Voltage		40	V
V_{GSS}	Gate-Source Voltage		±20	V
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-55 to 150	°C
I_S	Diode Continuous Forward Current	T_A=25°C	2	A
I_D	Continuous Drain Current	T_A=25°C	12	A
		T_A=70°C	8	
I_{DM} [a]	Pulse Drain Current Tested	T_A=25°C	40	A
P_D	Maximum Power Dissipation	T_A=25°C	3	W
		T_A=70°C	2.5	
$R_{\theta JL}$	Thermal Resistance-Junction to Lead	Steady State	50	°C/W
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	t ≤ 10s	62.5	°C/W
		Steady State [b]	110	
I_{AS} [c]	Avalanche Current, Single pulse	L=0.5mH	10	A
E_{AS} [c]	Avalanche Energy, Single pulse	L=0.5mH	25	mJ

Note a：Pulse width limited by max. junction temperature.
Note b：Surface Mounted on 1in^2 pad area, t =999sec.
Note c：UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature T_j=25°C).

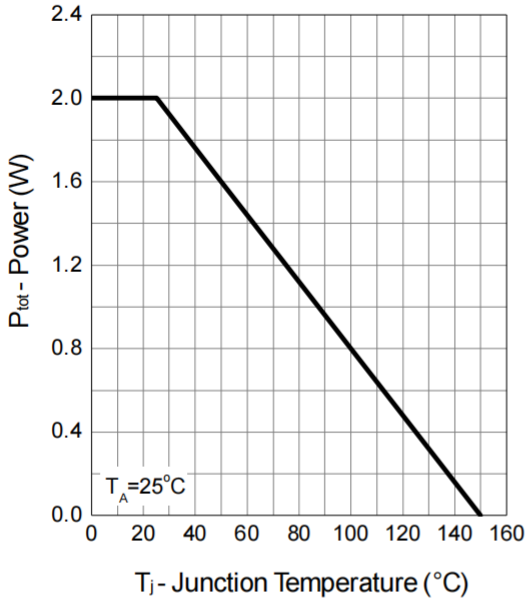
Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250μA	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=32V, V_{GS}=0V	-	-	1	μA
		T_J=85°C	-	-	30	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250μA	1.5	2	2.5	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
$R_{DS(ON)}$ [c]	Drain-Source On-state Resistance	V_{GS}=10V, I_{DS}=6A	-	7	9	mΩ
		V_{GS}=4.5V, I_{DS}=5A	-	10	13	
Diode Characteristics						
V_{SD} [c]	Diode Forward Voltage	I_{SD}=1A, V_{GS}=0V	-	0.75	1.1	V
t_{rr}	Reverse Recovery Time	I_{DS}=6A, dI_{SD}/dt=100A/μs	-	13	-	ns
Q_{rr}	Reverse Recovery Charge		-	8.7	-	nC
Dynamic Characteristics [d]						
R_G	Gate Resistance	V_{GS}=0V,V_{DS}=0V,F=1MHz	-	2.5	-	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=20V, Frequency=1.0MHz	-	815	-	pF
C_{oss}	Output Capacitance		-	95	-	
C_{rss}	Reverse Transfer Capacitance		-	60	-	
$t_{d(ON)}$	Turn-on Delay Time	V_{DD}=20V, R_L=20Ω, I_{DS}=1A, V_{GEN}=10V, R_G=6Ω	-	7.8	-	ns
t_r	Turn-on Rise Time		-	6.9	-	
$t_{d(OFF)}$	Turn-off Delay Time		-	22.4	-	
t_f	Turn-off Fall Time		-	4.8	-	
Gate Charge Characteristics [d]						
Q_g	Total Gate Charge	V_{DS}=20V, V_{GS}=10V, I_{DS}=6A	-	15.7	22	nC
Q_g	Total Gate Charge	V_{DS}=20V, V_{GS}=4.5V, I_{DS}=6A	-	7.5	10.5	
Q_{gth}	Threshold Gate Charge		-	1.85	-	
Q_{gs}	Gate-Source Charge		-	3.24	-	
Q_{gd}	Gate-Drain Charge		-	2.75	-	

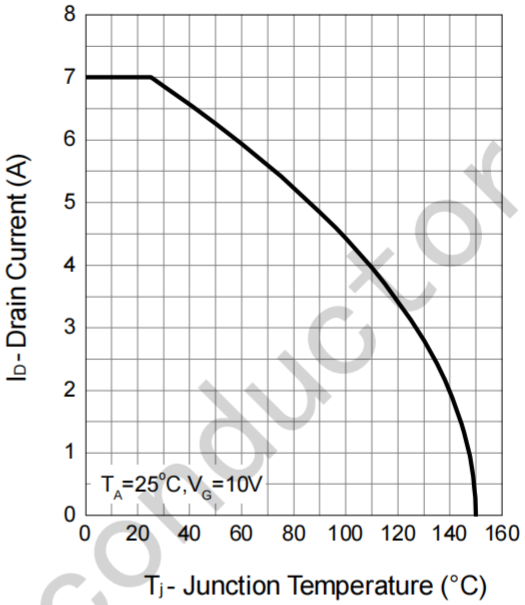
Note c：Pulse test ; pulse width≤300μs, duty cycle≤2%.
Note d：Guaranteed by design, not subject to production testing.

Typical Operating Characteristics

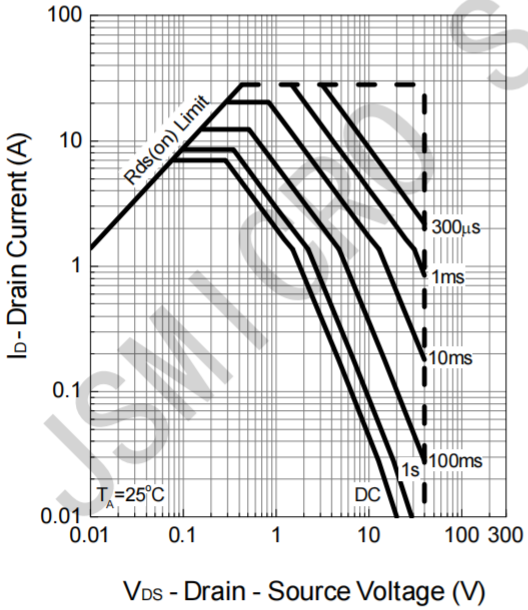
Power Dissipation



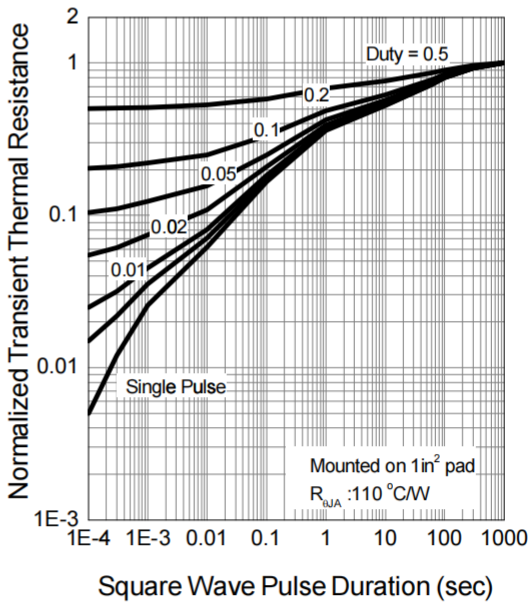
Drain Current



Safe Operation Area

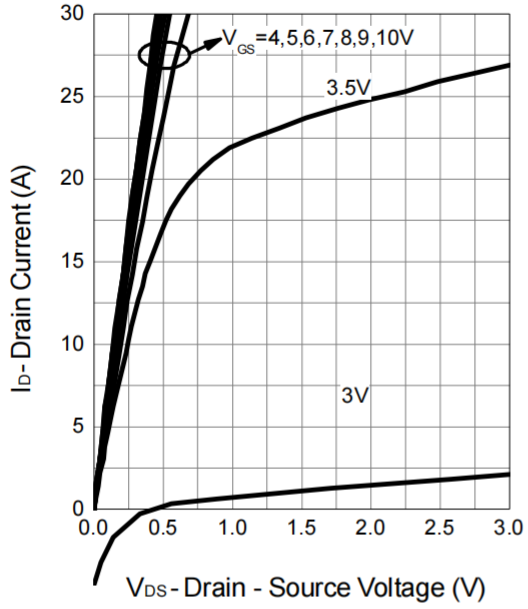


Thermal Transient Impedance

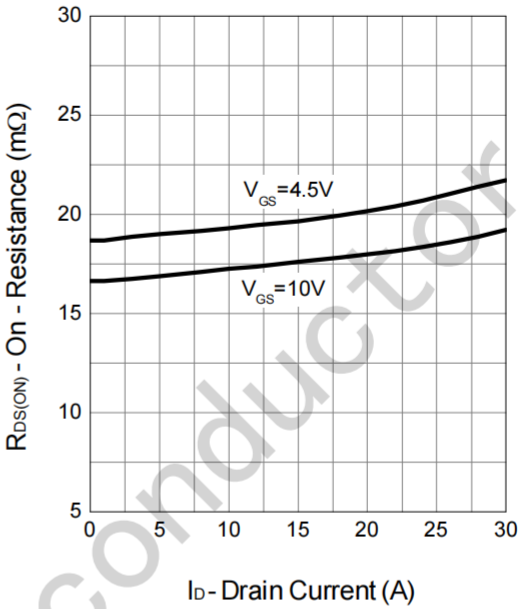


Typical Operating Characteristics(Cont.)

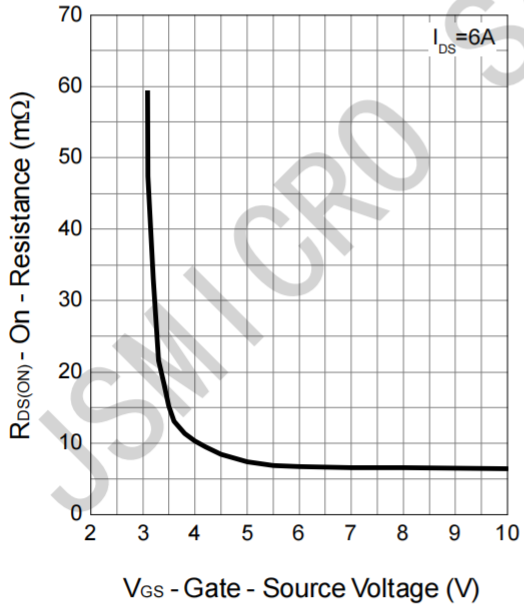
Output Characteristics



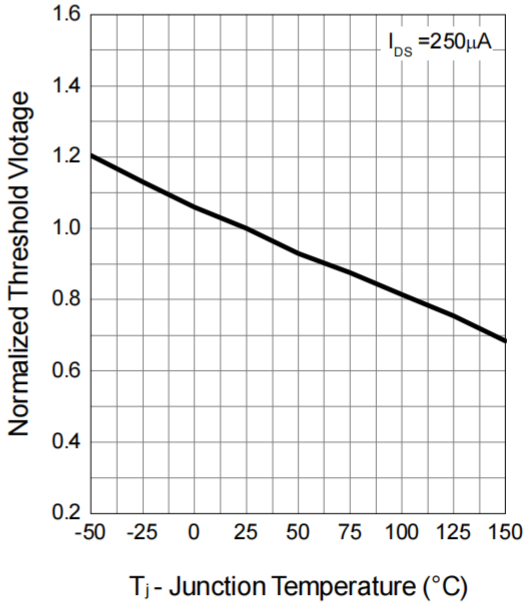
Drain-Source On Resistance



Gate-Source On Resistance

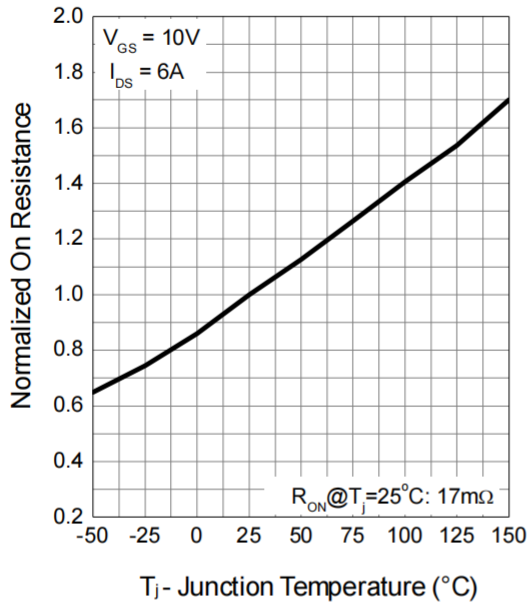


Gate Threshold Voltage

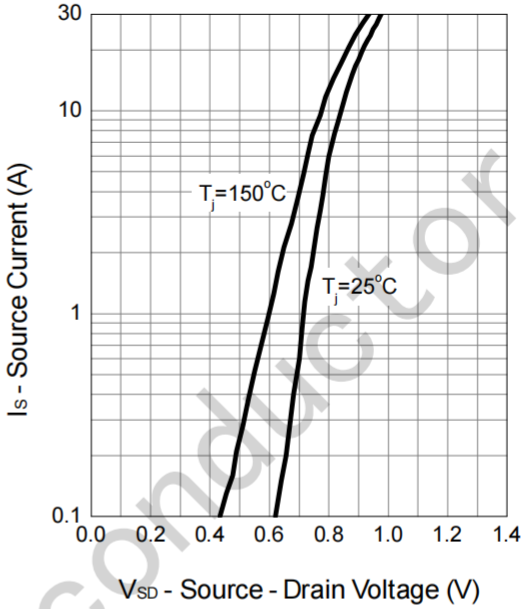


Typical Operating Characteristics(Cont.)

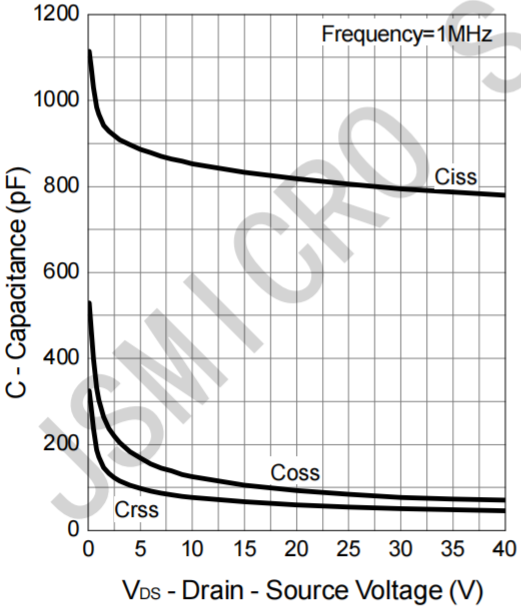
Drain-Source On Resistance



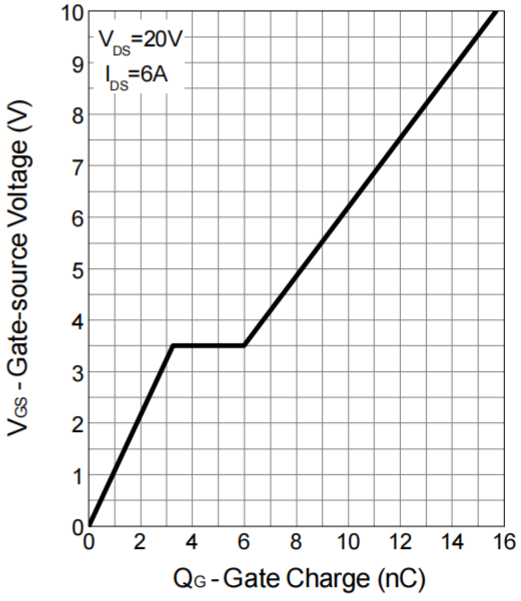
Source-Drain Diode Forward



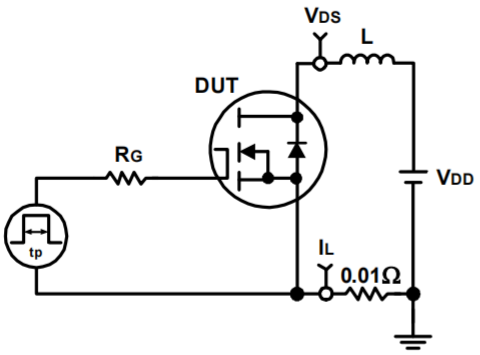
Capacitance

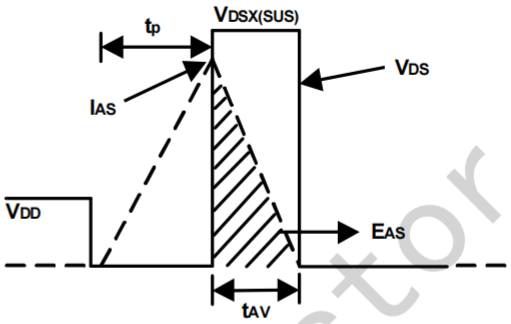


Gate Charge

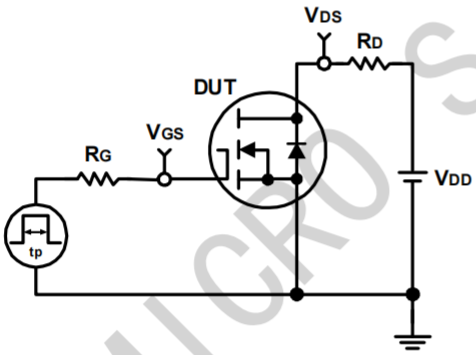


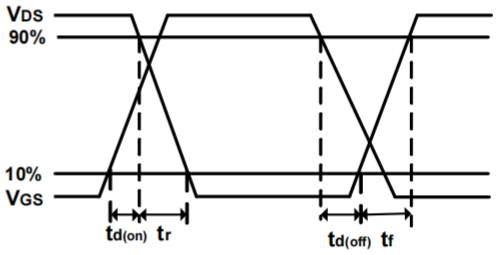
Avalanche Test Circuit and Waveforms





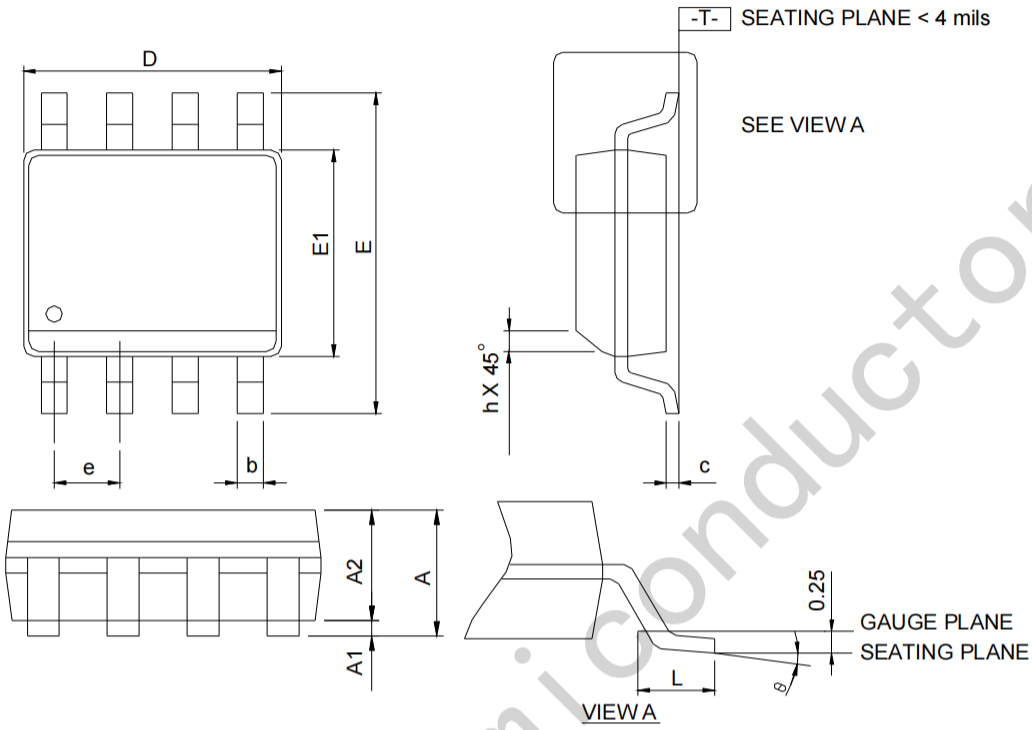
Switching Time Test Circuit and Waveforms





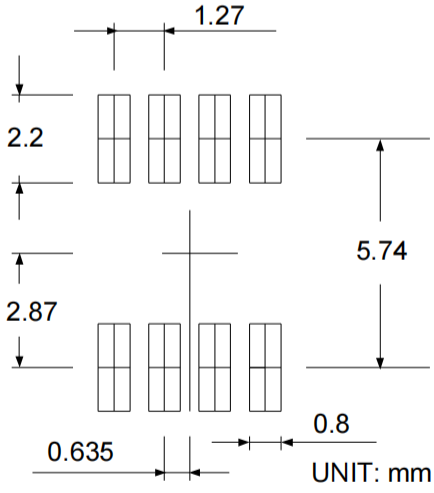
Package Information

SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

RECOMMENDED LAND PATTERN



Note: 1. Follow JEDEC MS-012 AA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.