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SEMICONDUCTOR



ESD



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## ULN2803Ax-MS

Product specification

General Description

The ULN2803Ax-MS is high-voltage high-current Darlington transistor arrays each containing eight open collector common emitter pairs. Each pair is rated at 500mA. Suppression diodes are included for inductive load driving, the inputs and outputs are pinned in opposition to simplify board layout.


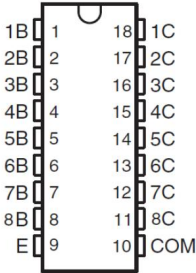
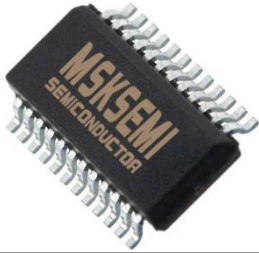
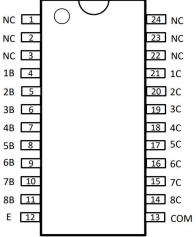
These devices are capable of driving a wide range of loads including solenoids, relays, DC motors, LED displays, filament lamps, thermal print-heads and high-power buffers.

The ULN2803Ax-MS is available in both a small outline 18-pin package (SOP18) and 24-pin package (SSOP24/QSOP24).

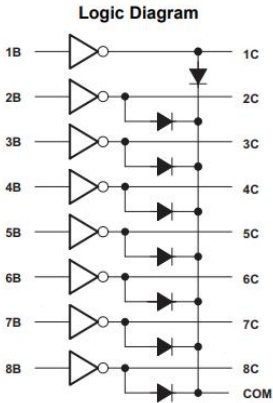
Features

- 500-mA-Rated Collector Current(single output)
  - High-Voltage Outputs:50V
  - Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
  - Relay-Driver Applications

Encapsulation form and pin definition function

PACKAGE OUTLINE	Pin Assignments	Marking
<div></div> <div>SOP-18</div>		<div>ULN2803</div>
<div></div> <div>SSOP-24/QSOP24</div>		<div>ULN2803</div> <div>****</div>

Connection Diagram



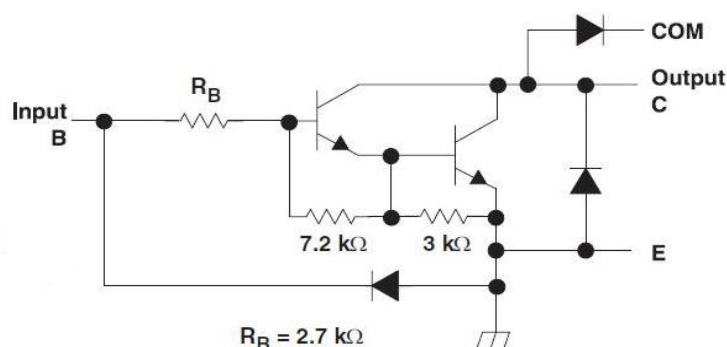
## Pin Descriptions

SOP18 Pin	SSOP24/QSOP24 Pin	Pin Name	Function
---	1	NC	---
---	2	NC	---
---	3	NC	---
1	4	1B	Input pair1
2	5	2B	Input pair2
3	6	3B	Input pair3
4	7	4B	Input pair4
5	8	5B	Input pair5
6	9	6B	Input pair6
7	10	7B	Input pair7
8	11	8B	Input pair8
9	12	E	Common Emitter (ground)
10	13	COM	Common Clamp Diodes
11	14	8C	Output pair8
12	15	7C	Output pair7
13	16	6C	Output pair6
14	17	5C	Output pair5
15	18	4C	Output pair4
16	19	3C	Output pair3
17	20	2C	Output pair2
18	21	1C	Output pair1
---	22	NC	---
---	23	NC	---
---	24	NC	---

## Order Information

Designator	Package	Packing type
ULN2803AG-MS	SOP-18	1500
ULN2803AT-MS	SSOP-24/QSOP24	4000

## Functional Block Diagram



Note: All resistor values shown are nominal.

The collector-emitter diode is a parasitic structure and should not be used to conduct current. If the collector(s) go below ground an external Schottky diode should be added to clamp negative undershoots.

### Absolute Maximum Ratings <sup>(1)</sup>

At 25°C free-air temperature (unless otherwise noted)

Symbol	Parameter		Min	Max	Unit
V <sub>CC</sub>	Collector to emitter voltage			50	V
V <sub>R</sub>	Clamp diode reverse voltage(2)			50	V
V <sub>I</sub>	Input voltage(2)			30	V
I <sub>CP</sub>	Peak collector current	See typical characteristics		500	mA
I <sub>OK</sub>	Output clamp current			500	mA
I <sub>TE</sub>	Total emitter-terminal current			-2.5	A
T <sub>A</sub>	Operating free-air temperature range	ULN2803	-30	+105	°C
θ <sub>JA</sub>	Thermal Resistance Junction-to-Ambient(3)			63	°C/W
θ <sub>JC</sub>	Thermal Resistance Junction-to-Case(4)			12	
T <sub>J</sub>	Operating virtual junction temperature			150	°C
T <sub>STG</sub>	Storage temperature range		-40	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
- (3) Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- (4) Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JC}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JC}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.

## Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
VCC	Collector to Emitter voltage	-	50	V
TA	Operating Ambient Temperature	-30	+105	°C

**Electrical Characteristics(TA=+25°C, unless otherwise specified)**

Parameter		Test Figure	Test Conditions		MIN	TYP	MAX	Unit
$V_{I(on)}$	On-state input voltage	Figure 6	$V_{CE} = 2\text{ V}$	$I_C = 200\text{ mA}$	--	--	2.4	V
				$I_C = 250\text{ mA}$	--	--	2.7	
				$I_C = 300\text{ mA}$	--	--	3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 5	$I_I = 250\text{ }\mu\text{A}$ ,	$I_C = 100\text{ mA}$	--	0.9	1.1	V
			$I_I = 350\text{ }\mu\text{A}$ ,	$I_C = 200\text{ mA}$	--	1	1.3	
			$I_I = 500\text{ }\mu\text{A}$ ,	$I_C = 350\text{ mA}$	--	1.2	1.6	
$I_{CEX}$	Collector cutoff current	Figure 1	$V_{CE} = 50\text{ V}$ ,	$I_I = 0$	--	--	50	$\mu\text{A}$
		Figure 2	$V_{CE} = 50\text{ V}$ , $T_A = +105^\circ\text{C}$	$I_I = 0$	--	--	100	
$V_F$	Clamp forward voltage	Figure 8	$I_F = 350\text{ mA}$		--	1.7	2	V
$I_{I(off)}$	Off-state input current	Figure 3	$V_{CE} = 50\text{ V}$ ,	$I_C = 500\text{ }\mu\text{A}$	50	65	--	$\mu\text{A}$
$I_I$	Input current	Figure 4	$V_I = 3.85\text{ V}$		--	0.93	1.35	mA
			$V_I = 5\text{ V}$		--	--	--	
			$V_I = 12\text{ V}$		--	--	--	
$I_R$	Clamp reverse current	Figure 7	$V_R = 50\text{ V}$		--	--	50	$\mu\text{A}$
				$T_A = 70^\circ\text{C}$	--	--	100	
$C_i$	Input capacitance		$V_I = 0$ , $f = 1\text{ MHz}$		--	15	25	pF

**Switching Characteristics (TA = +25°C, unless otherwise specified)**

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low- to high-level output	See Figure 9		0.25	1	$\mu\text{s}$
$t_{PHL}$	Propagation delay time, high- to low-level output	See Figure 9		0.25	1	$\mu\text{s}$
$V_{OH}$	High-level output voltage after switching	$V_S = 50\text{ V}$ , $I_O = 300\text{ mA}$ , See Figure 9	$V_S - 20$			mV

## Parameter Measurement Information

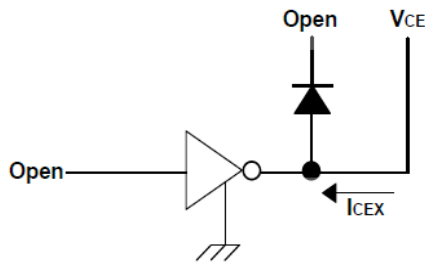


Fig.1  $I_{CEX}$  Test Circuit

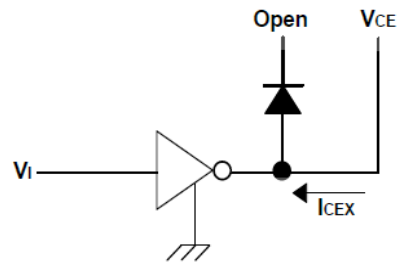


Fig.2  $I_{CEX}$  Test Circuit

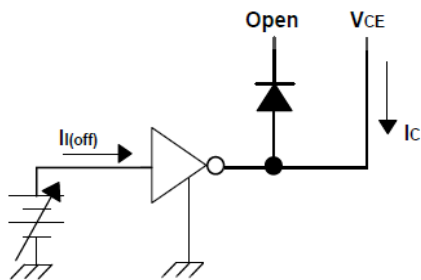


Fig.3  $I_{i(off)}$  Test Circuit

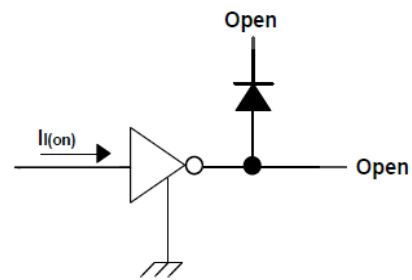


Fig.4  $I_i$  Test Circuit

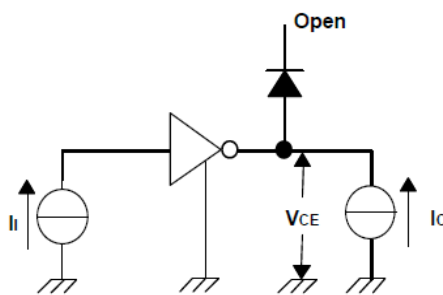


Fig.5  $h_{FE}$ ,  $V_{CE(sat)}$  Test Circuit

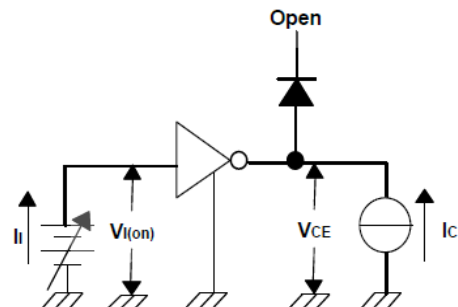


Fig.6  $V_{i(on)}$  Test Circuit

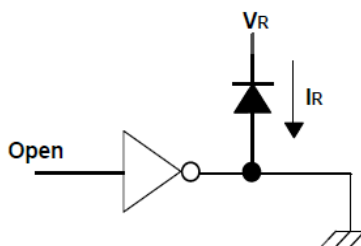


Fig.7  $I_R$  Test Circuit

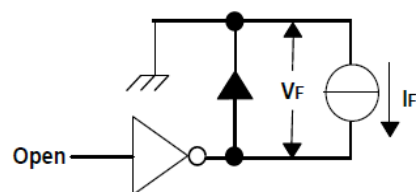
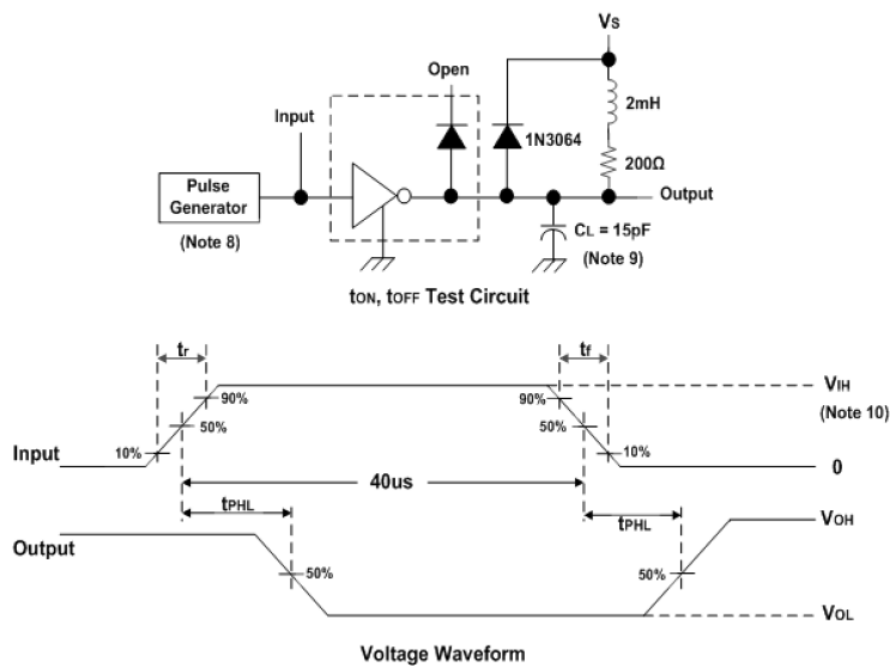


Fig.8  $V_F$  Test Circuit



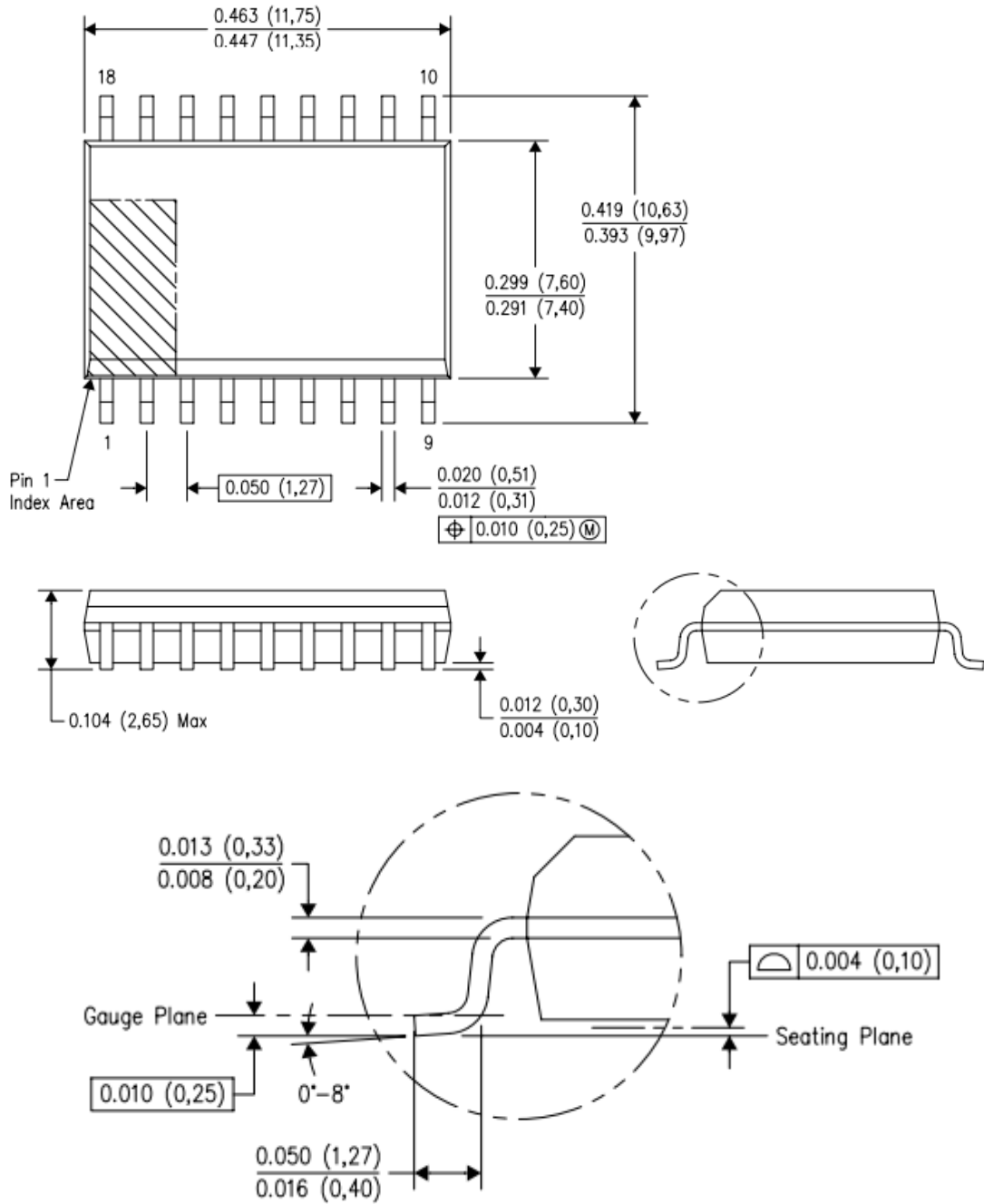
**Fig. 9 Latch-Up Test Circuit and Voltage Waveform**

Notes: 9. The pulse generator has the following characteristics: PRR = 12.5 kHz,  $Z_o = 50 \Omega$ .

10.  $C_L$  includes probe and jig capacitance.

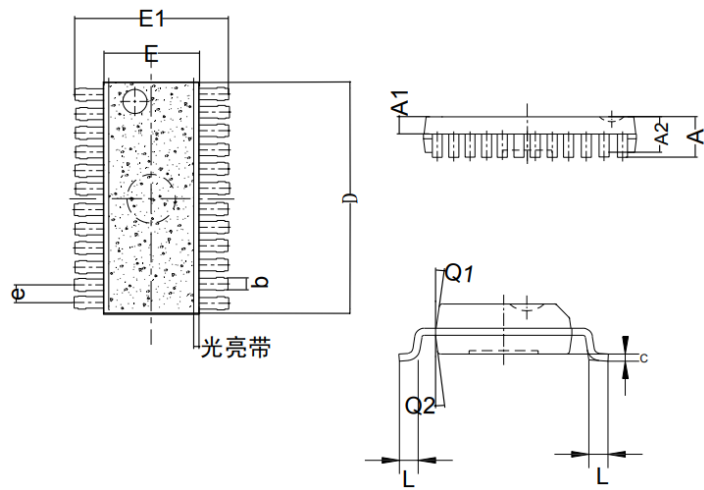
11.  $V_{IH}=3V$

## SOP-18 Outline Dimensions





SSOP24/QSOP24 Outline Dimensions



COMMON DIMENSIONS CUNITS MEASURE=MILLIMETER			
SYMBOL	MIN	MID	MAX
A	1.35	1.60	1.75
A1	0.65	0.70	0.75
A2	1.35	1.45	1.55
b	0.20	0.25	0.30
c	0.17	0.20	0.25
D	8.60	8.65	8.70
e	-	0.635TYP	-
E1	5.76	5.96	6.16
E	3.80	3.90	4.00
L	0.40	0.60	0.80
Q1	0°	/	8°
Q2	0°	/	8°

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