

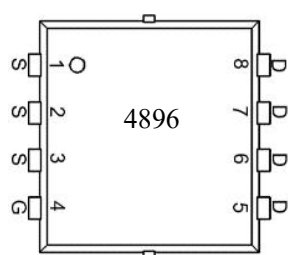
**Features**

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

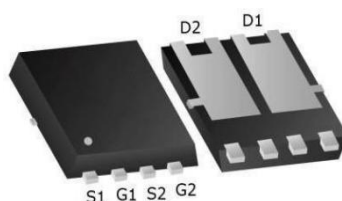
 B_{vds} **40V** **R_{dson}** **7.2m Ω** **I_D** **40A****Application**

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

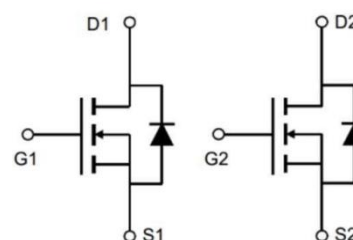
RoHS

Package

Marking and pin assignment



PDFN3x3-8L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
4896	S4896D	PDFN3x3-8L	5000

Absolute Maximum Ratings ($T_C=25^{\circ}\text{C}$ unless otherwise specified)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current, $V_{GS}@10^1$	$T_A=25^{\circ}\text{C}$	I_D	40	A
	$T_A=100^{\circ}\text{C}$		20	A
Pulsed Drain Current ²		I_{DM}	180	A
Single Pulsed Avalanche Energy ³		EAS	26.1	mJ
Avalanche Current		I_{AS}	15	A
Total Power Dissipation ⁴		P_D	43.6	W
Operating Junction Temperature Range		T_J	-55 ~ 150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ 150	$^{\circ}\text{C}$



Thermal Resistance Ratings

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance,Junction-to-Case ¹	$R_{\theta JC}$	--	2.8	°C/W
Thermal Resistance,Junction-to-Ambient ¹	$R_{\theta JA}$	--	62	°C/W

Ordering Information

Ordering Number	Package	Pin Assignment						Packing
Halogen Free		G1	G2	D1	D2	S1	S2	
HLS4896D	PDFN3x3-8L	2	4	7,8	5,6	1	3	Tape Reel

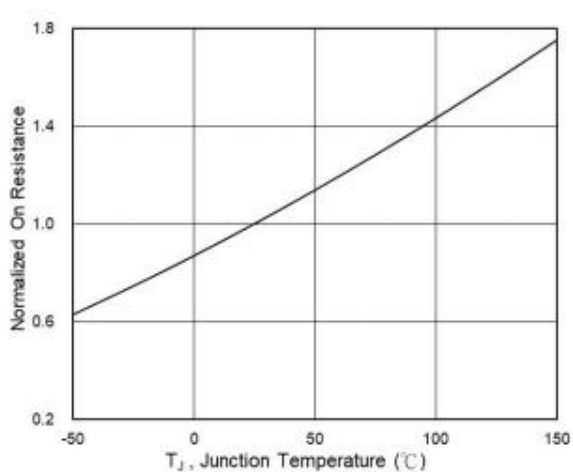
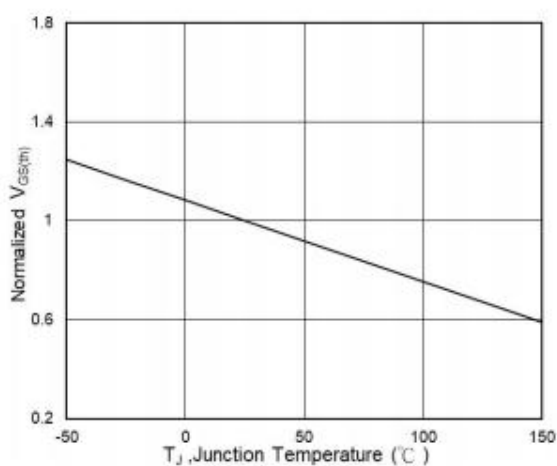
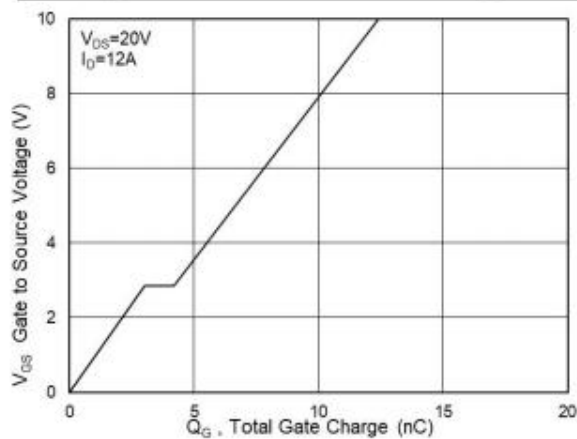
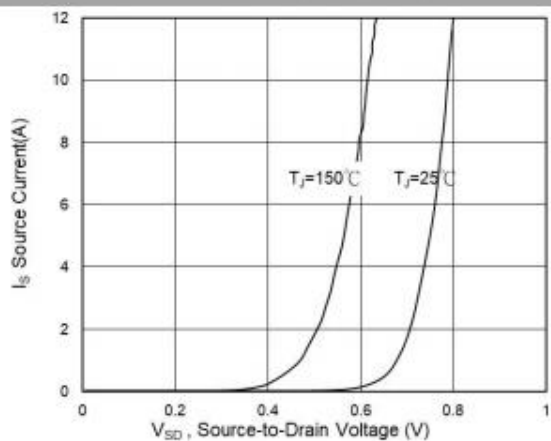
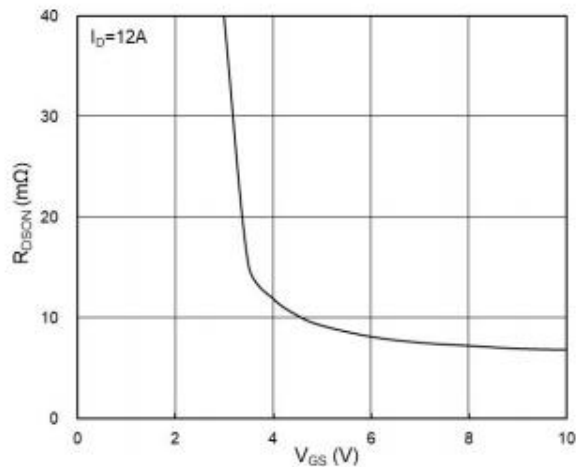
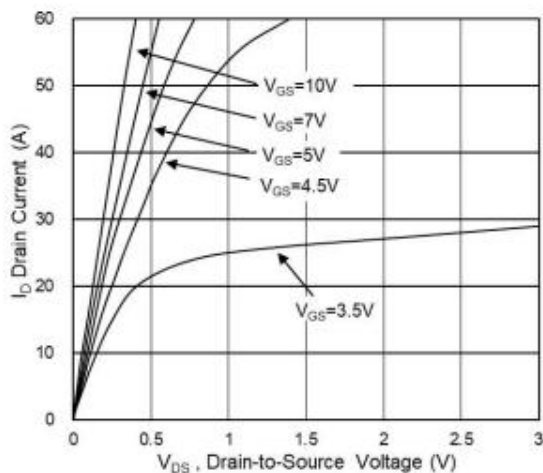
Electrical Characteristics (T_J=25°C, unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=32V, V_{GS}=0V$	-	-	1	μA
Gate to Body Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.35	-	3	V
Static Drain-Source On-Resistance ²	$R_{DS(on)}$	$V_{GS}=10V, I_D=12A$	-	7.2	9.5	m Ω
		$V_{GS}=4.5V, I_D=10A$	-	10	15	
gate Resistance	R_g	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	-	1.7	-	Ω
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	-	690	-	pF
Output Capacitance	C_{oss}		-	193	-	
Reverse Transfer Capacitance	C_{rss}		-	38	-	
Total Gate Charge	Q_g	$V_{DS}=20V, V_{GS}=4.5V, I_D=12A$	-	5.8	-	nC
Gate-Source Charge	Q_{gs}		-	3	-	
Gate-Drain Charge	Q_{gd}		-	1.2	-	
Turn-on Delay Time	$T_{d(on)}$	$V_{GS}=10V, V_{DD}=15V, R_G=3.3\Omega, I_D=1A$	-	14.3	-	nS
Turn-on Rise Time	t_r		-	5.6	-	
Turn-Off Delay Time	$T_{d(off)}$		-	20	-	
Turn-Off Fall Time	T_f		-	11	-	
Maximum Continuous Drain to Source Diode Forward Current ^{1,5}	I_S	$V_G=V_D=0V, \text{Force Current}$	-	-	40	A
Maximum Pulsed Drain to Source Diode Forward Current	I_{SM}	-	-	-	-	A
Drain to Source Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=1A$	-	-	1	V

Notes:

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=31A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics



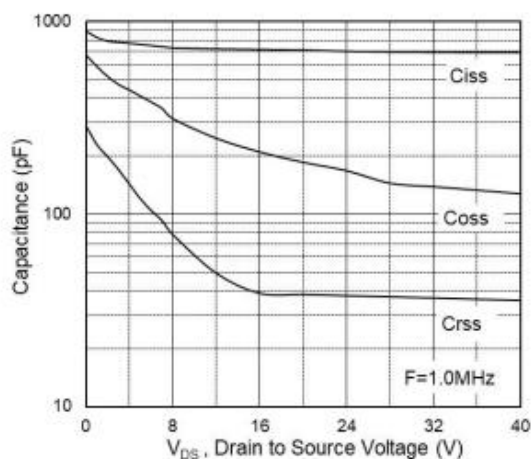


Fig.7 Capacitance

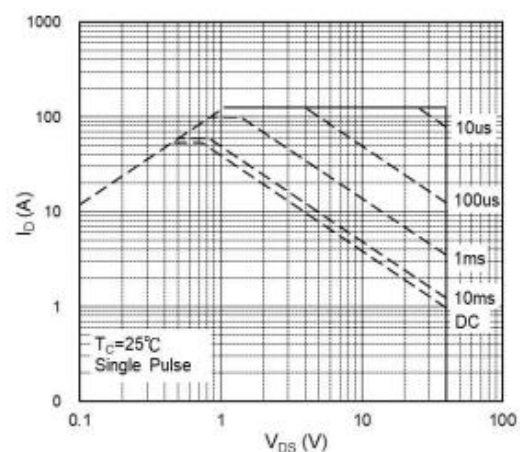


Fig.8 Safe Operating Area

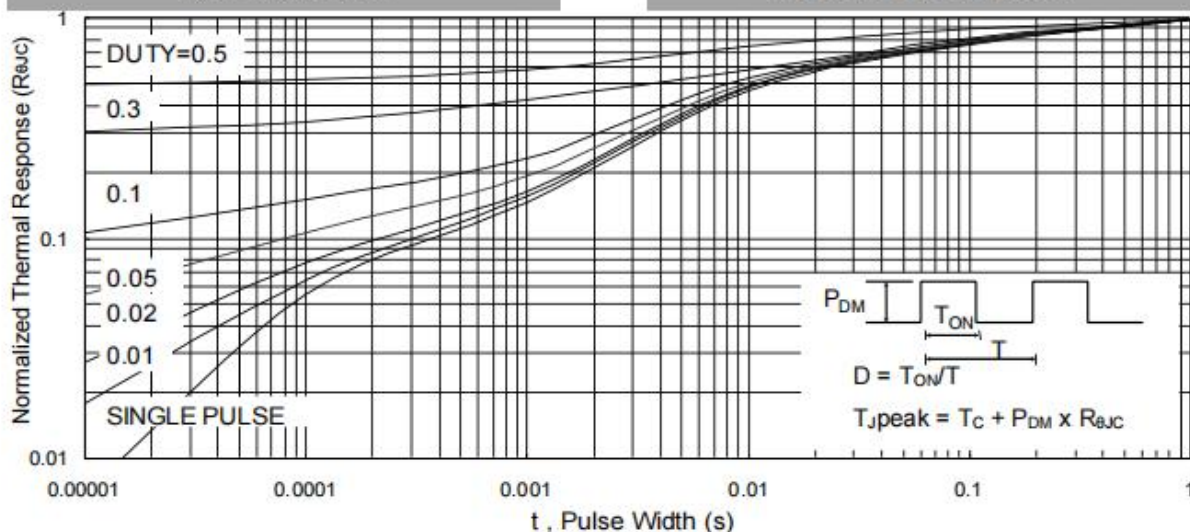
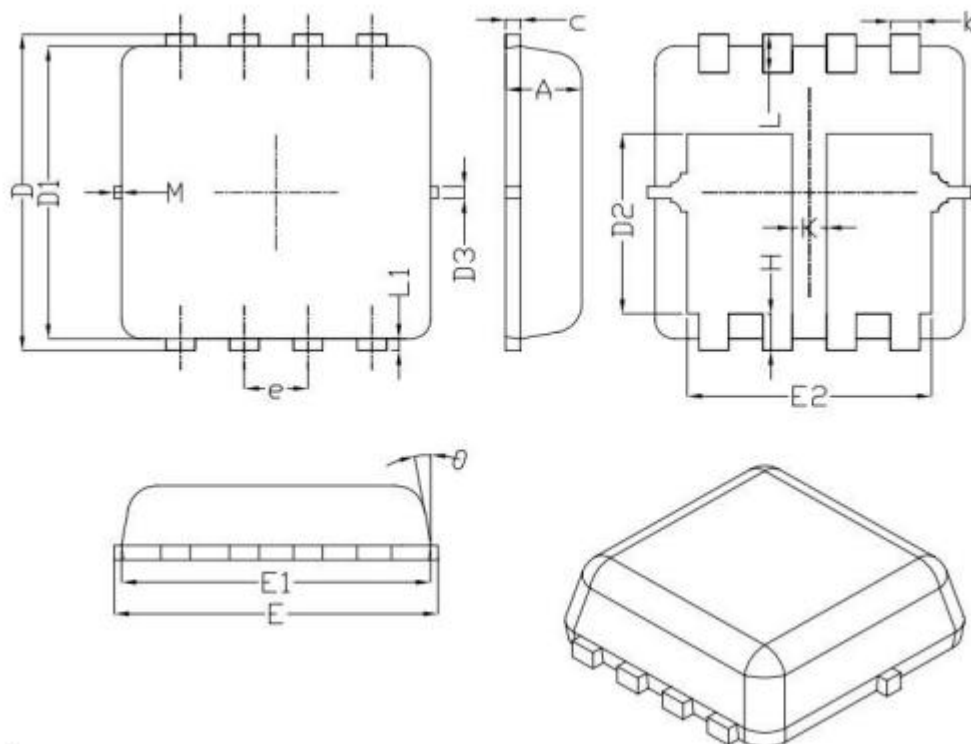


Fig.9 Normalized Maximum Transient Thermal Impedance

Package Dimensions PDFN3x3-8L



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	--
K	0.30	--	--
θ	--	10°	12°
M	*	*	0.15
* Not Specified			

Notes:

1. Refer to JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion.



Important Notice and Disclaimer

HL Microelectronics reserves the right to make changes to this document and its products and specifications at any time without notice.

Customers should obtain and confirm the latest product information and specifications before final design, purchase or use.

HL Microelectronics makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, not does HL Microelectronics assume any liability for application assistance or customer product design.

HL Microelectronics does not warrant or accept any liability with products which are purchased or used for any unintended or unauthorized application.

No license is granted by implication or otherwise under any intellectual property rights of HL Microelectronics.

HL Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of HL Microelectronics.