VA9105

Mono Class D Amplifier with Integrated Boost Controller For 2-Cell Battery Application

General Description

The VA9105 is a cost-effective, space saving filter-less Class D mono audio power amplifier featured with integrated of one current-mode boost controller. VA9105 is capable of delivering continuous 20W output at 18V boosted supply within 10% distortion at 8Ω load. With the filter-less output filter design and fully differential input, VA9105 is ideal to provide excellent sound quality with good RF noise immunity on portable electronics devices.

VA9105 integrates a current-mode boost controller with fast response and high efficiency. With 6V to 13.2V input voltage, it could boost the lower input voltage such as single cell Li-ion battery output to higher and then makes the audio amplifier operates at higher voltage to reduce the distortion.

The VA9105 is available in cost-effective TSSOP-28 green package with exposed pad.

Features

Mono Class D Amplifier

- Operation Voltage from 6V to 20V
- 8Ω Speaker:
  - 20W@18V with 8.5% THD+N
- Fully Differential Input
- Programmable Two Gains
- Configurable Output Power Limit
- Excellent EMI Performance
- Short Circuit and Thermal protection

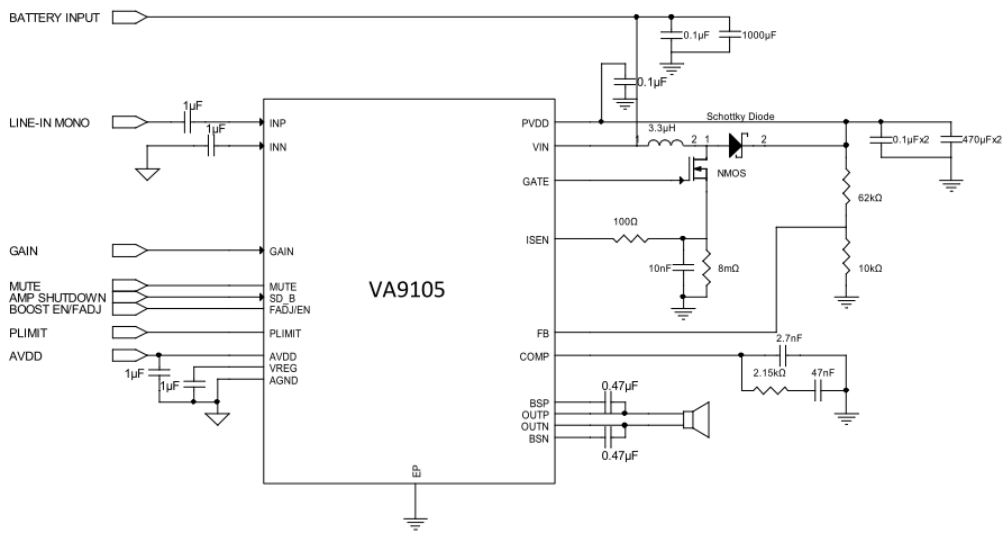
Boost Controller

- Input Voltage From 6V to 13.2V
- Adjustable output Voltage: from 6V to 20V
- Up to 90% Efficiency
- Adjustable PWM Frequency

Package

- RoHS 2.0 compliant TSSOP-28 Green Package with Exposed Pad

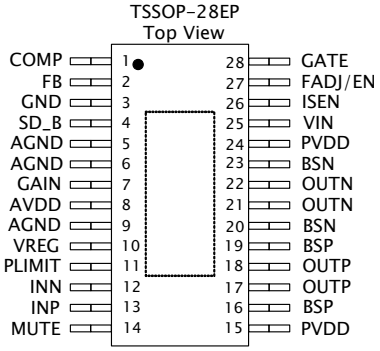
Typical Application



Applications

- Battery Powered Portable Speakers

Pin Assignments And Descriptions



Pin No.	Pin	I/O/P	Function Description
1	COMP	-	Compensation. Use a RC/C network to do proper loop compensation.
2	FB	I	Output Feedback. Connect the external resistor divider network from output to this pin to sense output voltage. The FB pin voltage is regulated to internal 1.26V reference voltage.
3	GND	P	Ground. Connect to exposed pad.
4	SD_B	I	Amplifier shutdown control terminal. Low active. TTL Logic levels with compliance to AVDD.
5	AGND	P	Analog Ground.
6	AGND	P	Analog Ground.
7	GAIN	I	Gain selection bit. Pull it low for 26dB gain and pull it high for 36dB gain. TTL logic level with compliance to AVDD.
8	AVDD	P	Analog Power Supply.
9	AGND	P	Analog Power Ground.
10	VREG	O	Internal Regulated Voltage Output.
11	PLIMIT	I	Power Limit Level Adjust. Connect a resistor divider from VREG to GND to set power limit. Connect to VREG directly for no power limit.
12	INN	I	Audio signal negative audio signal input.
13	INP	I	Audio signal positive audio signal input.
14	MUTE	I	Mute signal for fast disable/enable of outputs (HIGH = outputs Hi-Z, LOW = outputs enabled). Low voltage level compliance to VREG.
15	PVDD	P	Power Stage supply.
16	BSP	-	Bootstrap I/O for positive channel high-side switch.
17	OUTP	O	Right channel positive output.
18	OUTP	O	Right channel negative output.
19	BSP	-	Bootstrap I/O for positive channel high-side switch.
20	BSN	-	Bootstrap I/O for negative channel high-side switch.
21	OUTN	O	Negative output.
22	OUTN	O	Negative output.
23	BSN	-	Bootstrap I/O for negative channel high-side switch.
24	PVDD	P	Power Stage supply.
25	VIN	P	Boost Controller Supply Input.
26	ISEN	O	Current Sense. Use an external resistor in series with ground to measure the voltage drop.
27	FADJ/EN	I	Boost Frequency Adjust/Synchronization/Shutdown. A resistor connected from this pin to ground simply sets the oscillator frequency. An external clock signal at this pin will synchronize the controller to the clock. Pull on this pin for ≥ 30 µs will turn the device off and the boost controller will then very few current about 10µA from the supply.
28	GATE	O	Gate Drive. Connect this terminal to the gate pin of the external MOSFET.
EP	GND	P	System Ground,

Absolutely Maximum Ratings

Over operating free-air temperature range, unless otherwise specified (* 1)

Symbol	Parameter	Limit	Unit
V_{IN}(VIN)	Boost Controller Supply voltage	-0.3 to 30	V
V_{DD}(PVDD, AVDD)	Amplifier supply voltage	-0.3 to 30	V
V_{IN} (COMP, FADJ, FB, INN, INP, MUTE, PLIMIT)	Amplifier Input voltage	0 to 6	V
V_{IN}(SD_B, GAIN)	Boost Input Voltage	0 to 30	V
V_{ISEN}	Current Sense Input	-0.4 to 0.6	V
T_A	Operating free-air temperature range	-40 ~ +85	°C
T_J	Operating junction temperature range	-40 to +150	°C
T_{STG}	Storage temperature range	-65 to 150	°C
$R_{(LOAD)}$	Minimum load resistance	8	Ω
Electrostatic discharge	Human body model	±2	kV
Electrostatic discharge	Machine model	±200	V

(*1): Stress beyond those listed at "absolute maximum rating" table may cause permanent damage to the device. These are stress rating ONLY. For functional operation are strongly recommend follow up "recommended operation conditions" table.

Recommended Operating Conditions

Over operating free-air temperature range, unless otherwise specified.

Symbol	Parameter	Test Condition	Specification		Unit
			Min	Max	
V_{IN}	Boost controller supply voltage	V_{DD}=18V	6	13.2	V
V_{DD}	Amplifier supply voltage		6	20	V
$V_{IH(HIGH)}$	High level input voltage (SD_B, GAIN)	V_{DD}=6V	2.0	V_{DD}	V
$V_{IH(LOW)}$	Low level input voltage (MUTE)	V_{DD}=6V	2.0	5	V
V_{IL}	Low Level Input Voltage (SD_B, GAIN, MUTE)		-	0.4	V
R_I	Analog External Input Resistor		39	-	kΩ

Electrical Characteristics

T_A = 25℃, V_{IN}=7V, V_{DD}(A_{VDD}/P_{VDD})=18V, R_L=8Ω, GAIN=26dB, unless otherwise noted.

Symbol	Parameter	Test Condition		Specification			Unit
				Min	Typ.	Max	
$\|V_{OS}\|$	Output offset voltage (measured differentially)	V_I=0V			1.5	15	mV
I_Q	Quiescent current (For AMP)	SD_B=2V, No load			50		mA
I_{SD}	Shutdown current (For AMP)	SD_B=0.4V, FADJ=3V, No load			400	600	μA
t_{ON}	Shutdown turn-on time	SD_B=2V			20		ms
t_{OFF}	Shutdown turn-off time	SD_B=0.4V			2		μs
f_{OSC}	Internal oscillation frequency				250		kHz
A	Amplifier gain	GAIN=0			26		dB
		GAIN=1			36		
$R_{DS(ON)}$	Drain-Source ON resistance[1]	V_{DD}=12V, I_{OUT}=500mA	High Side		100		mΩ
			Low Side		100		
V_{REG}	Regulator output	I_{VREG} = 100μA, V_{DD}=6~20V			5.8		V
t_{DC-DET}	DC detect time				450		ms
$t_{HYSTERSIS}$	OTP hystersis				20		℃
I_{OCP}	Over-current trap threshold				7		A

(1) Design center value.

Operating Characteristics

T_A = 25℃, V_{IN}=7V, V_{DD}(A_{VDD}/P_{VDD})=18V, R_L=8Ω, GAIN=26dB, unless otherwise noted.

Symbol	Parameter	Test Condition		Specification			Unit
				Min	Typ.	Max	
P_O	Output power	f=1kHz, R_L=8Ω *	THD+N=1%		17.5		W
			THD+N=10%		21.6		
THD+N	Total harmonic distortion plus noise	P_O=10W, R_L=8Ω, f=1kHz			0.06		%
$\|V_{OS}\|$	Offset voltage				20		mV
$\|K_{SVR}\|$	Supply ripple rejection ration	Input AC-Grounded, C_i=1μF, f=1kHz			65		dB
|SNR|	Signal-to-Noise ratio	A-weighted, THD+N=1%, R_L=8Ω			78		dB
V_n	Output voltage noise	C_i=1μF, f=20Hz to 20kHz, A-weighted, Input AC-Grounded			160		μV_{RMS}
|CMRR|	Common mode rejection ratio	V_{DD}=18V, V_{IC}=1V_{PP}	f=120Hz		63		dB
Z_I	Input impedance				60		kΩ

(*) Heat-sink is required.

Functional Descriptions

Gain Settings

The gain of the VA9105 can be set by the GAIN pin. The gain ratios listed in Table 1 are implemented by changing the taps on the feedback resistors in the preamplifier stage.

The input resistance is depended on the gain setting. Since the gain setting is determined by the ratio of the internal feedback resistive network, the variation of the gain is small. But the absolute value of the input resistance may shift by ±20% at the same gain. In actual design cases, 80% of nominal value should be assumed as the input resistance of VA9105 in the input network of whole amplifier.

GAIN	Gain Ratio	Resistance	Range
1	36dB	9kΩ	7.2kΩ~10.8kΩ
0	26dB	30kΩ	24kΩ~36kΩ

Table 1. Gain Setting

Amplifier Input Impedance

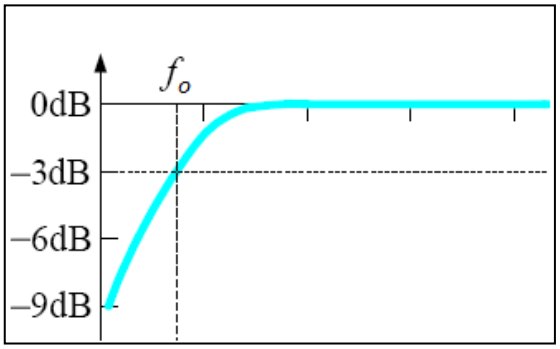


Figure 2. Cut-off point of high-pass filter

In most cases, no extra resistor needs to be added on the input of VA9105. The actual input resistor is already determined while selecting the gain. If a single capacitor is used in the input high-pass filter, the cut-off frequency *fo* may vary with the change of gain setting. The -3dB point of the cut-off frequency can be calculated by the following equation,

$$fo = \frac{1}{2\pi \times R_I \times C_I} \quad \text{(Hz)} \quad \text{Equation (2)}$$

,where the R_I values is given in Table 1.

Shutdown Operation

The VA9105 employs a state of shutdown mode to reduce supply current to the absolute minimum level during periods of nonuse for power conservation. This terminal should be held high during normal operation when the amplifier is in normal operating. Pulling low causes the output drivers shutdown and the amplifier to enter a low-current state. Do not leave it unconnected, because there is no weakly pulling resistor inside the amplifier.

Remember that to place the amplifier in the shutdown state prior to removing the power supply voltage so that power-off pop noise can be eliminated.

VREG Supply

The V_{REG} Supply is used to bias the gates of the output full-bridge upper half MOSFETs. It could be used to supply the PLIMIT pin and related voltage divider circuit. Add at least 1μF capacitor to ground at this pin.

Speaker Protection

Due to the nature of Class D amplifiers, the speakers may have DC current if the audio inputs get DC voltage in any case. An output DC fault will make internal fault function in low state and shuts down the audio amplifier and change the state of output into high impedance.

Functional Descriptions (cont.)

To resolve the case of DC input, it is good to treat it as very low frequency sine wave much lower than audio band such as 2Hz. Based on this criteria, a DC detect fault shall be issued when the output differential duty-cycle of either channel exceeds 14% for more than 500ms at the same polarity. This feature protects the speakers away from large currents.

The minimum differential input DC voltages required to trigger the DC detection fault are listed in Table 2.

A_V (dB)	V_{IN} (mV, Differential)
36	17
26	56

Table 2. DC detect fault threshold

To resume the normal operation, it is necessary to power off the amplifier and then power on, cycling SD_B can not resume normal operation.

Short Circuit Protection

VA9105 has protection from over-current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the internal fault function to low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SD_B pin through the low state.

Thermal Protection

Thermal protection on the VA9105 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±30°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 30°C. VA9105 will be back to normal operation at this point with no external system interaction.

Thermal protection fault will not be reported on the internal fault function terminal.

Power Limit Operation

The voltage at PLIMIT terminal (pin 11) can be used to limit the power to levels below that which is possible based on the supply rail. Add a resistor divider from VREG to ground to set the voltage at the PLIMIT terminal. An external reference may also be used if precise limitation is required. Also add a 1μF capacitor from this pin to ground.

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to power rail. This "virtual" rail is 5 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L}$$

V_P=5 x PLIMIT voltage if PLIMIT<5 x V_P

P_{OUT} (with 10% THD) = 1.25 x P_{OUT}

where R_S is the total series resistance including $R_{DS(ON)}$ and any resistance in the output filter. R_L is the load resistance. V_P is the peak amplifier of the

Functional Descriptions (cont.)

output possible within the supply rail.

V_{DD}(V)	R_L(Ω)	PLIMIT(V)	Po@THD+N (W)	
			10%	1%
12	8	0.93	1.328	1.005
12	8	1.107	1.923	1.452
12	8	1.33	2.955	2.118
12	8	1.434	3.527	2.536

Table 3. PLIMIT value vs. Output Power

Due to the VREG driving ability limitation, it is not recommended to use this pin to drive other circuits except PLIMIT resistor network. The recommended resistor network is shown on Figure 3.

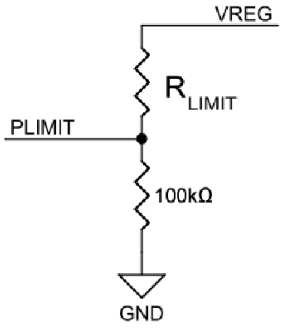


Figure 3. PLIMIT Pin Voltage Divider

Use the simple voltage divider to determine the voltage on PLIMIT pin from VREG pin by the following equation:

$$V_{PLIMIT} = V_{VREG} \frac{100\,k\Omega}{100\,k\Omega + R_{LIMIT}}$$

In order to maintain the regulation of VREG pin well please apply higher resistor value such as 100kΩ on low side resistor but should not less than 50kΩ.

Application Information

Output Filter

Design the VA9105 without the filter if the traces from amplifier to speaker are short (< 10cm), where the speaker is in the same enclosure as the amplifier is a typical application for class D without a filter. Many applications require a ferrite bead filter at least. The ferrite filter reduces EMI above 30MHz. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies, be aware of its maximum current limitation.

Use an LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and there are long wires from the amplifier to the speaker.

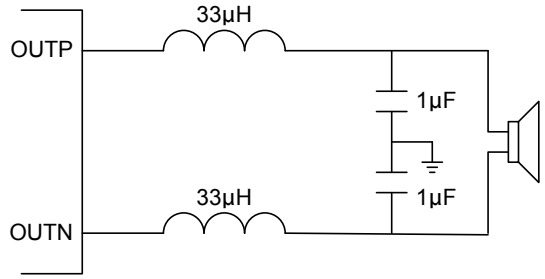


Figure 4. Typical LC Output Filter, Speaker Impedance=8Ω

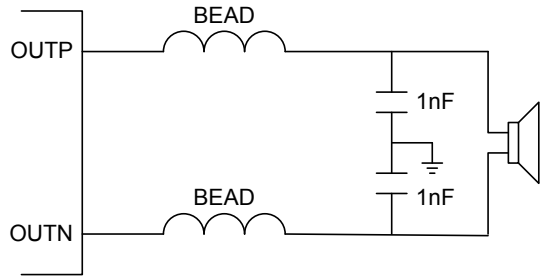


Figure 5. Typical Ferrite Chip Bead Output Filter

Inductors used in LC filters must be selected carefully. A significant change in inductance at the peak output current of the VA9105 will cause increased distortion. The change of inductance at currents up to the peak output current must be less than 0.1µH per amp to avoid this. Also note that smaller inductors than 33µH may cause an increase in distortion above what is shown in preceding graphs of THD versus frequency and output power.

Like the selection of the inductor in LC filters, the capacitor must be selected carefully, too. A significant change in capacitance at the peak output voltage of the VA9105 will cause increased distortion. LC filter capacitors should be double of DC voltage ratings of the peak application voltage (the power supply voltage) at least. In general, it is strongly recommended using capacitors with good temperature performance like X7R series.

Output Snubbers

In Figure 6, the 330pF capacitors in series with 10Ω resistors connected with the outputs of the VA9105 are snubber circuits. They smooth switching transitions and reduce overshoot and ringing. With these networks, THD+N can be improved at lower power levels and EMC can be reduced 2~4 dB at middle frequencies. They increase quiescent current by 3mA~11mA depending on supply voltage.

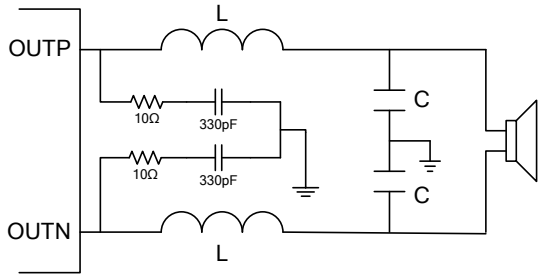


Figure 6. Output Snubber Circuits

Low ESR Capacitors

Low ESR capacitors are high recommended for this application. In general, a practical capacitor can

Application Information (cont.)

be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this unwanted resistor can eliminate the effects of the ideal capacitor. Place low ESR capacitors on supply circuitry can improve THD+N performance.

Boot-Strap Capacitors

The full H-bridge output stages use only MOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 0.47μF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding boot-strap input. Specifically, one 0.47μF capacitor must be connected from OUTP to BSP, and one 0.47μF capacitor must be connected from OUTN to BSN.

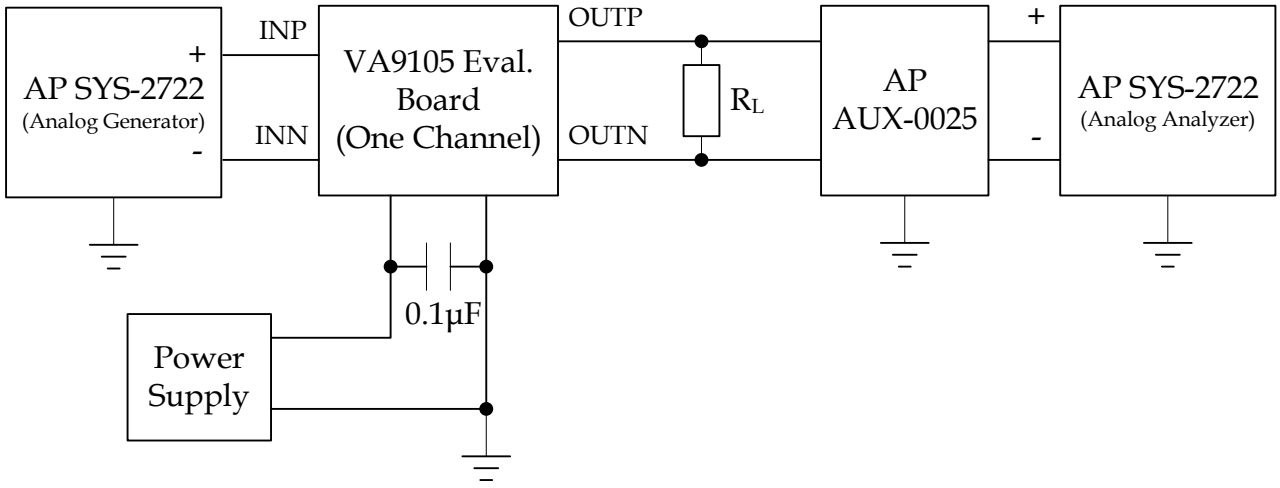
The bootstrap capacitors connected between the BSP or BSN pins and corresponding output function as a floating power supply for the high side N-channel power MOSFET gate drive circuitry. During each high side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

Decoupling Capacitors

VA9105 requires appropriate power decoupling to minimize the output total harmonic distortion (THD) and improves EMC performance. Power supply decoupling also prevents intrinsic oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling can be achieved by using two different types of capacitors which target different types of noise on the power supply lines. For higher frequency spikes, or digital hash on the rail, a good low ESR ceramic capacitor, for example 0.1μF to 10μF, placed as close as possible to all PVDD pins works best. For filtering lower frequency noise, a larger low ESR aluminum electrolytic capacitor of 470μF or greater placed near the audio power amplifier is suggested. The 470μF capacitor also serves as local storage capacitor for supplying current during heavy power output on the amplifier outputs. The PVDD terminals provide the power to the output transistors, so a 470μF or larger capacitor should be placed by PVDD terminals as near as possible. And 0.1uF, 10μF ceramic capacitor on each PVDD terminal is also recommended.

Typical Characteristic

Test Setup Connection Diagram



* Remove all L/C (BEAD) filter components on board before performing all measurements.

Figure No.	Description
7	Frequency Response (7V to 18V† @26dB)
8	Noise (8Ω@26dB)
9	SNR (8Ω@26dB)
10	THD+N vs. Frequency (7V to 18V@26dB)
11	THD+N vs. Output Power (7V to 18V@1kHz)
12	THD+N vs. Output Power (7V to 18V)
13	THD+N vs. Output Power vs. Analog Input
14	Efficiency vs. Output Power

(†) Boost V_{IN}=7V, Amplifier V_{DD}=18V.

Typical Characteristic (cont.)

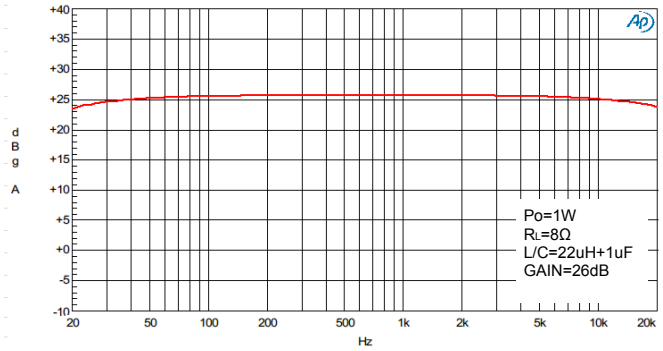


Figure 7. Frequency Response (7V to 18V@26dB)

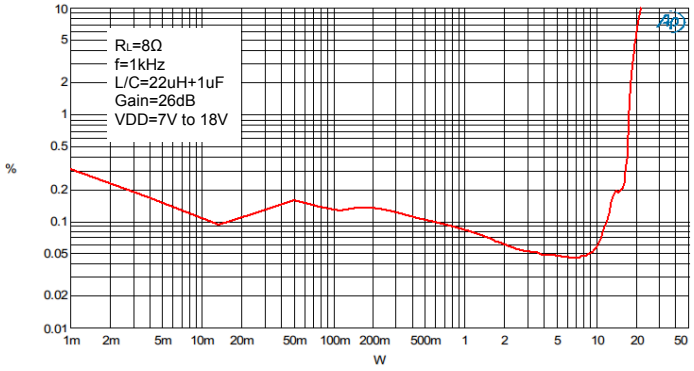


Figure 11. THD+N vs. Output Power (7V to 18V@1kHz)

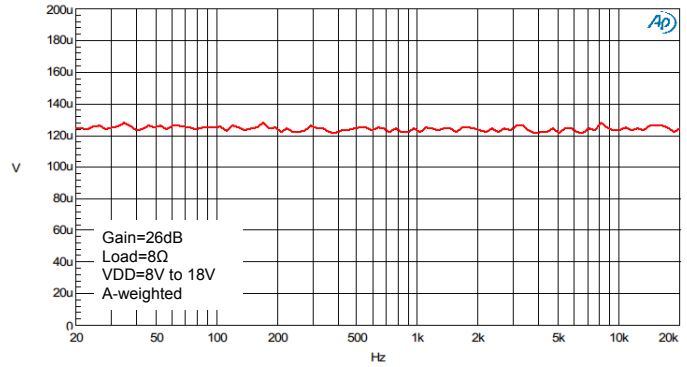


Figure 8. Noise (8Ω@26dB)

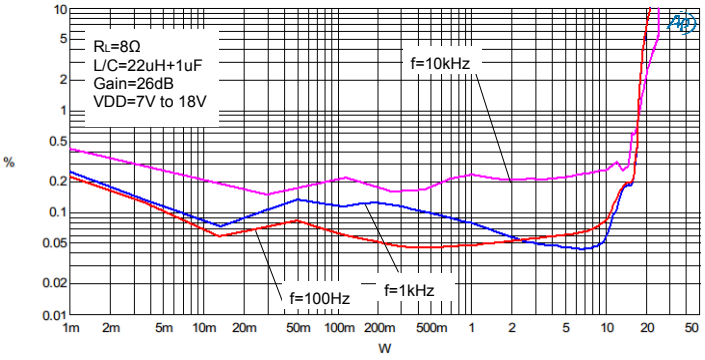


Figure 12. THD+N vs. Output Power (7V to 18V)

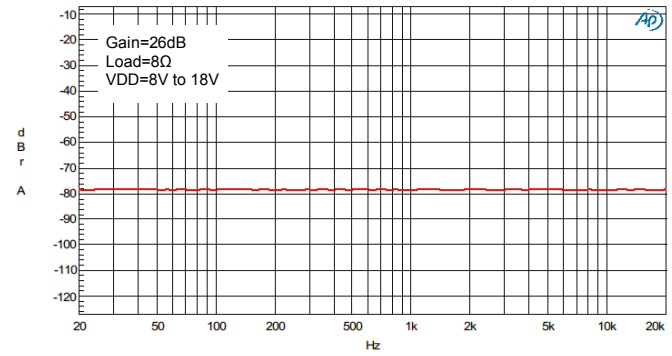


Figure 9. SNR (8Ω@26dB)

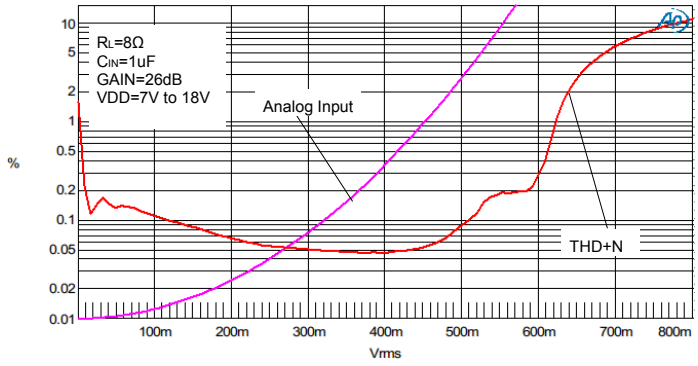


Figure 13. THD+N vs. Analog Input (7V to 18V)

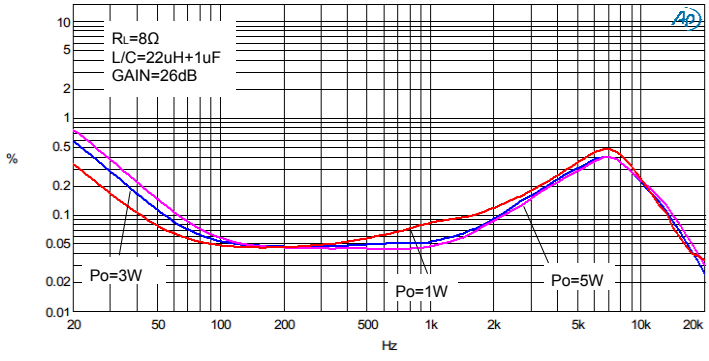


Figure 10. THD+N vs. Frequency (7V to 18V@26dB)

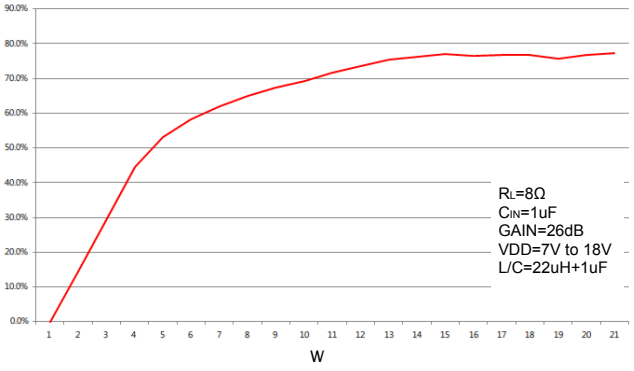
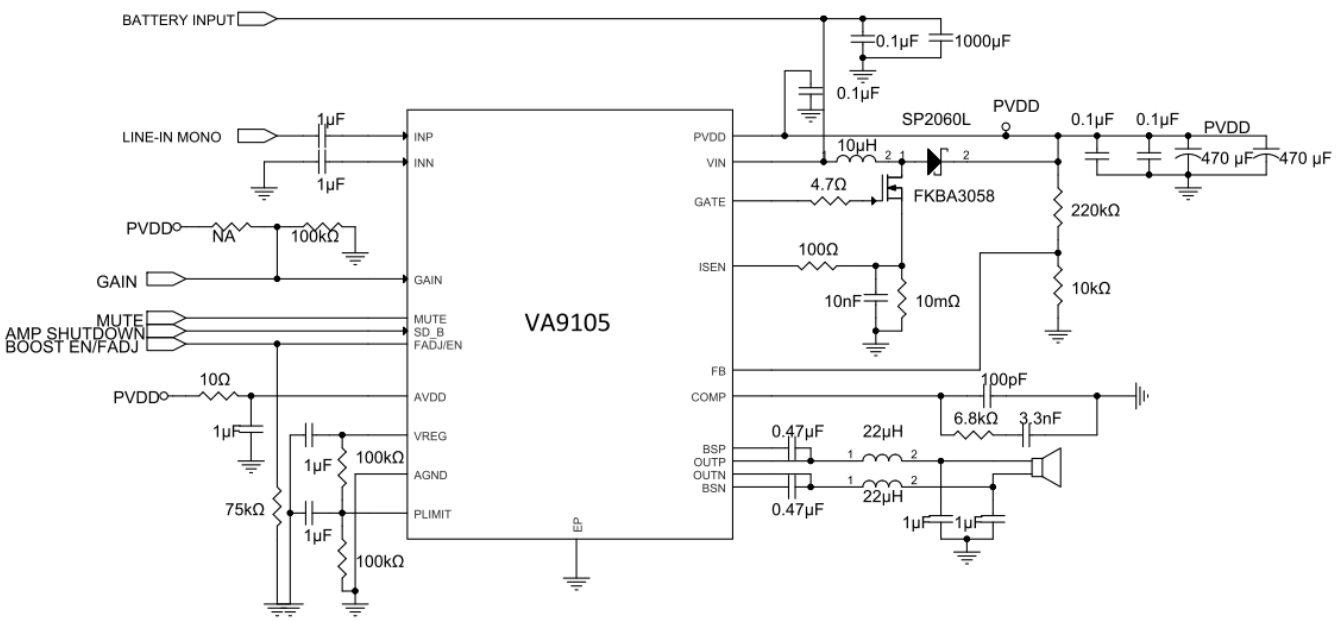


Figure 14. Efficiency vs. Output Power

Application Circuit



Reference Input:

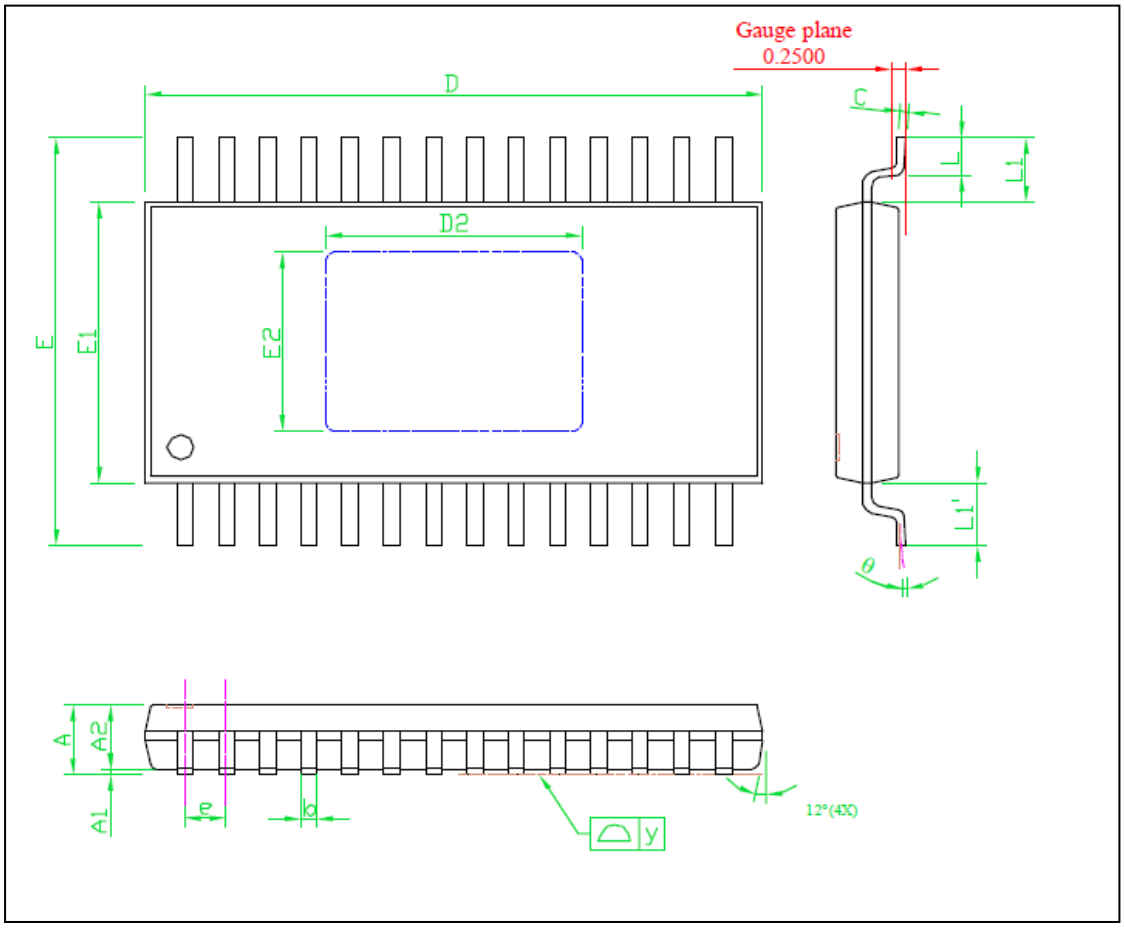
V_{IN}=7V (Norminal), V_{DD}= 17.3V, Load=8Ω, Gain=26dB

Result:

Po=20W, I_{IN}=3.92A, THD+N=8.5%

Package Information

TSSOP-28EP



NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS
2. TOLERANCE ±0.1 mm UNLESS OTHERWISE SPECIFIED
3. COPLANARITY : 0.1 mm
4. REFER TO JEDEC MO-153

SYMBOLS	DIMENSIONS IN MILLIMETER			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.15	—	—	0.045
A1	0.00	—	0.10	0.000	—	0.004
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	—	0.30	0.007	—	0.012
C	0.09	—	0.20	0.004	—	0.008
D	9.60	9.70	9.80	0.378	0.382	0.386
D2	3.70	3.80	3.90	0.146	0.150	0.154
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
E2	2.70	2.80	2.90	0.106	0.110	0.114
e	—	0.65	—	—	0.026	—
L	0.45	0.60	0.75	0.018	0.024	0.030
y	—	—	0.10	—	—	0.004
θ	0°	—	8°	0°	—	8°
⚠ |L1-L1'|	—	—	0.12	—	—	0.005
⚠ L1	1.00REF			0.039REF		

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