Bootstrap circuit design for the CIPOS™ IPM series

Application note

About this document

Scope and purpose

The scope of this application note is to describe the basic requirements of the CIPOS™ IPM series for bootstrap circuit design.

Intended audience

Power electronics engineers who want to design a bootstrap circuit for the CIPOS™ IPM series.

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1 Bootstrap circuit design

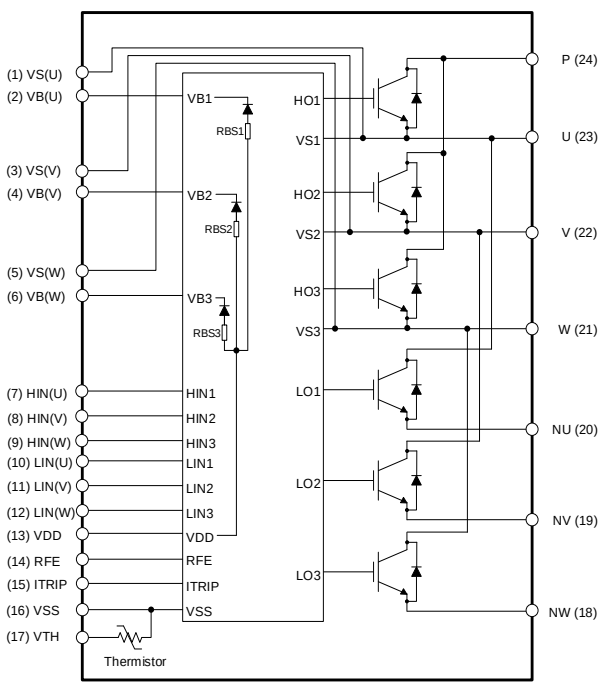
1.1 Bootstrap circuit operation

The V_{BS} voltage, which is the voltage difference between $V_{B\,(U,V,W)}$ and $V_{S\,(U,V,W)}$, provides the supply to the high-side gate driver (GD) IC within the CIPOS™ IPM. This supply voltage (V_{BS}) is recommended to be in the range of 12.5 ~ 18.5 V to ensure that the GD IC can fully drive the high-side switches (IGBTs or MOSFETs). The CIPOS™ IPM includes an undervoltage detection function for the V_{BS} to ensure that the GD IC does not drive the high-side switches if the V_{BS} voltage drops below a specified voltage (see datasheet). This function prevents the switch from operating in a high dissipation mode. Please note here that the undervoltage lockout function of any high-side section acts only on the triggered channel without any feedback to the control level.

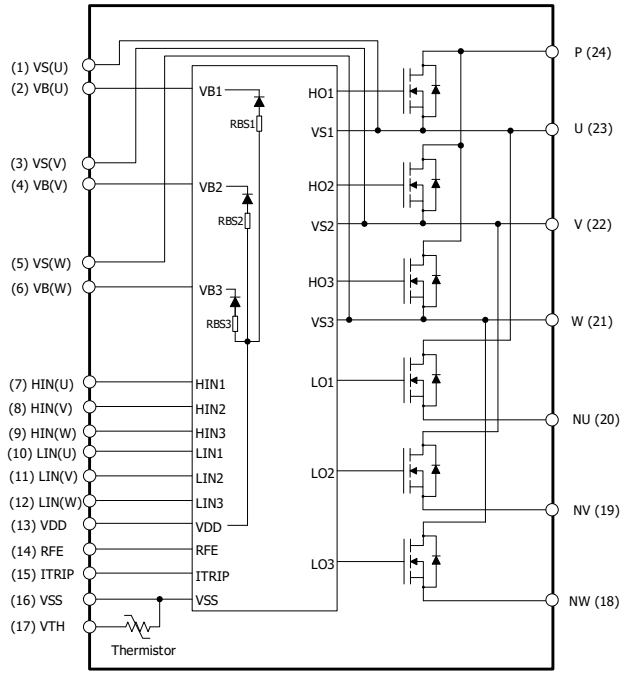
There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here. This method has the advantage of being simple and inexpensive. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of a bootstrap diode (D_{BS}), resistor (R_{BS}) and capacitor (C_{BS}) as shown in Figure 4 (a). The current flow path of the bootstrap circuit is shown in Figure 4 (a). When V_S is pulled down to ground (either through the low side or the load), C_{BS} is charged through D_{BS} and R_{BS} from the V_{DD} supply.

1.1.1 Internal bootstrap functionality characteristics

The CIPOS™ IPM integrates three bootstrap functionalities in the internal GD IC, which consist of three diodes and three resistors, as shown in Figure 1. A typical value of R_{BS} of the CIPOS™ Maxi family is 120 Ω at room temperature. For more information, please refer to Figure 2 and Table 1.



(a) IM818-MCC

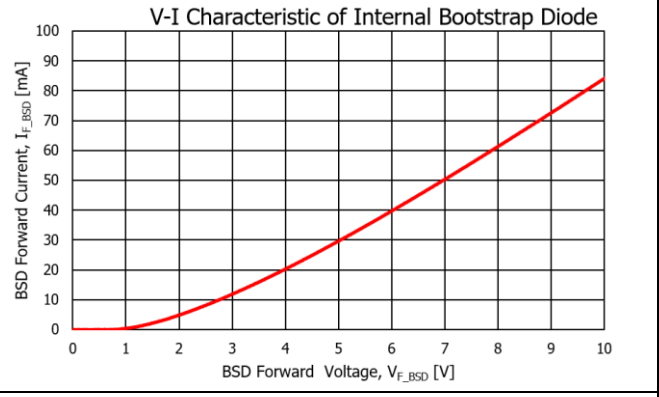


(b) IM828-XCC

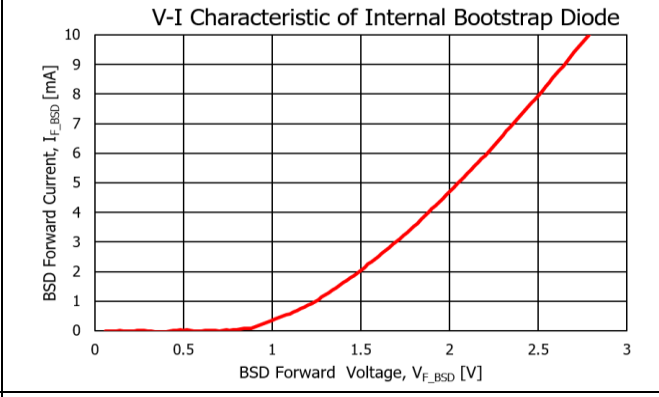
Figure 1 Internal block diagram of CIPOS™ Maxi family

Bootstrap circuit design

V_{DD} of 15 V is recommended when only the integrated bootstrap circuitry is used.



(a) I_F - V_F characteristics



(b) I_F - V_F characteristics (zoom-in)

Figure 2 Internal bootstrap diode I_F - V_F characteristics

Table 1 Electrical characteristics of internal bootstrap parameters

Description	Conditions	Symbol	Value			Unit
			Min.	Typ.	Max.	
Repetitive peak-reverse voltage		V_{RRM}	1200	-	-	V
Diode resistance	Between V_F = 4 V and V_F = 5 V	R_{BS}	-	120	-	Ω
Diode forward voltage	I_F = 0.3 mA	V_{F_BS}	-	0.9	-	V

1.1.2 Initial charging of bootstrap capacitor

Once we assume that the user uses a single-pulse charging method, the time required for the initial charge depends on the capacitance of C_{BS}, the forward voltage of bootstrap diode (V_{F_BSD}) and the resistance of R_{BS}. The charge is performed with a time constant that is roughly calculated from the capacitance of C_{BS} and the resistance of R_{BS}.

Example of simulation charging waveform is shown in Figure 3.

Conditions: CIPOS™ Maxi IM818-MCC (1200 V / 10 A, D_{BS} and R_{BS} (120 Ω) are embedded on GD IC), C_{BS} = 22 µF / 100 µF, V_{DD} = 15 V and R_{SHUNT} = 20 mΩ.

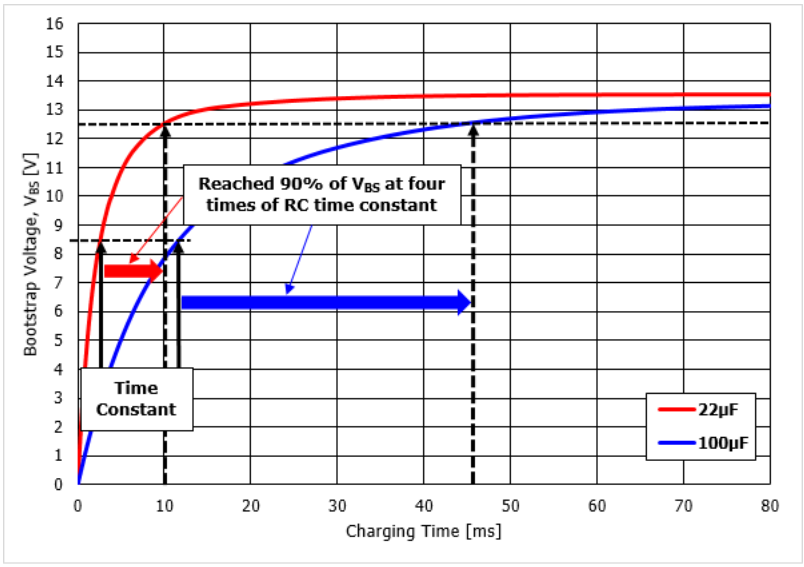
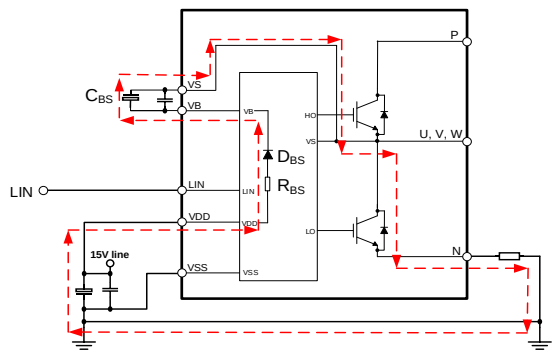
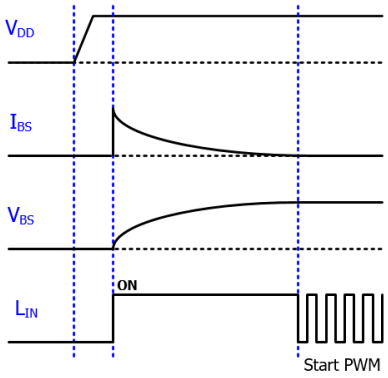


Figure 3 Example of initial charging of bootstrap

As in Figure 3, the V_{BS} does not reach the target voltage (only around 62%) by charging up to the time constant (e.g. τ = R x C = 120 Ω x 22 µF = 2.64 ms). To reach 90% of the target voltage (12.6 V), approximately four times the time constant (τ) will be needed. Target voltage does not reach the control power supply voltage (V_{DD}). It will be approximately 1.0 V lower than V_{DD} due to the voltage drop of the low-side IGBT ($V_{CE(Sat)}$) and D_{BS} (V_F) which are in the charging path (see Figure 4 a).



(a) Bootstrap circuit



(b) Timing chart of initial bootstrap charging

Figure 4 Bootstrap circuit operation and initial charging

Initial charging needs to be performed until the V_{BS} (voltage of C_{BS}) exceeds the recommended minimum bootstrap voltage (V_{BS_min}) 12.5 V. It is recommended to charge as high as possible taking into account the voltage drop between the end of charging and the start of inverter operation.

1.1.3 Voltage drop during pause state of inverter operation

Bootstrap voltage (V_{BS}) will gradually decrease due to the circuit current of the GD IC during the pause state of inverter operation. The V_{BS} drop ratio will be estimated by calculating the capacitance of C_{BS} and quiescent current of the high-side GD IC, I_{QBS} (e.g. typical 175 µA at V_{DD} = 15 V for CIPOS™ Maxi IM818-MCC).

ΔV_{BS} (voltage drop) = I_{QBS} x $t_{discharge}$ / C_{BS}

When the pause state continues for a long time, and V_{BS} goes below 12.5 V (the recommended minimum control voltage for V_{BS}), it is necessary to recharge to C_{BS} before starting operation. An example of voltage drop calcuation for IM818-MCC is shown in Figure 5. Conditions are as follows: initial V_{BS} = 13.7 V, I_{QBS} is a variable value influenced by bootstrap volage (V_{BS}), C_{BS} = 22 and 100 µF)

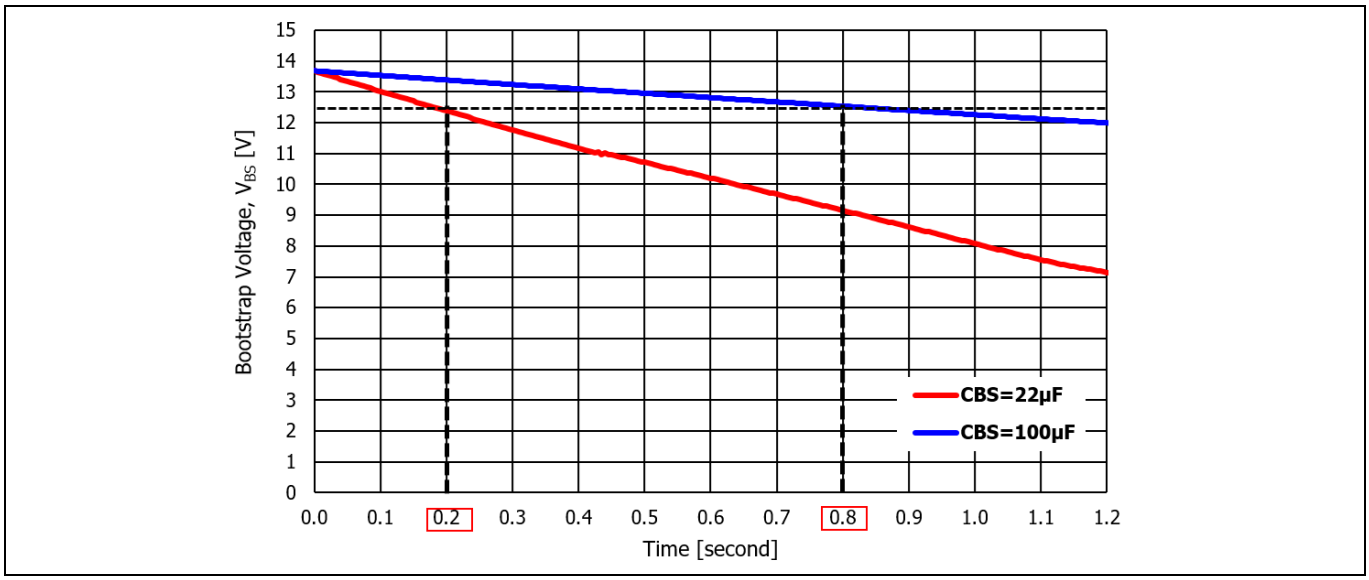


Figure 5 Example of voltage drop of V_{BS} during pause time (IM818-MCC at given conditions)

When the pause state continues over 0.2 s with C_{BS} = 22 µF, V_{BS} will drop below 12.5 V. So, recharging will be required before a restart. If it continues over 0.7 s, V_{BS} will drop below 9.5 V (minimum voltage of undervoltage lockout function) and the undervoltage protection may work. This is only a calculation example, and ultimately needs to be evaluated in the actual system.

1.2 Bootstrap voltage (V_{BS}) charging during inverter operation

The energy of C_{BS}, which was consumed by the internal circuit operating current (e.g. gate charge for high-side IGBT) during the inverter operation by PWM signals like 3-phase space vector pulse width modulation (SVPWM), is recharged through the bootstrap diode (D_{BS}) when V_{BS} becomes lower than the 15 V control supply voltage (V_{DD}), as the output terminal (U, V, W) is changed to the GND level during the low-side IGBT turn-on period or low-side freewheeling period after high-side IGBT turns off.

However, the charge current practically starts flowing when V_{BS} is approximately 1.0 V lower than the low-side control supply 15 V, as D_{BS} needs to turn on. (Figure 6)

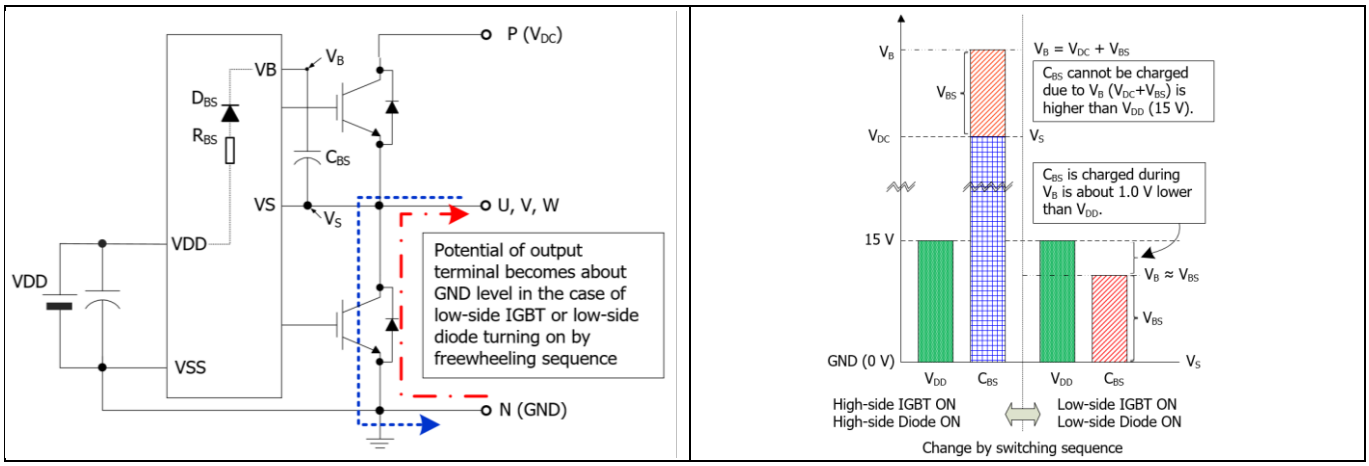


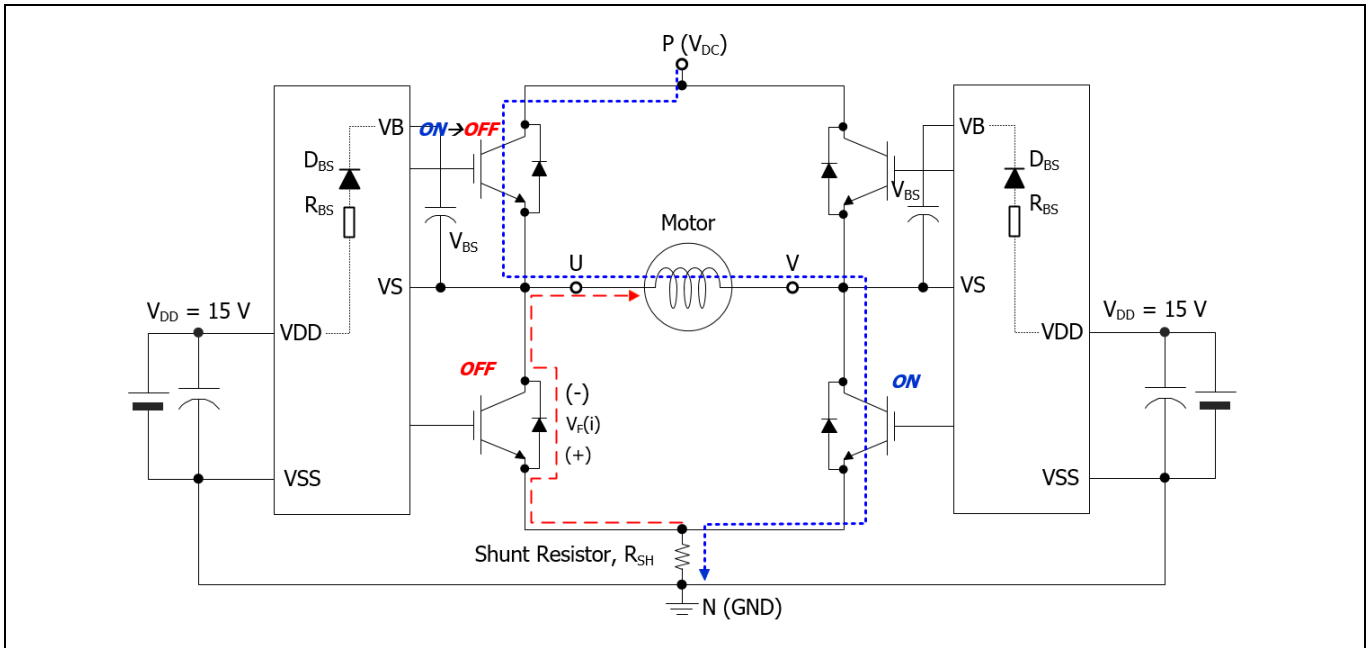
Figure 6 V_{BS} charging conditions

Because the potential of the output terminal changes depending on the direction of the motor current flow, i.e. the device (low-side IGBT or diode) into which the current flows, the potential of C_{BS} (V_B), which goes by potential of output terminal, also changes. So, C_{BS} is not always charged when the low-side IGBT or diode turns on. The charging situation is explained below.

There are two different charging situations during inverter operation:

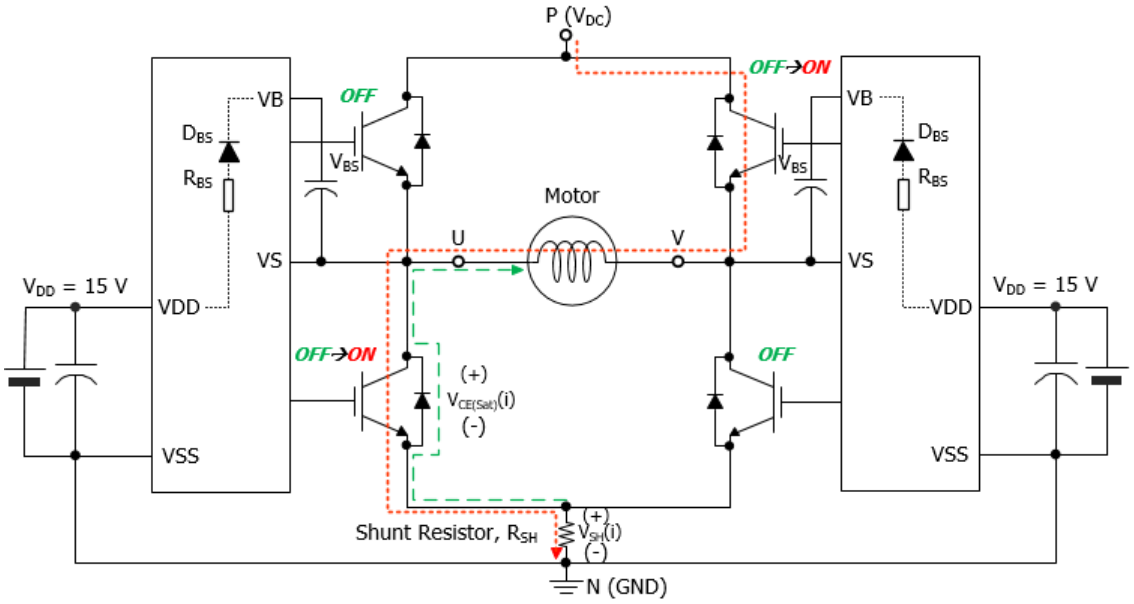
- Mode 1: Freewheeling situation of the low-side diode after high-side turns off
- Mode 2: Current flowing situation into the low-side IGBT

Current flow chart for both modes is illustrated in Figure 7. The charge mode is decided by the output current direction (Figure 8).



[Mode 1]

The potential of the U(VS(U)) terminal is changed to the GND level, and charging starts when the U-phase, low-side diode turns on as a result of the freewheeling current following turn-off of high-side IGBT.



[Mode 2]
The potential of the U(VS(U)) terminal is changed to the GND level, and charging starts when U-phase, low-side IGBT turns on.

Figure 7 V_{BS} charging mode when currents flows between U and V phases

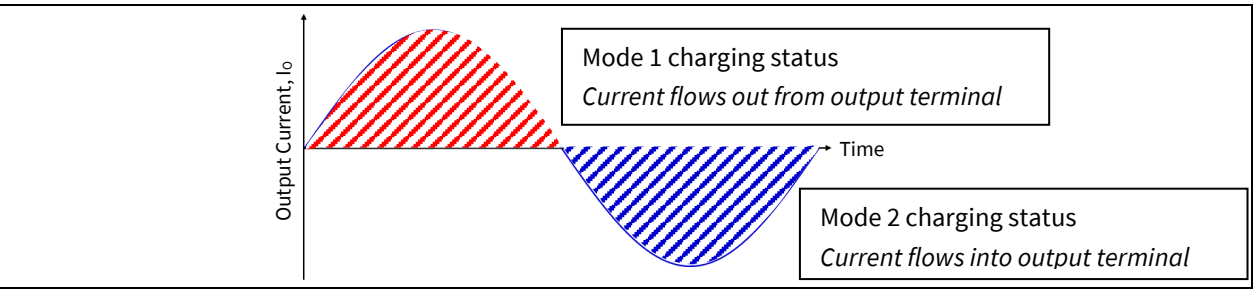


Figure 8 Relationship between output current (I_O) waveform and charging mode

The potential of the output terminal (i.e. reference voltage of V_{BS}) depends on the forward voltage ($V_F(i)$) in Mode 1, or the saturation voltage of IGBT ($V_{CE(Sat)}(i)$) and the voltage drop by the shunt resistor ($V_{SH}(i)$) in Mode 2, as shown below.

- Mode 1: Voltage of output terminal = GND potential (0 V) – $V_F(i)$ < 0 V
- Mode 2: Voltage of output terminal = GND potential (0 V) + $V_{CE(Sat)}(i)$ + $V_{SH}(i)$ > 0 V

Because the V_{BS} (voltage by charge stored in C_{BS}) can be changed by the potential of the output terminal, the voltage potential of C_{BS} (V_B) then is as follows in Figure 9.

- Mode 1: $V_B = V_{BS} - V_F(i)$
- Mode 2: $V_B = V_{BS} + V_{CE(Sat)}(i) + V_{SH}(i)$

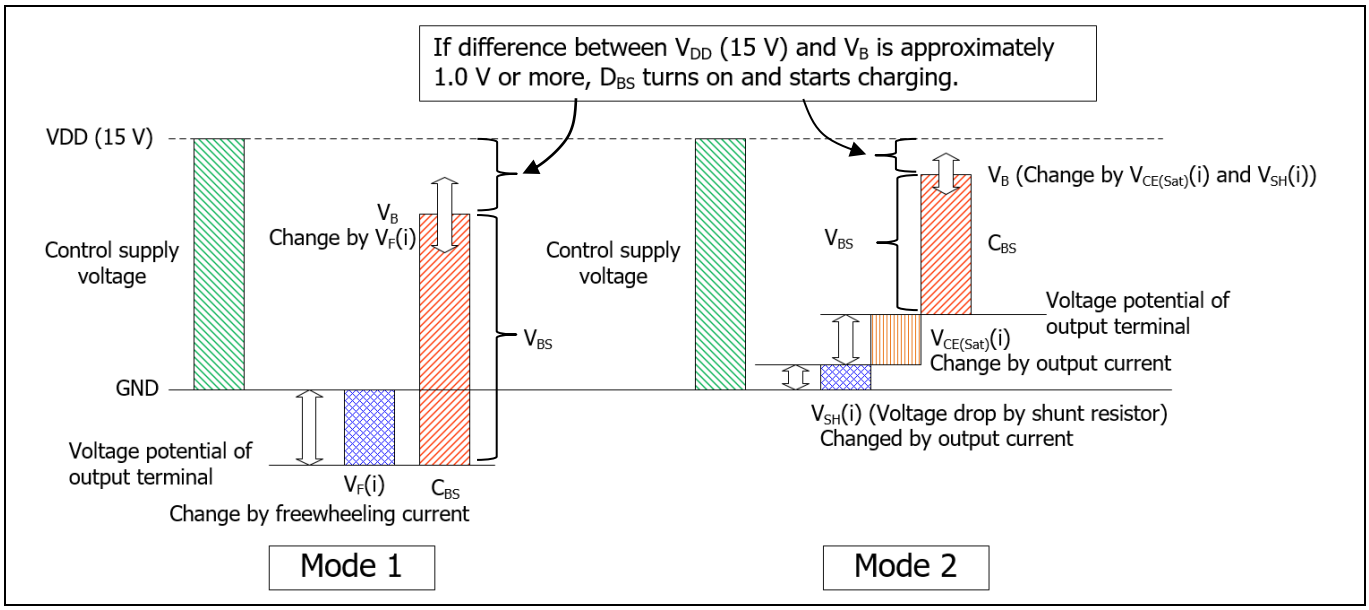


Figure 9 Difference of potential V_{CBS} by charging modes

When the voltage difference between the control supply voltage (V_{DD} = 15 V) and V_B is about 1.0 V or more, D_{BS} turns on, and the charge current starts flowing. So the voltage of V_B, at which C_{BS} can be initially charged, is calculated as shown below.

- Mode 1: $15\ V - V_B \geq 1.0\ V$
  $15\ V + V_F(i) - 1.0\ V \geq V_{BS}$
- Mode 2 : $15\ V - V_B \geq 1.0\ V$
  $15\ V - V_{CE(Sat)}(i) - V_{SH}(i) - 1.0\ V \geq V_B$

For example, in the case of CIPOS™ Maxi IM818-MCC at about 0 A and 10 A collector current, the maximum V_{BS} (voltage by charge stored in C_{BS}), at which C_{BS} can start to be charged, is roughly estimated at each mode as below.

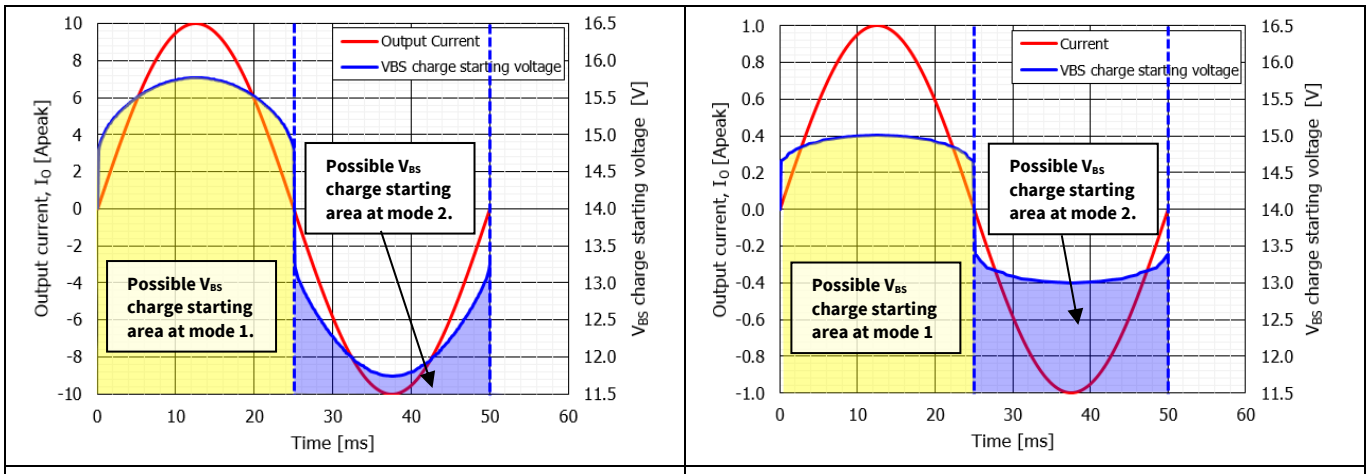
- Conditions: At I_C = 10 A, V_F = 1.76 V, $V_{CE(Sat)}$ = 2.06 V and shunt resistance = 20 mΩ
  At $I_C \approx 0$ A, V_F = 0.0 V, $V_{CE(Sat)}$ = 0 V and shunt resistance = 20 mΩ

Table 2 Electrical characteristics of internal bootstrap parameters

	I_C = 10 A	**I_C = 0 A**
Mode 1	15.76 V (15 V + 1.76 V - 1.0 V)	14.0 V (15 V + 0.0 V - 1.0 V)
Mode 2	11.84 V (15 V – 2.06 V - (0.02*10 A) - 1.0 V)	14.0 V (15 V – 0.0 V - (0.02 * 0 A) - 1.0 V)

In Table 2, it can be seen that the V_{BS} charging at mode 1 is able to start at higher V_{BS} than that at mode 2, i.e. V_{BS} is needed to drop further to start charging at mode 2. Since C_{BS} can start to be charged under this maximum voltage, it also means the maximum charged voltage by the bootstrap circuit depends on the output current and characteristics of power devices such as IGBTs and diodes.

Calculated charge starting voltage is described in Figure 10 under the following conditions: output current (10 A / 1 A and 20Hz) for the DUT IM818-MCC. This has helped us to understand that bootstrap voltage V_{BS} is related to output current amplitude.



(a) I_C = 10 Apeak | (b) I_C = 1 Apeak

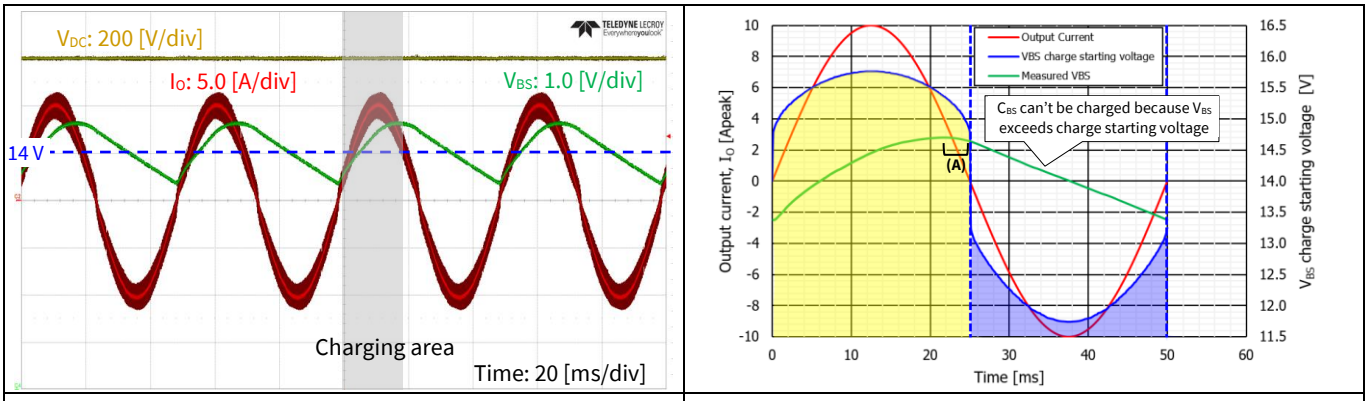
Figure 10 Expected V_{BS} charge starting voltage (F_O = 20Hz)

1.2.1 Charging scheme under the 3-phase SVPWM operation

This section shows the details of a charging scheme in the case of a 3-phase SVPWM. Figure 11 (a) shows the V_{BS} and output current waveforms of the CIPOS™ Maxi IM818-MCC (10 A / 1200 V) in real operation under the conditions shown below.

In this example, the capacitance of C_{BS} is selected intentionally at a smaller value for easy confirmation of the V_{BS} change in actual operation.

- Conditions: V_{DC} = 600 V, V_{DD} = 15 V, F_{SW} = 10 kHz, I_O = 10 Apeak, PF = 0.99, MI = 0.56, F_O = 20 Hz, C_{BS} = 10 µF, R_{shunt} = 20 mΩ, 3-phase SVPWM operation



(a) Example of bootstrap voltage waveform | (b) V_{BS} charging situation

Figure 11 Bootstrap voltage (V_{BS}) charge and discharge sequence

From Figure 11 (a), it can be confirmed that charging for C_{BS} was performed only in the Mode 1 period (positive output current), and discharging for C_{BS} continued in the Mode 2 period (negative output current).

Figure 11 (b) shows that the V_{BS} (voltage of C_{BS}) waveform was overlapped in Figure 10 (a) at 10 A. In this figure, we can see that C_{BS} can be charged during the positive output current period (Mode 1), but during the negative output current period (Mode 2), it cannot be charged, as the voltage of V_{BS} is higher than the charge starting voltage. Therefore, ***C_{BS} will mainly be charged in Mode 1 (positive current freewheeling to low-side diode)*** except for certain conditions like small capacitance of C_{BS} or slow output frequency. Here there are non-charged periods despite V_{BS} being lower than charge starting voltage. (Part A in Figure 11 (b)) The reasons are suggested below.

In part A, the voltage difference between the voltage of V_{BS} and the charge starting voltage is smaller, i.e. the voltage applied to D_{BS} is small and hence the charging current that flows into C_{BS} also decreases. It leads to a drop in V_{BS}, as the quantity of discharge exceeds that of the charge.

In addition, charging to C_{BS} can also be affected by other inverter operating conditions. In the next section, the effects on the charging situation due to operating conditions by 3-phase SVPWM are explained using simulation waveforms.

1.2.2 Effects on the charging situation by operating conditions

To consider the effects on the charging situation by operating conditions, the results of simulation of V_{BS} with various conditions are described here. The simulation conditions are as follows:

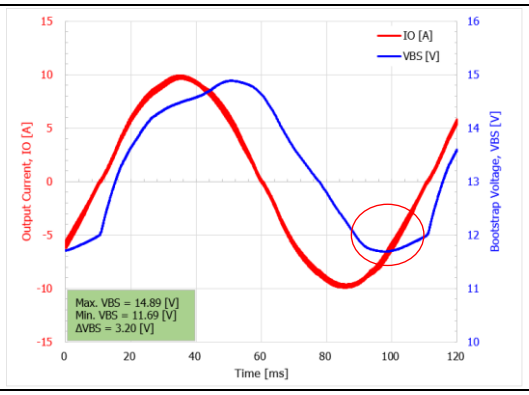
- Normal conditions
  - DUT : CIPOS™ Maxi IM818-MCC (1200 V / 10 A), F_{SW} = 10 kHz, F_O = 20 Hz, C_{BS} = 6.8 µF, power factor = 0.8, modulation index = 0.8, V_{DC} = 600 V, V_{DD} = 15 V, R_{shunt} = 20 mΩ, 3-phase SVPWM
- Comparative conditions (normal conditions are used, if not stated otherwise)
  - Output frequency, F_O : 10 / 20 / 60 / 120 Hz
  - Switching frequency, F_{SW} : 5 / 10 / 20 kHz
  - Capacitance of C_{BS} : 4.7 / 10 / 22 / 100 µF
  - Output current, I_O : 5 / 10 Apeak

(1) Comparison of output frequency, F_O : 10 / 20 / 60 / 120 Hz

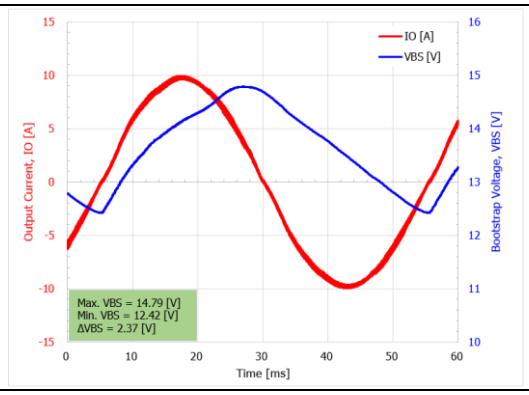
The results of simulation under four output-frequency conditions are shown in Figure 12. In Figure 12 (a) where the output frequency is 10 Hz, one cycle is longer and the Mode 2 period (negative output current area) is longer as well. The V_{BS} drops to under 12.5 V, which is the recommended minimum V_{BS} of IM818-MCC. Here, V_{BS} is partially charged under Mode 2 conditions due to excessive V_{BS} drops.

On the other hand, in Figure 12 (d) where the output frequency is 120 Hz, one cycle is shorter, so the V_{BS} drop is smaller. The ripple of the bootstrap voltage (ΔV_{BS}) is also smaller than one at 10 Hz.

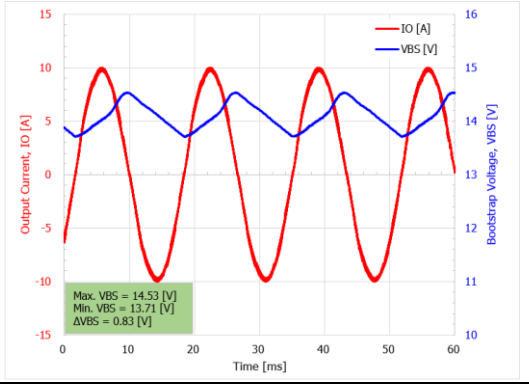
Under these normal operating conditions, if the lower output frequency operation (below 10 / 20Hz) is needed in your system, the capacitance of C_{BS} (6.8 µF) in the given conditions is not suitable. The reason for this is that the lower V_{BS} can lead to high power dissipation or to a system stop via the IPM protection function, i.e. undervoltage lockout. Therefore, sufficient evaluation is needed when designing bootstrap circuits.



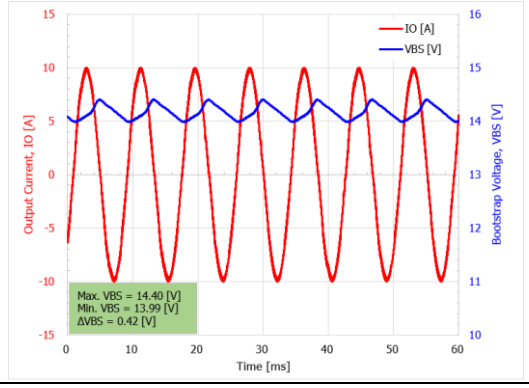
(a) F_O = 10Hz



(b) F_O = 20Hz



(c) F_O = 60Hz



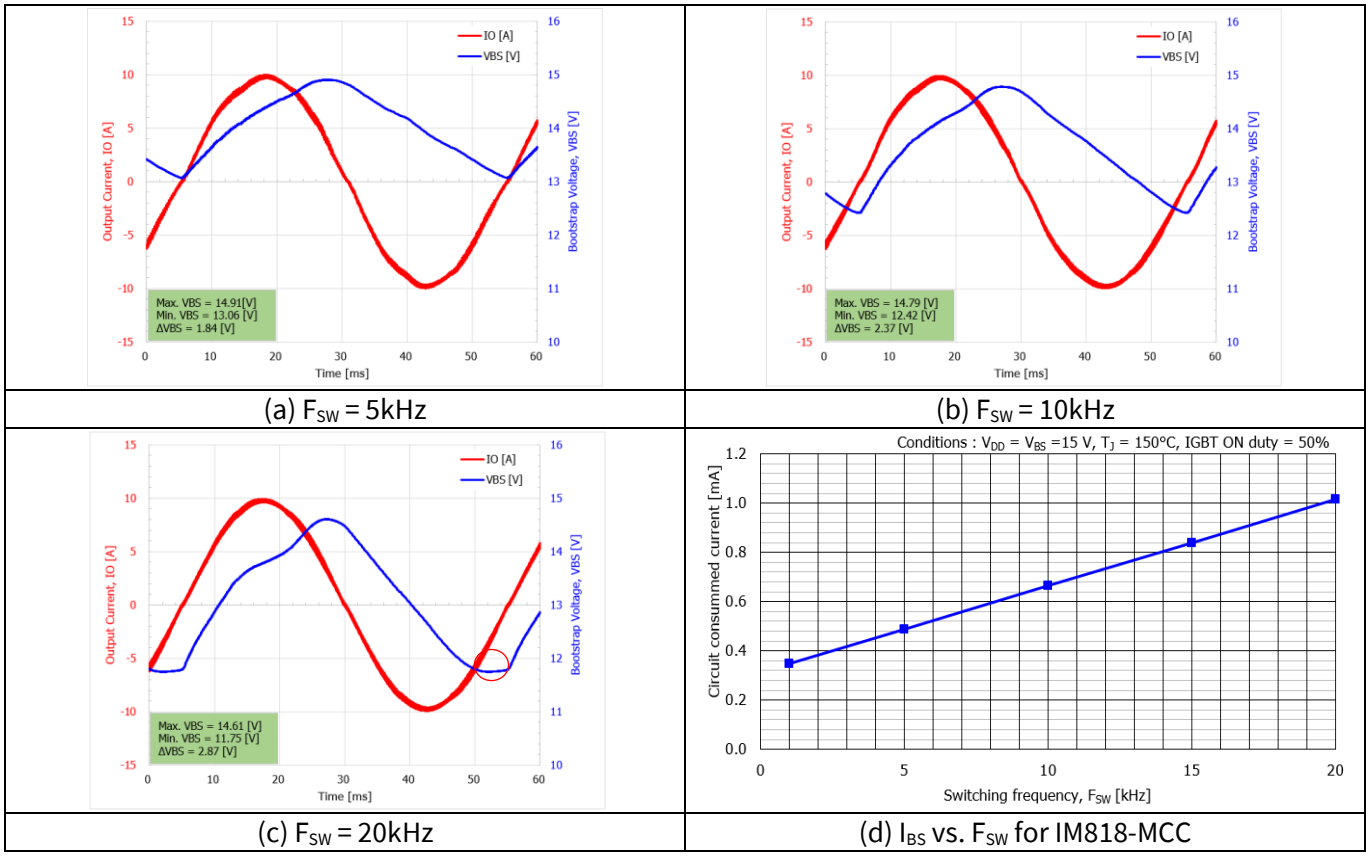
(d) F_O = 120Hz

Figure 12 Comparison of output frequency

(2) Comparison of switching frequency, F_{SW} : 5 / 10 / 20 kHz

The results of the simulation with three switching-frequency conditions are shown in Figure 13 (a), (b), and (c). When the switching frequency (F_{SW}) is increased, the amount of gate charge (circuit current of GD IC) increases by switching frequency accordingly as Figure 13 (d).

Therefore, the amount of discharge by the gate charge increase exceeds the amount of charge. Therefore ΔV_{BS} increases depending on the switching frequency. So usually the capacitance of C_{BS} needs to increase when you want to use higher switching-frequency conditions.



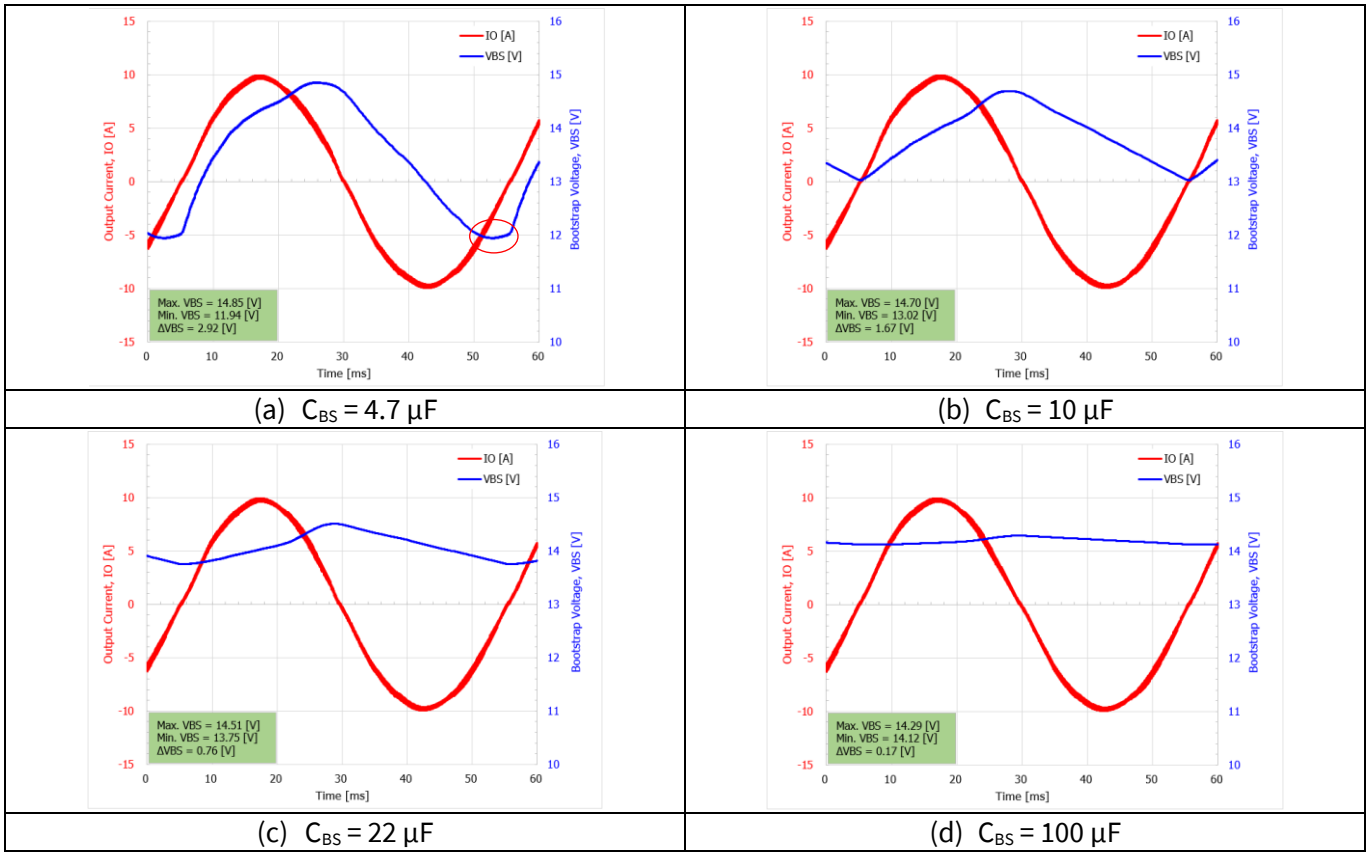
(a) F_{SW} = 5kHz | (b) F_{SW} = 10kHz

(c) F_{SW} = 20kHz | (d) I_{BS} vs. F_{SW} for IM818-MCC

Figure 13 Comparison of switching frequency and bootstrap circuit consumed current (I_{BS}) vs. switching frequency (F_{SW}) for IM818-MCC

(3) Comparison of bootstrap capacitance, C_{BS} : 4.7 / 10 / 22 / 100 µF

The results of simulation with four conditions of capacitance of C_{BS} are shown in Figure 14. When the capacitance C_{BS} is quite small such as in Figure 14 (a), the voltage drop of V_{BS} increases significantly. Then the minimum V_{BS} falls extremely low and the V_{BS} ripple voltage (ΔV_{BS}) rises. The increment of ΔV_{BS} can affect the reduction of bootstrap capacitor lifetime. Therefore, the recommended value of ΔV_{BS} for CIPOS™ IPM is within 1.0 Vp-p.



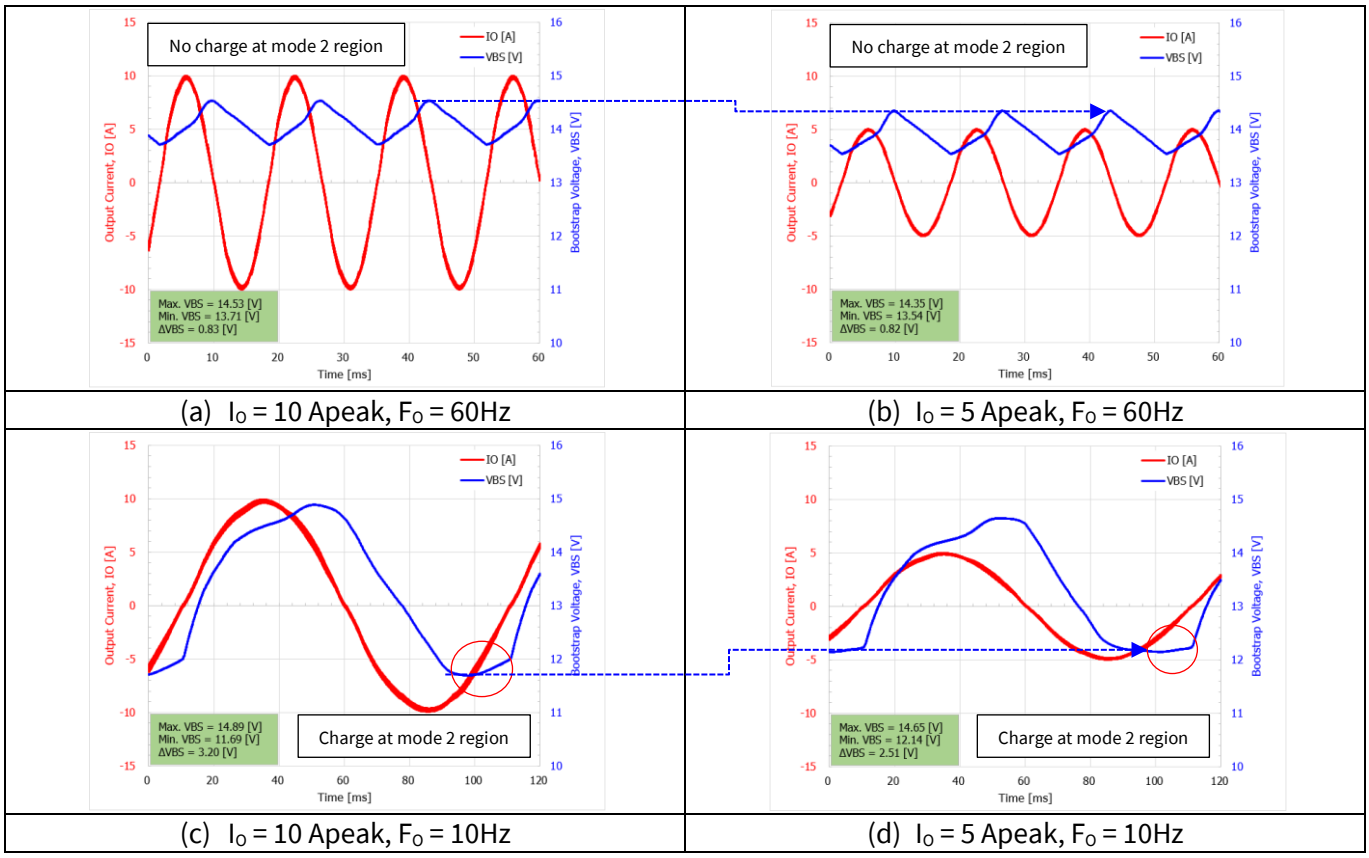
(a) C_{BS} = 4.7 µF | (b) C_{BS} = 10 µF

(c) C_{BS} = 22 µF | (d) C_{BS} = 100 µF

Figure 14 Comparison of capacitance of C_{BS}

(4) Comparison output current, I_O : 5 / 10 Apeak at F_O = 10 / 60Hz

The results of simulation with four conditions of output current are shown in Figure 15. As mentioned in section 1.2, the charge-starting voltage is affected by output current. As shown in Figure 10, when the output current gets low, the charge-starting voltage decreases in Mode 1 (positive output current area) and increases in Mode 2 (negative output current area). So the maximum / minimum value of V_{BS} changes accordingly. As shown in Figure 15 (a) and (b), the maximum V_{BS} decreases at a lower output current condition. Also, as shown in Figure 15 (c) and (d), on which there is charging at Mode 2, minimum V_{BS} will rise, since the charge-starting voltage rises, and charging becomes easily.



(a) I_O = 10 Apeak, F_O = 60Hz

(b) I_O = 5 Apeak, F_O = 60Hz

(c) I_O = 10 Apeak, F_O = 10Hz

(d) I_O = 5 Apeak, F_O = 10Hz

Figure 15 Comparison of output current

According to simulation results above (1) ~ (4), with the exception of capacitance of bootstrap capacitor (C_{BS}), we can consider that the operating conditions mostly affected by bootstrap voltage (V_{BS}) are

- Output current frequency, F_O
- Switching frequency, F_{SW}

Note that these results are only provided as examples. It is necessary to consider further evaluations and confirmation at the system-design stage. Becase bootstrap voltage is also affected by other operating conditions, such as PWM (e.g. discontinuous PWM), power factor, modulation index, power device (IGBT and MOSFET).

And above all, simulations are performed at a control supply voltage of V_{DD} = 15 V. If V_{DD} is reduced to 14 V, it can lead to a drop of 1 V on all above results of V_{BS} directly. So, the variation of V_{DD} must also be considered.

1.2.3 Selection of bootstrap capacitance of C_{BS}

The charging state of C_{BS} changes due to continuously changing operating conditions. Therefore, it is not easy to estimate the exact value of bootstrap voltage (V_{BS}). But the ripple voltage of V_{BS} (ΔV_{BS}) can be roughly estimated under the conditions without charging in Mode 2, as the bootstrap capacitor charging current (I_{BS}) is almost zero in Mode 2. In this section, the estimation method of ΔV_{BS} under the given conditions is explained in Figure 16.

- Conditions : V_{DC} = 600 V, V_{DD} = 15 V, F_{SW} = 10 kHz, I_O = 10 A, F_O = 60 Hz, C_{BS} = 4.7 µF, 3-phase SVPWM, IM818-MCC

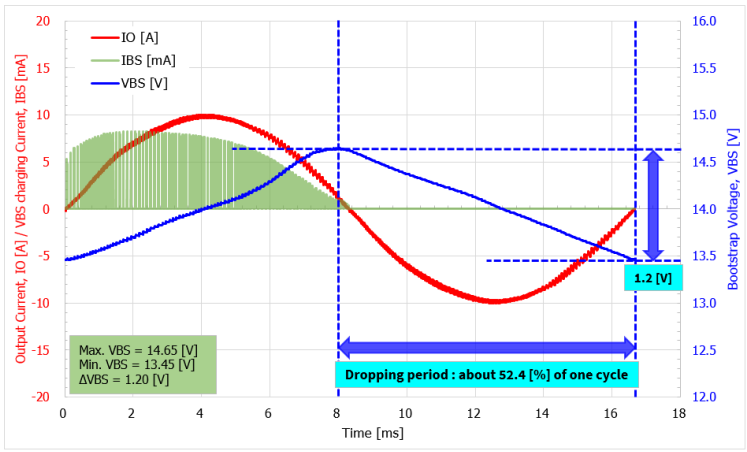


Figure 16 Charging waveform (based on simulation)

The waveform on the conditions is shown in Figure 16. As mentioned above, the charge of C_{BS} is performed during the period of positive current. Its voltage drop time is about 52.4 [%] of the output current cycle. The voltage drop for this period equals the ripple voltage at this condition. The ΔV_{BS} can be estimated as the amount of discharge of C_{BS} for the dropping time and capacitance of C_{BS}.

- ΔV_{BS} = Amount of discharge of C_{BS} for the dropping period ÷ capacitance of C_{BS}

Amound of discharge of C_{BS} is calculated as below

- Amount of discharge of C_{BS} = consumed current of GD IC × output current cycle × dropping time ratio

The consumed current of GD IC can be obtained from the graph of bootstrap circuit consumed current (I_{BS}) vs. switching frequency (F_{SW}) as shown in Figure 13 (d). So the ΔV_{BS} under given conditions can be estimated roughly as:

- ΔV_{BS} = (0.66 [mA] X 16.67 [ms] X 52.4 [%]) ÷ 4.7 [µF] = 1.23 [V]

The recommended value of ΔV_{BS} is within 1.0 Vp-p for CIPOS™ IPM. When designing capacitance of C_{BS}, it is necessary to consider various conditions such as operating conditions, tolerance of capacitance, and temperature characteristics of capacitance, DC bias and life time, and the tolerance of bootstrap circuit current of GD IC. Also the minimum voltage of V_{BS} during operation should remain above 12.5 V. For example, 3 ~ 4 times capacitance is recommended, which makes a 1.0 V voltage drop under typical conditions. In the above case, when type 5.6 µF capacitor is used, its typical ΔV_{BS} is approximately 1.0 V. So a value above 16 ~ 22 µF, which is 3 ~ 4 times the 5.6 µF, is the target value.

This estimation method is only an example under given conditions. If conditions are changed, the dropping period (52.4%) can be changed. Also, capacitance might have to be increased due to the characteristics of C_{BS} in Table 3. Therefore, sufficient evaluation in the real system is needed.

1.2.3.1 Characteristics of bootstrap capacitor, C_{BS}

Electrolytic capacitors are used for C_{BS} generally. And recently MLCC (multilayer ceramic capacitors) with large capacitance are also applied. But, the DC bias characteristics of the MLCC when applying DC voltage are considerably different from those of the electrolytic capacitor, especially the large capacitance type. Some differences in capacitance characteristics between electrolytic and ceramic capacitors are listed in Table 3.

Table 3 Difference of capacitance characteristics between electrolytic and ceramic capacitors

	Electrolytic capacitor	MLCC
Temperature characteristics (T_A : -20 ~ 85°C)	- Aluminum type: Low temp. : -10%, High temp.: +10% - Conductive polymer aluminum solide type: Low temp.: -5%, High temp.: +10%	- Difference due to temp. characteristics: Low temp. : -5% ~ 0% High temp. : -5% ~ -10% (with X5R, X7R)
DC bias characteristics (applying DC 15 V)	Nothing within rating voltage	Difference due to temp. characteristics, rating voltage, package size and so on -50% ~ -15% (with X7R, 50 VDC rating)

1.2.4 Effect of charging by other modulation schemes

1.2.4.1 Circuit current of gate driver IC

High-side, gate driver-IC circuit current that applies the bootstrap circuit varies according to the control method. The above Figure 13 (d) described the circuit current in the case of 3-phase SVPWM (continuous switching). In this section, the approximation method of the gate driver (GD) IC circuit current in the case of 60° discontinuous PWM and 120° discontinuous PWM is explained.

Bootstrap circuit current I_{BS} vs. switching frequency characteristics for IM818-MCC (typical data), which are described in Figure 17, are re-described in Figure 13 (d).

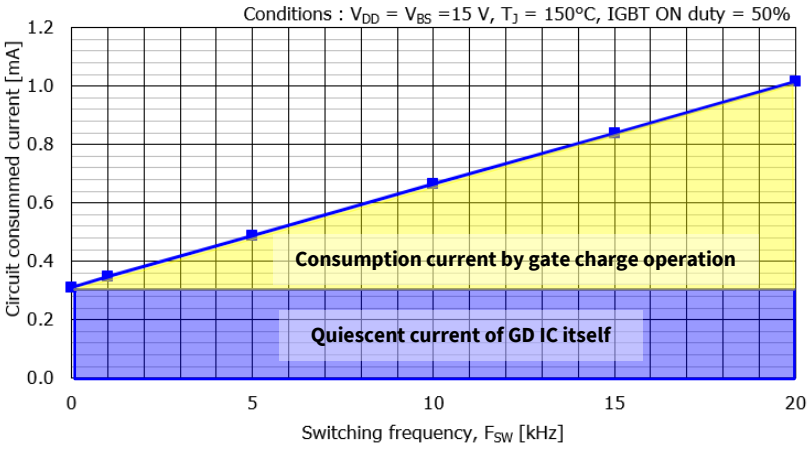


Figure 17 Bootstrap-circuit consumed current (I_{BS}) vs. switching frequency (F_{SW}) for IM818-MCC

The total GD IC circuit current at each frequency consists of the quiescent current and the current by gate charge operation. GD IC circuit current at 0Hz is the quiescent current, which is consumed by GD IC itself regardless whether it is with or without switching. When the value exceeds 0 Hz, the sum of the quiescent current at 0 Hz and the consumption current caused by the gate charge operation during switching becomes the total GD IC circuit current.

To estimate the circuit current in the case of discontinuous PWM, all modulation schemes are explained as follows:

- SVPWM: 3-phase space vector pulse-width modulation (continuous switching)
- 60° DPWM: discontinuous PWM with 60° continuous conduction periods in phase with the peak of the phase voltage
- 120° DPWM(LS): discontinuous PWM with 120° continuous conduction of each low-side switch

And, the difference between SVPWM and and two discontinuous PWM schemes is shown in Figure 18.

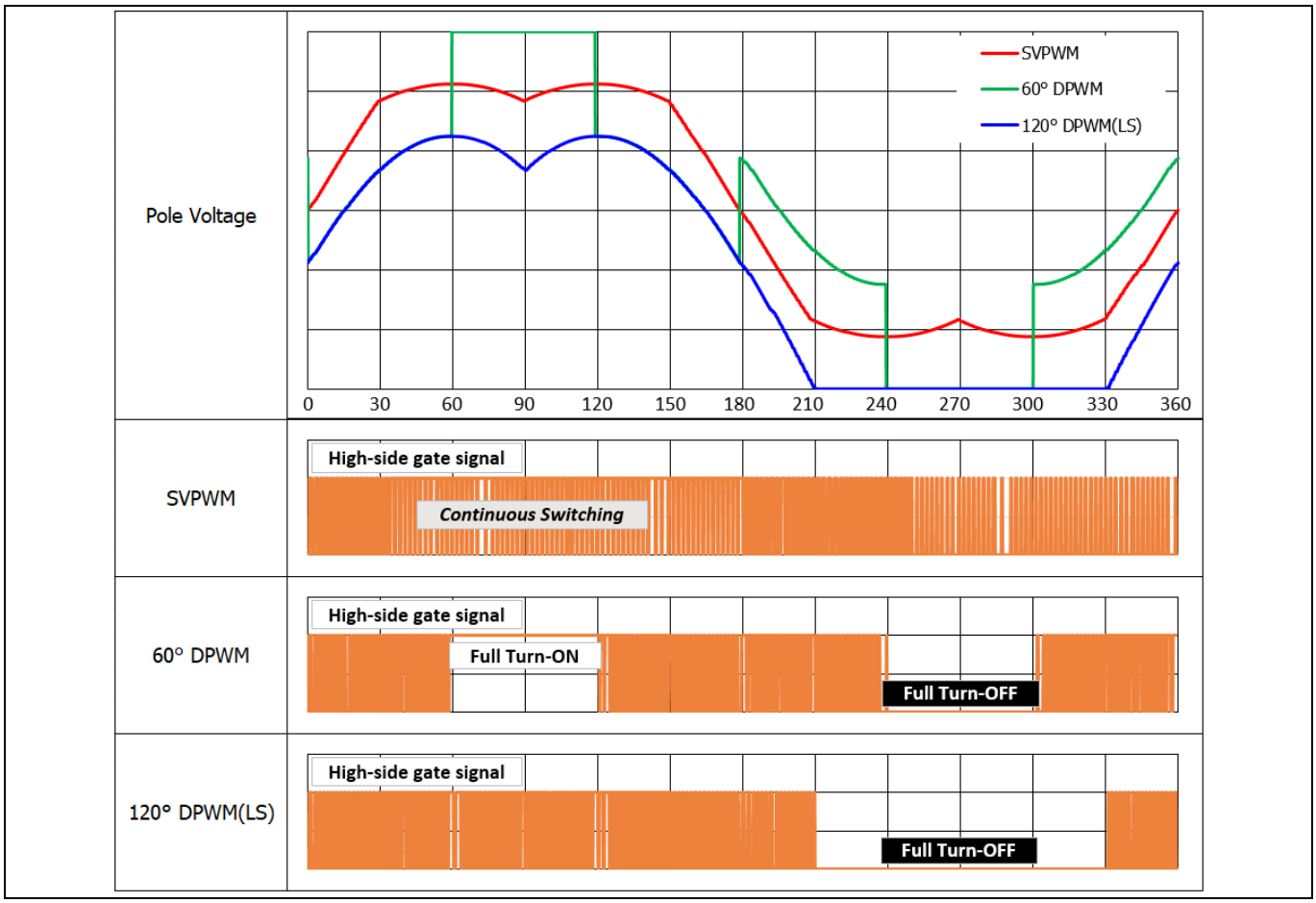


Figure 18 Difference in switching state by PWM scheme

As shown in Figure 18, the difference in GD IC circuit current between these three methods equals the difference in switching times. Switching times in the case of 60° DPWM becomes two-thirds that of SVPWM, and switching times at 120° DPWM becomes one-third at SVPWM. So each GD IC circuit current is the sum of steady consumption current and two-thirds or one-third of the switching current, respectively, as seen in Figure 17. The calculated results of the GD IC circuit currents at each modulation scheme are shown in Figure 19.

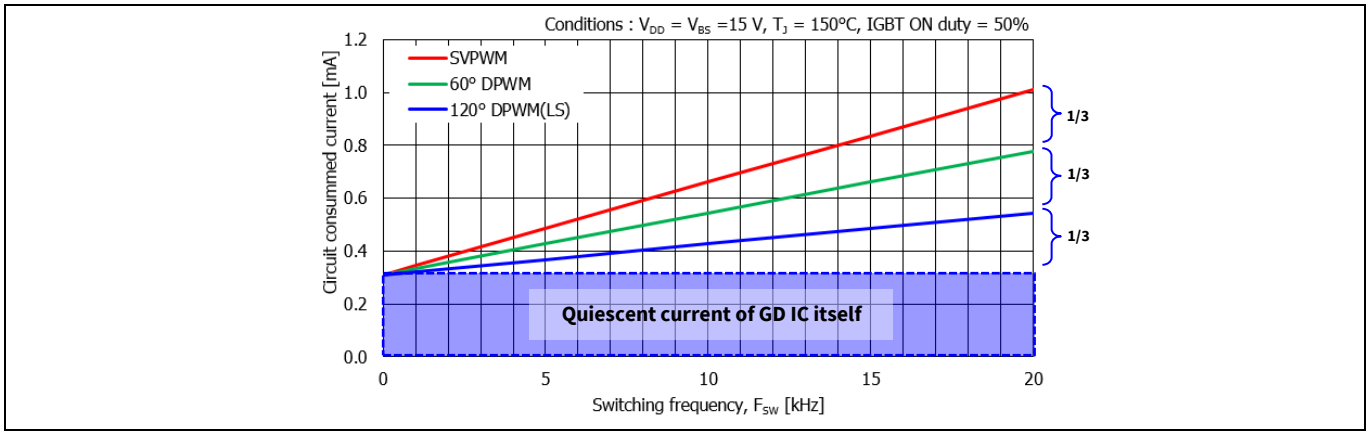
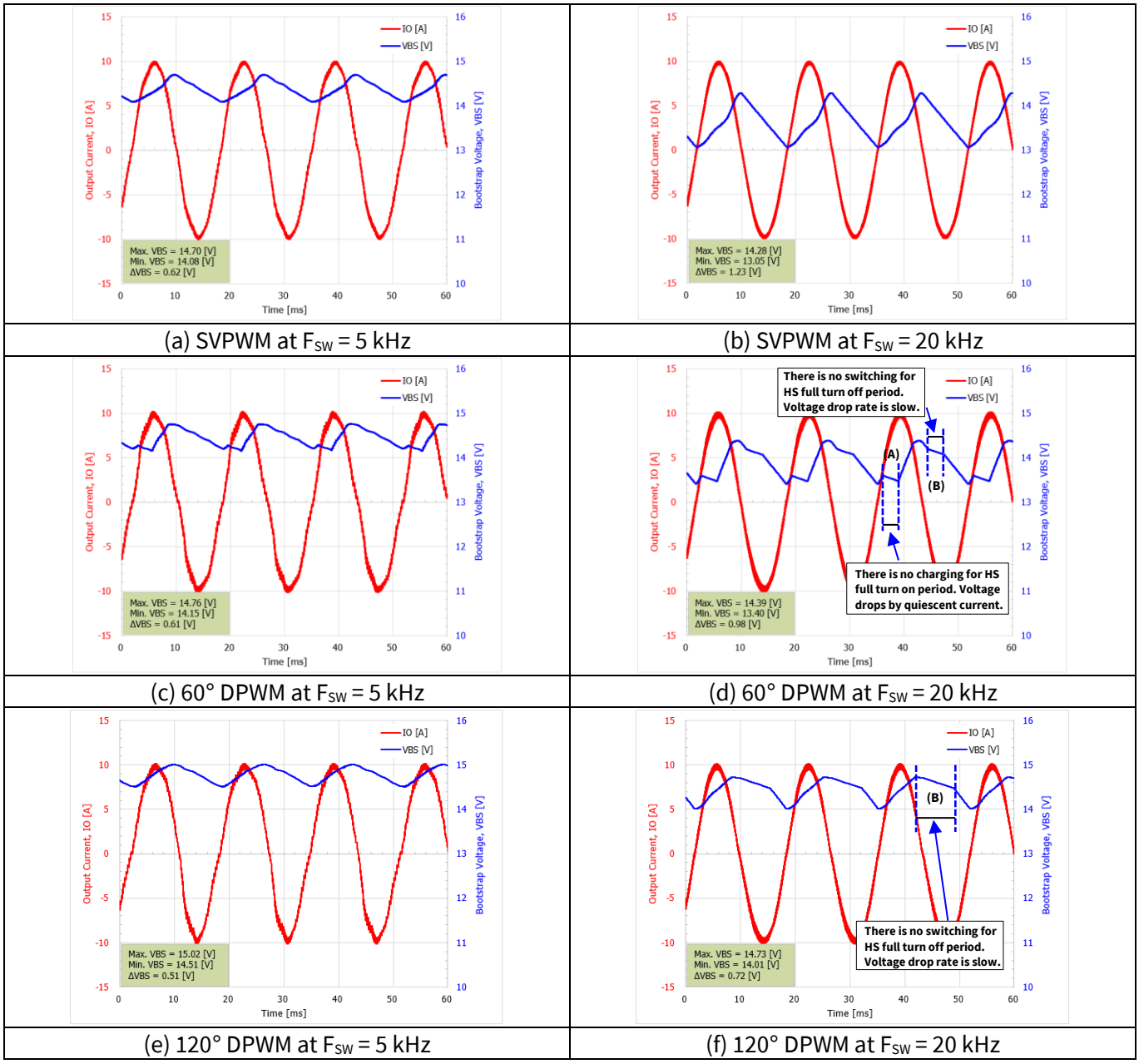


Figure 19 GD IC circuit current (I_{BS}) vs. switching frequency characteristics by modulation scheme

Example of simulation results of charging state at SVPWM and two discontinuous modulation schemes are described in Figure 20.

- Conditions : CIPOS™ Maxi IM818-MCC (1200 V / 10 A), F_{SW} = 5 / 20 kHz, F_O = 60 Hz, C_{BS} = 6.8 µF, power factor = 0.8, modulation index = 0.8, V_{DC} = 600 V, V_{DD} = 15 V, R_{shunt} = 20 mΩ



(a) SVPWM at F_{SW} = 5 kHz | (b) SVPWM at F_{SW} = 20 kHz

(c) 60° DPWM at F_{SW} = 5 kHz | (d) 60° DPWM at F_{SW} = 20 kHz

(e) 120° DPWM at F_{SW} = 5 kHz | (f) 120° DPWM at F_{SW} = 20 kHz

Figure 20 Bootstrap voltage charging state according to modulation scheme

In the case of 60° DPWM (Figure 20 (d)), during the full turn-off period (B), the voltage drop rate gets smaller because gate charging is not performed, and the voltage drops by quiescent current. On the other hand, bootstrap voltage (V_{BS}) charging is not performed during the full turn-on period (A) in the positive current region, in which charging normally has a good performance; the charging efficiency is worse. But in these results, since total GD IC circuit current in the case of 60° DPWM was smaller than at SVPWM, the minimum / maximum V_{BS} and ΔV_{BS} improved somewhat.

In the case of 120° DPWM (Figure 20 (f)), during full turn-off period (B), the voltage drop rate is smaller, as gate charging is not performed, and the voltage drops due to quiescent current. So, in these simulation conditions, V_{BS} charging efficiency of 120° DPWM is an improvement in comparison to the other schemes.

2 Reference

[1] AN2020-41_CIPOS™ MAXI IPM IM828 series application note, Infineon Technologies

[2] AN2019-16_CIPOS MAXI IPM IM818 series application note, Infineon Technologies

[3] IM818-MCC and IM828-XCC datasheet, Infineon Technologies

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