D2668

Stereo 2.6W Audio Power Amplifier With DC_Volume Control

General Description


ESOP16

D2668 is a monolithic integrated circuit, which provides precise DC volume control, and a stereo bridged audio power amplifiers capable of producing2.6W (1.8W) into 4Ω with less than 10% (1.0%)THD+N. The attenuator range of the volume control in D2668 is from 20dB (DC_Vol=0V) to -80dB (DC_Vol=3.54V) with 32 steps. The advantage of internal gain setting can be less components and PCB area. Both of the depop circuitry and the thermal shutdown protection circuitry are integrated in D2668, that reduce pops and clicks noise during power up or shutdown mode operation. It also improves the power off pop noise and protects the chip from being destroyed by over temperature and short current failure. To simplify the audio system design, D2668 combines a stereo bridge-tied loads (BTL) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip, where both modes are easily switched by the SE/BTL input control pin signal.

The D2668 is available in ESOP16 package.

Features

- Low Operating Current with 9mA
- Improved Depop Circuitry to Eliminate Turn-on and Turn-off Transients in Outputs
- High PSRR
- 32 Steps Volume Adjustable by DC Voltage with Hysteresis
- 2.6W per Channel Output Power into 4Ω Load at 5V,BTL Mode
- Two Output Modes Allowable with BTL and SE Modes Selected by SE/BTL pin
- Low Current Consumption in Shutdown Mode(1μA)
- Short Circuit Protection
- Thermal shutdown protection and over current protection circuitry
- Maximum Output Swing Clamping Function
- Lead Free Available (RoHS Compliant)

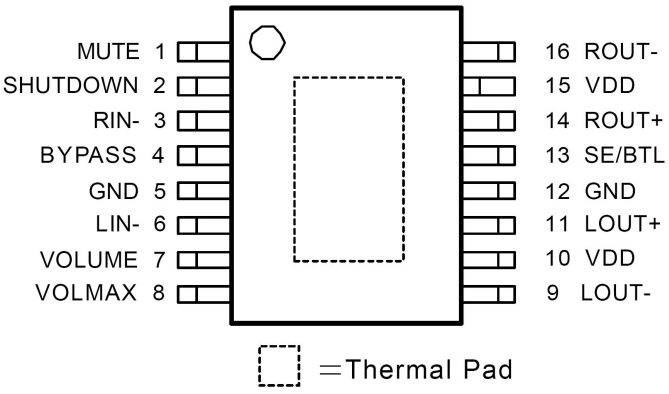
Package Information

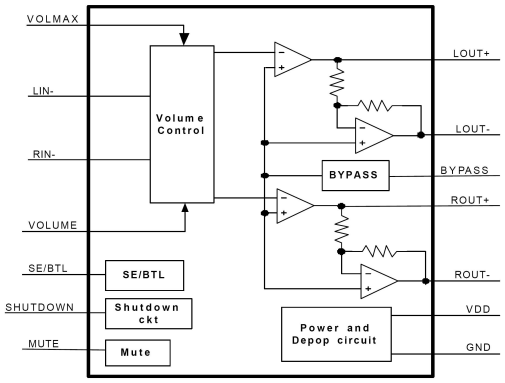
PART NO.	PACKAG DESCRIPTION	PACKAGE MARKING	PACKAGE OPTION
D2668	ESOP16	CHMC D2668 SXXXX	50/Tube 4000/Reel

CHMC:Trademark D2668:Part NO. SXXXX:Lot NO.

Block Diagram and Pin Configuration

BLOCK DIAGRAM





D2668(ESOP16)

PIN DESCRIPTION

No.	Name	Config	Descriptionsa
1	MUTE	I	Mute control signal input,hold low for normal operation,hold high to mute
2	SHUTDOWN	I	It will be into shutdown mode when pull low.I_{SD}=1μA
3	RIN-	I	Right channel input terminal
4	BYPASS	I	Bias voltage generator
5,12	GND		Ground connection,Connected to thermal pad.
6	LIN-	I	Left channel input terminal
7	VOLUME	I	Input signal for internal volume gain setting
8	VOLMAX	I	Setting the maximum output swing.Input a non-zero voltage(Vc)to this pin,the output voltage swing will be clamped between V_{OH}(the maximum positive value) –Vc&V_{OL}(minimum negative value)+Vc.Disable this function when tie this pin to GND.Maximum input voltage≤1/2VDD
9	LOUT-	O	Left channel postive output in BTL mode and SE mode
10,15	VDD		Supply voltage
11	LOUT+	O	Left channel negative output in BTL mode and high impedance in SE mode
13	SE/BTL	I	Output mode control input,high or SE output mode and low for BTL mode
14	ROUT+	O	Right channel negative output in BTL mode and high impedance in SE mode
16	ROUT-	O	Right channel positive output in BTL mode and SE mode

ABSOLUTE MAXIMUM RATING

(Over operating free-air temperature range unless otherwise noted.)

Characteristics	Symbol	Value	Unit
supply voltage range	V_{DD}	-0.3～6	V
Input voltage range, SE/BTL,SHUTDOWN,Mute	V_{IN}	-0.3～V_{DD}+0.3	V
Operating ambient temperature range	Ta	-40 ～ +85	℃
Maximum junction temperature	Tj	Internal limited	℃
Storage temperature range	Tstg	-65 ～ +150	℃
Soldering temperature,10seconds	Ts	260	℃
Electrostatic discharge	V_{ESD}	-3000～3000 *2 -200～200 *3	V
Power dissipation	P_D	Internal limited	

*1.D2668 integrated internal thermal shutdown protection when junction temperature ramp up to 150°C

*2.Human body model: C=100pF, R=1500Ω, 3 positives pulse plus 3 negative pulses

*3.Machine model: C=200pF, L=0.5μF, 3 positive pulses plus 3 negative pulses

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Test Conditions	Min.	Max.	Unit
Supply voltage	V_{DD}		4.5	5.5	V
High level threshold voltage	V_{IH}	SHUTDOWN,Mute	2		V
		SE/BTL	4		
Low level threshold voltage	V_{IL}	SHUTDOWN,Mute		1.0	V
		SE/BTL		3	
Common mode input voltage	V_{ICM}		V_{DD}-1.0		V

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal resistance from junction to ambient in free air	R_{THJA}	45	℃/W

ELECTRICAL CHARACTERISTICS

（Unless otherwise specified， V_{DD}=5V,-20℃<Ta<85℃）

Characteristics	Symbol	Test conditions	Min.	Typ.	Max	Unit
Supply voltage	V_{DD}		4.5		5.5	V
Supply current	I_{DD}	SE/BTL=0V		9	20	mA
		SE/BTL=5V		4	10	
Supply current in shutdown mode	I_{SD}	SE/BTL=0V SHUTDOWN=0V		1		μA
High input current	I_{IH}			900		nA
Low input current	I_{IL}			900		nA
Output differential voltage	V_{OS}			5		mV

*Current flowing into the IC is positive(+) and current flowing out is negative(-).

BTL mode（Unless otherwise specified， V_{DD}=5V, Ta=25℃ ,R_L=4Ω,Gain=2V/V）

Characteristics	Symbol	Test conditions	Min.	Typ.	Unit
Maximum output power	P_O	THD=10%, R_L=3Ω,Fin=1kHz		2.9	W
		THD=10%, R_L=4Ω,Fin=1kHz		2.6	
		THD=10%, R_L=8Ω,Fin=1kHz		1.6	
		THD=1%, R_L=3Ω,Fin=1kHz		2.4	
		THD=1%, R_L=4Ω,Fin=1kHz		1.8	
		THD=0.5%, R_L=8Ω, Fin=1kHz	1	1.3	
Total harmonic distortion plus noise	THD+N	Po=1.2W, R_L=4Ω,Fin=1kHz		0.07	%
		Po=0.9W, R_L=8Ω,Fin=1kHz		0.08	
Power ripple rejection ratio	PSRR	V_{IN}=0.1Vrms,R_L=8Ω C_B=1μF,Fin=120Hz		60	dB
Channel separation	Xtalk	C_B=1μF, R_L=8Ω,Fin=1kHz		90	dB
Signal to noise ratio	S/N	Po=1.1W, R_L=8Ω,A_wieght		95	dB

SE mode（Unless otherwise specified， V_{DD}=5V, Ta=25℃,Gain=1V/V）

Characteristics	Symbol	Test conditions	Min.	Typ.	Unit
Maximum output power	P_O	THD=10%, R_L=16Ω,Fin=1kHz		220	mW
		THD=10%, R_L=32Ω,Fin=1kHz		120	
		THD=1%, R_L=16Ω,Fin=1kHz		160	
		THD=1%, R_L=32Ω,Fin=1kHz		95	
Total harmonic distortion plus noise	THD+N	Po=125mW, R_L=16Ω,Fin=1kHz		0.09	%
		Po=65mW, R_L=32Ω,Fin=1kHz		0.09	
Power ripple rejection ratio	PSRR	V_{IN}=0.1Vrms,R_L=8Ω C_B=1μF,Fin=120Hz		60	dB
Channel separation	Xtalk	C_B=1μF, R_L=32Ω,Fin=1kHz		60	dB
Signal to noise ratio	S/N	Po=75mW, SE,R_L=8Ω A_wieght		100	dB

CONTROL INPUT TABLE

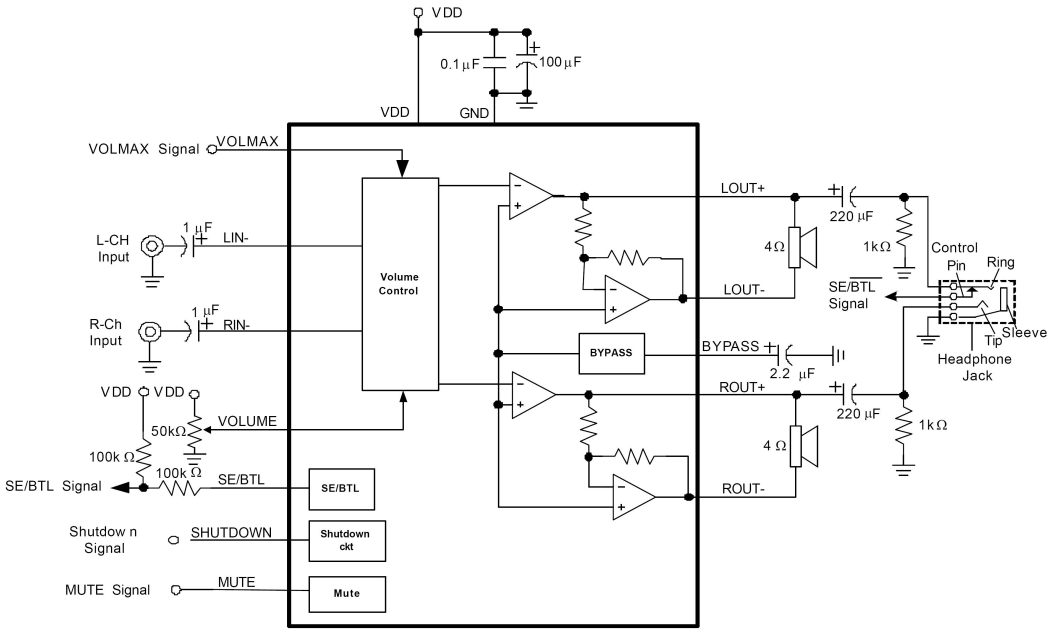
SHUTDOWN	MUTE	SE/BTL	Operating Mode
L			Shutdown mode
H	L	L	BTL out
H	L	H	SE out
H	H		Mute

VOLUME CONTROL TABLE_BTL MODE

Supply voltage VDD=5V

Gaib(dB)	High(V)	Low(V)	Hysteresis(mV)	Recommended Voltage(V)
20	0.12	0.00		0
18	0.23	0.17	52	0.20
16	0.34	0.28	51	0.31
14	0.46	0.39	50	0.43
12	0.57	0.51	49	0.54
10	0.69	0.62	47	0.65
8	0.80	0.73	46	0.77
6	0.91	0.84	45	0.88
4	1.03	0.96	44	0.99
2	1.14	1.07	43	1.10
0	1.25	1.18	41	1.22
-2	1.37	1.29	40	1.33
-4	1.48	1.41	39	1.44
-6	1.59	1.52	38	1.56
-8	1.71	1.63	37	1.67
-10	1.82	1.74	35	1.78
-12	1.93	1.85	34	1.89
-14	2.05	1.97	33	2.01
-16	2.16	2.08	32	2.12
-18	2.28	2.19	30	2.23
-20	2.39	2.30	29	2.35
-22	2.50	2.42	28	2.46
-24	2.62	2.53	27	2.57
-26	2.73	2.64	26	2.69
-28	2.84	2.75	24	2.80
-30	2.96	2.87	23	2.91
-32	3.07	2.98	22	3.02
-34	3.18	3.09	21	3.14
-36	3.30	3.20	20	3.25
-38	3.41	3.32	18	3.36
-40	3.52	3.43	17	3.48
-80	5.00	3.54	16	5

APPLICATION CIRCUIT



APPLICATION SUMMARY

BTL Operation

The D2668 output stage (power amplifier) has two pairs of operational amplifiers internally, allowed for different amplifier configurations.

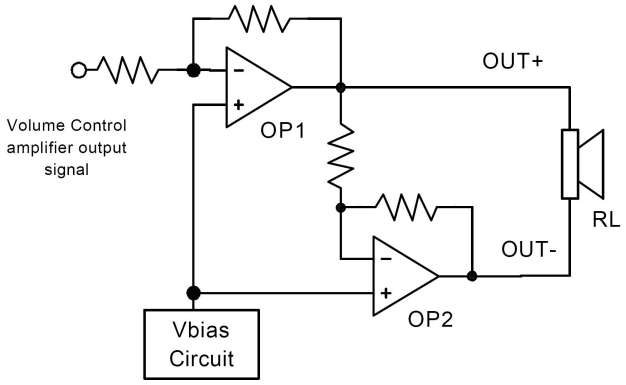


Fig.1 D2668 internal configuration(each channel)

The power amplifier's OP1 gain is setting by internal unity-gain and input audio signal is come from internal volume control amplifier, while the second amplifier OP2 is internally fixed in a unity-gain, inverting configuration. Figure 1 shows that the output of OP1 is connected to the input to OP2, which results in the output signals of with both amplifiers with identical in magnitude, but out of phase 180°. Consequently, the differential gain for each channel is 2 x (Gain of SE mode).

By driving the load differentially through outputs OUT+ and OUT-, an amplifier configuration commonly referred to as bridged mode is established. BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to ground.

A BTL amplifier design has a few distinct advantages over the SE configuration, as it provides differentialdrive to the load, thus doubling the output swing for aspecified supply voltage.

Four times the output power is possible as compared toa SE amplifier under the same conditions. A BTL configuration, such as the one used in D2668, also creates a second advantage over SE amplifiers. Since the differential outputs, ROUT+, ROUT-, LOUT+, and LOUT-, are biased at half-supply, no need DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, SE configuration.

Single-Ended Operation

Consider the single-supply SE configuration shown Application Circuit. A coupling capacitor is required to block the DC offset voltage from reaching the load. These capacitors can be quite large (approximately33μF to 1000μF) so they tend to be expensive, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system(refer to the Output Coupling Capacitor).The rules described still hold with the addition of the following relationship:

$$\frac{1}{Cbypass \times 125k\Omega} \leq \frac{1}{RiCi} << \frac{1}{R_LC_C} \qquad (1)$$

Output SE/BTL Operation

The ability of the D2668 to easily switch between BTL and SE modes is one of its most important costs saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated.

Internal to the D2668, two separate amplifiers drive OUT+ and OUT- (see Figure 1). The SE/BTL input controls the operation of the follower amplifier that drives LOUT- and ROUT-.

- When SE/BTL is held low, the OP2 is turn on and the D2668 is in the BTL mode.
- When SE/BTL is held high, the OP2 is in a high

Output SE/BTL Operation (Cont.)

Output impedance state, which configures the D2668 as SE driver from OUT+. IDD is

reduced by approximately one-half in SE mode.

Control of the SE/BTL input can be a logic-level TTL source or a resistor divider network or the stereo headphone jack with switch pin as shown in Application Circuit.

In Figure 2, input SE/BTL operates as follows : When the phonejack plug is inserted the 1kW resistor is disconnected and the SE/BTL input is pulled high and enables the SE mode. When the input goes high, the OUT- amplifier is shutdown causing the speaker to mute. The OUT+ amplifier then drives through the output capacitor (Co) into the headphone jack. When there is no headphone plugged into the system, the contact pin of the headphone jack is connnected from the signal pin, the voltage divider set up by resistors100kΩ and 1kΩ.Resistor 1kΩ then pulls low the SE/BTL pin, enabling the BTL function.

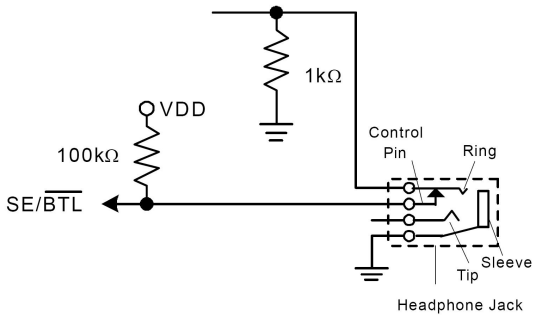


Fig.2 SE/BTL input selection by phonejack plug

Volume Control Function

D2668 has an internal stereo volume control whose setting is a function of the DC voltage applied to the VOLUME input pin. The D2668 volume control consists of 32 steps that are individually selected by a variable DC voltage level on the VOLUME control pin. The range of the steps, controlled by the DC voltage, are from 20dB to -80dB. Each gain step corresponds to a specific input voltage range, as shown in table. To minimize the effect of noise on the volume control pin, which can affect the selected gain level, hysteresis and clock delay are implemented. The amount of hysteresis corresponds to half of the step width, as shown in volume control graph.

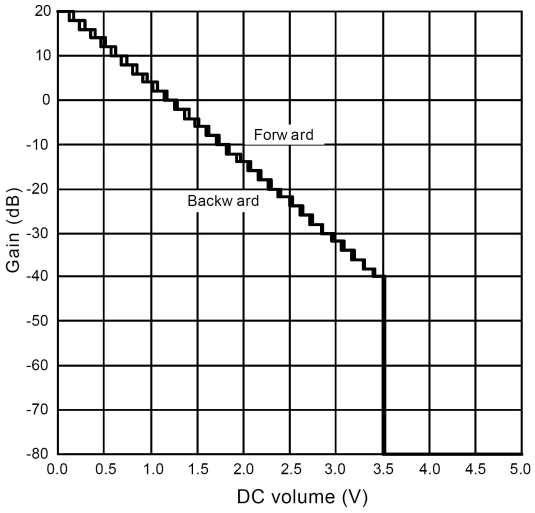


Fig.3 Gain setting vs VOLUME pin voltage

For highest accuracy, the voltage shown in the ‘recommended voltage’ column of the table is used to select a desired gain. This recommended voltage is exactly halfway between the two nearest transitions. The gain levels are 2dB/step from 20dB to -40dB in BTL mode, and the last step at -80dB as mute mode.

Input Resistance, Ri

The gain for each audio input of the D2668 is set by the internal resistors (Ri and Rf) of volume control amplifier in inverting configuration.

$$\text{SE Gain} = A_V = -\frac{R_F}{Ri} \qquad (2)$$

$$\text{BTL Gain} = -2 \times \frac{R_F}{Ri} \qquad (3)$$

BTL mode operation brings the factor of 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. For the varying gain setting, D2668 generates each input resistance on figure 4. The input resistance will affect the low frequency performance of audio signal. The minmum input resistance is 10kΩ when gain setting is 20dB and the resistance will ramp up when close loop gain below20dB. The input res istance has wide variation (+/-10%) caused by process variation.

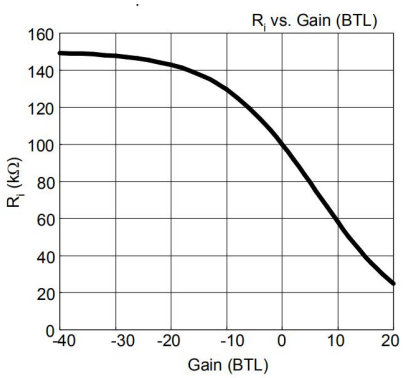


Fig.4 Input resistance vs gain setting

Input Capacitor, Ci

In the typical application an input capacitor, Ci, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, Ci and the minimum input impedance Ri (25kΩ) form a high-pass filter with the corner frequency determined in the follow equation :

$$F_C(\text{highpass}) = \frac{1}{2\pi \times 10k\Omega \times Ci} \qquad (4)$$

The value of Ci is important to consider as it directly affects the low frequency performance of the circuit. Consider the example where Ri is 25kΩ and the specification calls for a flat bass response down to100Hz. Equation is reconfigured as follow :

$$Ci = \frac{1}{2\pi \times 10k\Omega \times f_C} \qquad (5)$$

Consider to input resistance variation, the Ci is 0.16μF so one would likely choose a value in the range A further consideration for this capacitor is the leakage path from the input source through the input network(Ri+Rf, Ci) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the

capacitor should face the amplifier input in most applications as the DC level there is held at VDD/2, which is likely higher that the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor, Cbypass

As other power amplifiers, proper supply bypassing is critical for low noise performance and high power supply rejection.

The capacitors located on both the bypass and power supply pins should be as close to the device as possible. The effect of a larger bypass capacitor will improve PSRR due to increased supply stability. Typical applications employ a 5V regulator with 1.0μF and a 0.1μF bypass capacitor as supply filtering. This does not eliminate the need for bypassing the supply nodes of the D2668. The selection of bypass capacitors, especially Cbypass, is thus dependent upon desired PSRR requirements, click and pop performance. To avoid start-up pop noise occurred, the bypass voltage should rise slower than the input bias voltage and the relationship shown in equation (6) should be maintained.

$$\frac{1}{Cbypass \times 125k\Omega} << \frac{1}{100k\Omega \times Ci} \qquad (6)$$

The bypass capacitor is fed thru from a 125kΩ resistor inside the amplifier and the 100kΩ is maximum input resistance of (Ri+ Rf). Bypass capacitor, Cb, values of3.3μF to 10μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

The bypass capacitance also effects to the start up time. It is determined in the following equation :

$$Tstart\ up = 5 \times (Cbypass \times 125K\Omega) \qquad (7)$$

Output Coupling Capacitor, Cc

In the typical single-supply SE configuration, an output coupling capacitor (Cc) is required to block the DC bias at the output of the amplifier thus preventing DC currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation.

$$F_C(highpass) = \frac{1}{2\pi R_L C_C} \qquad (8)$$

For example, a 330μF capacitor with an 8Ω speaker would attenuate low frequencies below 60.6Hz. The main disadvantage, from a performance standpoint, is the load

impedance is typically small, which drives the low-frequency corner higher degrading the bass response. Large values of Cc are required to pass low frequencies into the load.

Power Supply Decoupling, Cs

The D2668 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker. The optimum decoupling is achieved by using two different type capacitors that target on different type of noise on the power supply leads.

For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance(ESR) ceramic capacitor, typically 0.1μF placed as close as possible to the device VDD lead works best. For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10μF or greater placed near the audio power amplifier is recommended.

Optimizing Depop Circuitry

Circuitry has been included in the D2668 to minimize the amount of popping noise at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate clicks and pops, all capacitors must be fully discharged before turn-on. Rapid on/off switching of the device or the shutdown function will cause the click and pop circuitry.

The value of Ci will also affect turn-on pops (Refer to Effective Bypass Capacitance). The bypass voltage ramp up should be slower than input bias voltage. Although the bypass pin current source cannot be modified, the size of Cbypass can be changed to alter the device turn-on time and the amount of clicks and pops. By increasing the value of Cbypass, turn-on pop can be reduced. However, the tradeoff for using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the size of Cbypass and the turn-on time. In a SE configuration, the output coupling capacitor, Cc, is of particular concern.

This capacitor discharges through the internal 10kΩresistors. Depending on the size of Cc, the time. constant can be relatively large. To reduce transients in SE mode, an external 1kΩresistor can be placed in parallel with the internal 10kΩ resistor. The tradeoff for using this resistor is an increase in quiescent current. In the most cases, choosing a small value of Ci in the range of 0.33μF to 1μF, Cb being equal to 4.7μF and

an external 1kΩ resistor should be placed in parallel with the internal 10kΩ resistor should produce a virtually clickless and popless turn-on.
A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. So it is advantageous to use low-gain configurations.

Shutdown Function

In order to reduce power consumption while not in use, the D2668 contains a shutdown pin to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the SHUTDOWN pin. The trigger point between a logic high and logic low level is typically 2.0V. It is best to switch between ground and the supply VDD to provide maximum device performance.
By switching the SHUTDOWN pin to low, the amplifier enters a low-current state, IDD<1μA. D2668 is in shutdown mode, except PC-BEEP detect circuit. On normal operating, SHUTDOWN pin pull to high level to keeping the IC out of the shutdown mode. The SHUTDOWN pin should be tied to a definite voltage to avoid unwanted state changes.

Mute Function

The D2668 mutes the amplifier outputs when logic high is applied to the MUTE pin. Applying logic low to the MUTE pin returns the D2668 to normal operation. Prevent unanticipated mute behavior by connecting the Mute pin to logic high or low. Do not let the Mute pin float.

Maximum Output Swing Clamping Function(VolMax)

The D2668 provide the maximum output swing clamping function to protect the speaker.

When input a non-zero voltage (Vx) to VolMax pin, the amplifier's output amplitude (Vo) is be limited at Vo = Vdd –Vx. This function can effective to limited the output power across the speaker, and avoid damaging the speaker.

The maximum setting voltage of VolMax is Vdd/2, and when this function is not used, place the VolMax connect to GND.

BTL Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load.

The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_O}{P_{SUP}} \qquad (9)$$

Where :

$$P_O = \frac{V_{ORMS} \times V_{ORMS}}{R_L} = \frac{V_P \times V_P}{2R_L}$$

$$V_{ORMS} = \frac{V_P}{\sqrt{2}} \qquad (10)$$

$$P_{SUP} = V_{DD} \times I_{DDAVG} = V_{DD} \times \frac{2V_P}{\pi R_L} \qquad (11)$$

Efficiency of a BTL configuration :

$$\frac{P_O}{P_{SUP}} = \left(\frac{V_P \times V_P}{2R_L}\right) / \left(V_{DD} \times \frac{2V_P}{\pi R_L}\right) = \frac{\pi V_P}{4V_{DD}} \qquad (12)$$

Table 1 calculates efficiencies for four different output power levels.

Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range.

Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1W audio system with 8Ω loads and a 5V supply, the maximum draw on the power supply is almost 3W.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation, VDD is in the denominator. This indicates that as VDD goes down, efficiency goes up. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

Po (W)	Efficiency (%)	I_{DD} (A)	Vpp (V)	P_D (W)
0.25	31.25	0.16	2.00	0.55
0.50	47.62	0.21	2.83	0.55
1.00	66.67	0.30	4.00	0.5
1.25	78.13	0.32	4.47	0.35

*High peak voltages cause the THD to increase.

Table 1. Efficiency Vs Output Power in 5-V/8Ω BTL Systems

Power Dissipation

Whether the power amplifier is operated in BTL or SE modes, power dissipation is a major concern. In equa tion13 states the maximum power dissipation point for a SE mode operating at a given supply voltage and driving a specified load.

$$\text{SE mode : } P_{D,MAX}=\frac{V_{DD}^2}{2\pi^2 R_L} \qquad (13)$$

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$\text{BTL mode : } P_{D,MAX}=\frac{4V_{DD}^2}{2\pi^2 R_L} \qquad (14)$$

Since the D2668 is a dual channel power amplifier, the maximum internal power dissipation is 2 times that both of equations depending on the mode of operation. Even with this substantial increase in power dissipation, the D2668 does not require extra heatsink. The power dissipation from equation14, assuming a 5V-power supply and an 8Ω load, must not be greater than the power dissipation that results from the equation15 :

$$P_{D,MAX}=\frac{T_{J,MAX}-T_A}{\theta_{JA}} \qquad (15)$$

For ESOP16 package with thermal pad, the thermal resistance (qJA) is equal to 45℃/W.

Since the maximum junction temperature ($T_{J,MAX}$) of D2668 is 150℃ and the ambient temperature (Ta) is defined by the power system design, the maximum power dissipation which the IC package is able to handle can be obtained from equation15.

Once the power dissipation is greater than the maximum limit ($P_{D,MAX}$), either the

supply voltage (VDD) must be decreased, the load impedance (R_L) must be increased or the ambient temperature should be reduced.

Thermal Pad Considerations

The thermal pad must be connected to ground. The package with thermal pad of the D2668 requires special attention on thermal design. If the thermal design issues are not properly addressed, the D2668 4Ω will go into thermal shutdown when driving a 4Ω load.

The thermal pad on the bottom of the D2668 should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 10 vias of 13 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane.

For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling will be required to keep the D2668 junction temperature below the thermal shutdown temperature (150°C). In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown.

Thermal Considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions.

To calculate maximum ambient temperatures, first consideration is that the numbers from the **Power Dissipation vs. Output Power** graphs are per channel values, so the dissipation of the IC heat needs to be doubled for two-channel operation. Given θ_{JA}, the maximum allowable junction temperature (T_{JMAX}), and the total internal dissipation (P_D), the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the D2668 is 150°C. The internal dissipation figures are taken from the **Power Dissipation vs. Output Power** graphs.

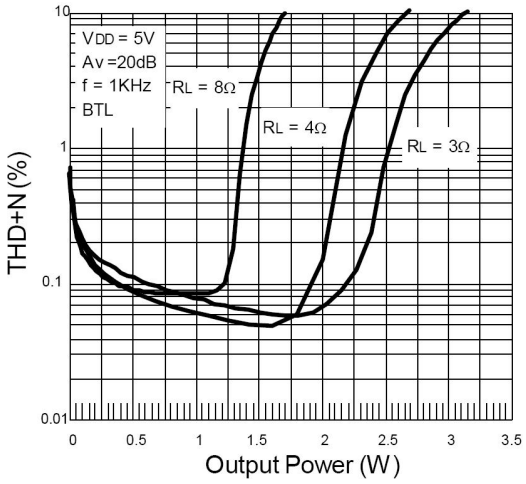
$T_{AMax} = T_{JMax} - \theta_{JA} P_D$ (16)

150 - 45(0.8*2) = 78°C

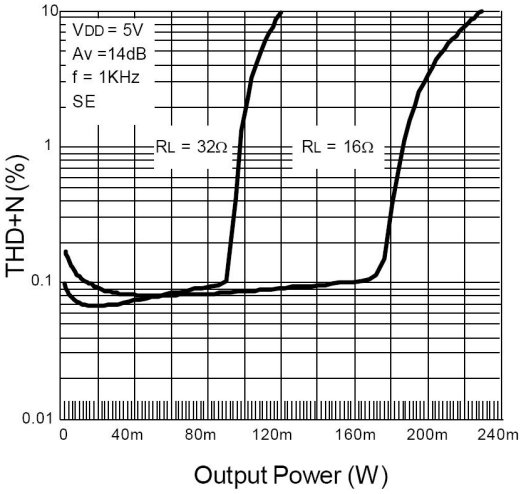
The D2668 is designed with a thermal shutdown protection that turns the device off when the junction temperature surpasses 150°C to prevent damaging the IC.

CHARACTERISTIC CURVES

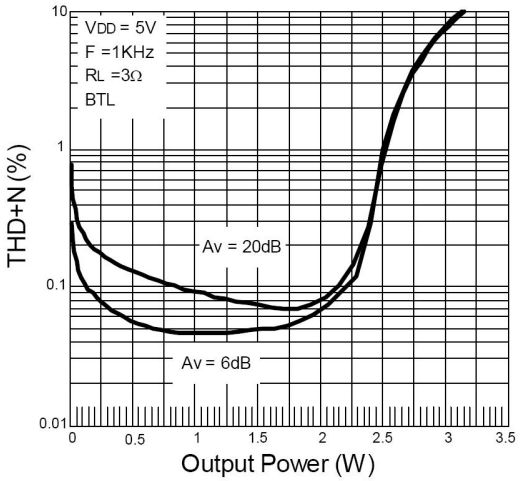
THD+N vs. Output Power



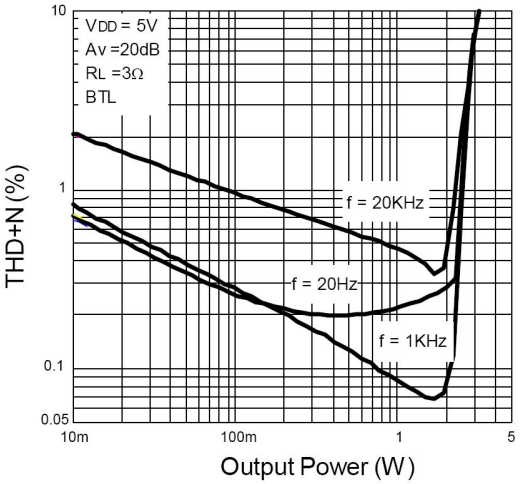
THD+N vs. Output Power



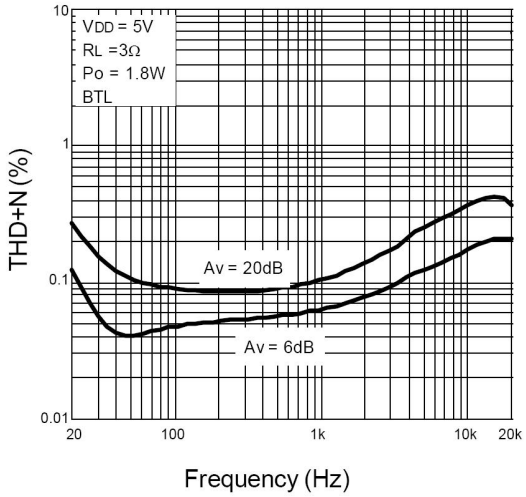
THD+N vs. Output Power



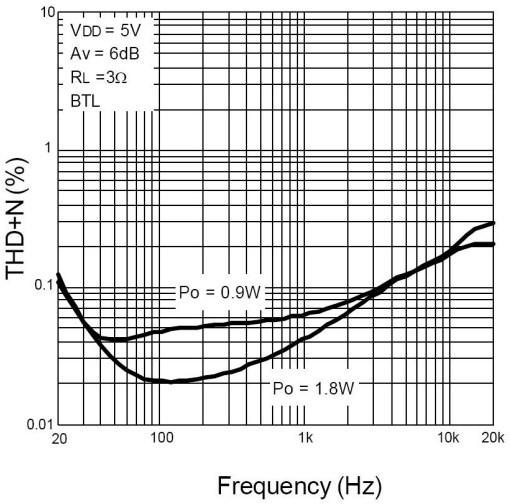
THD+N vs. Output Power



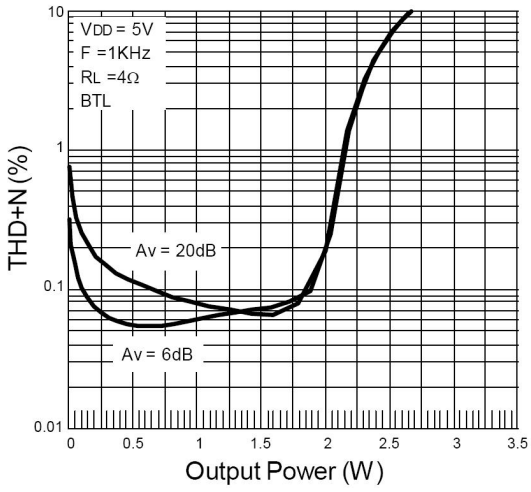
THD+N vs. Frequency



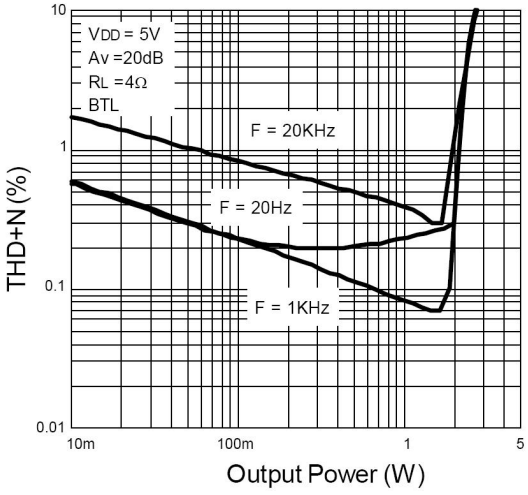
THD+N vs. Frequency



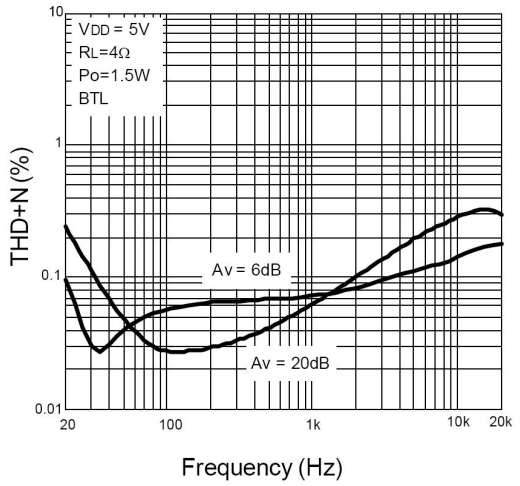
THD+N vs. Output Power



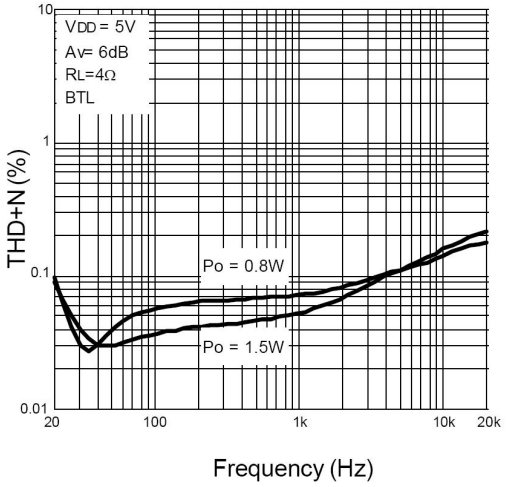
THD+N vs. Output Power



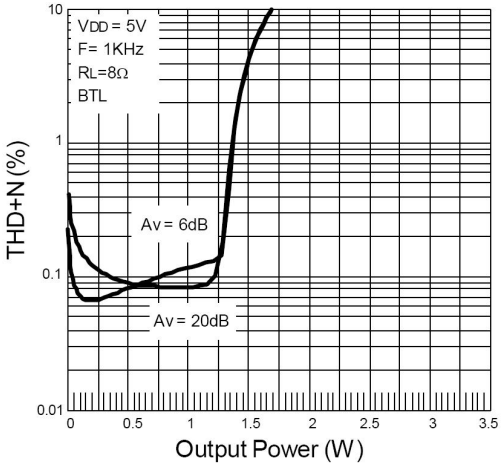
THD+N vs. Frequency



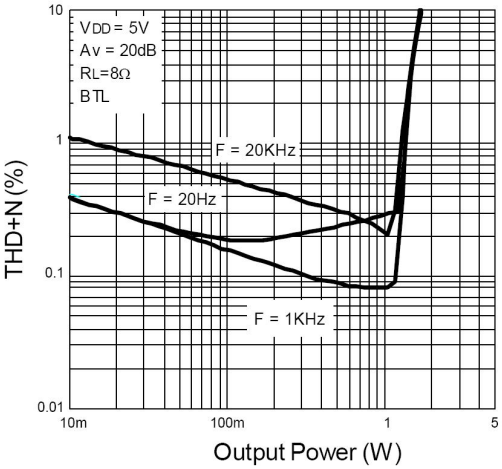
THD+N vs. Frequency



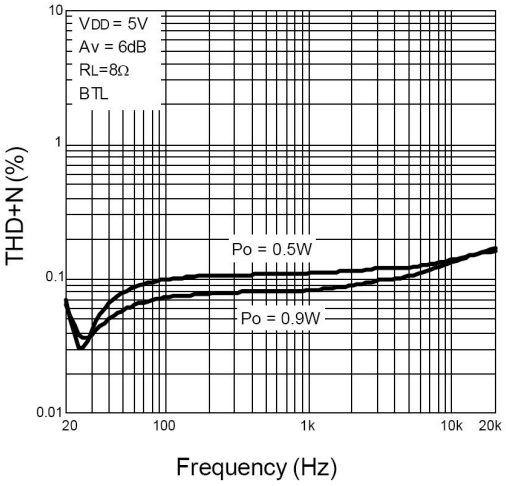
THD+N vs. Output Power



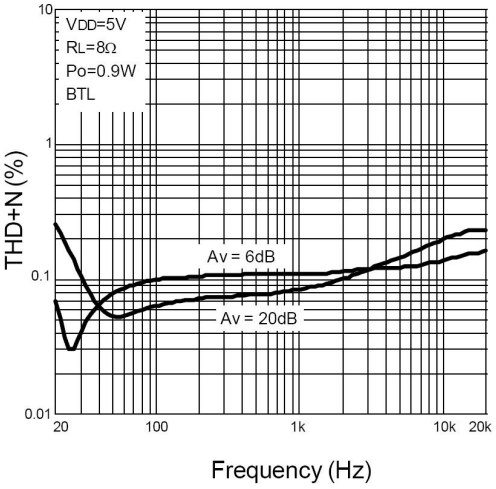
THD+N vs. Output Power



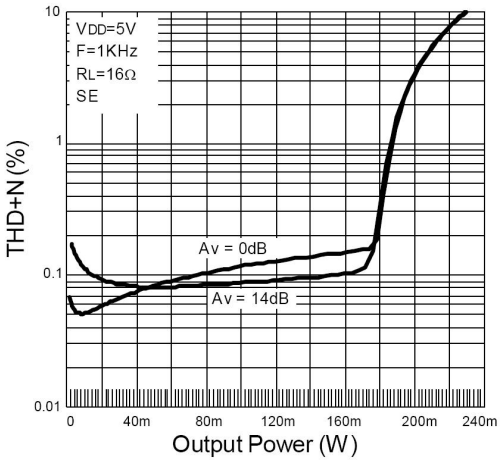
THD+N vs. Frequency



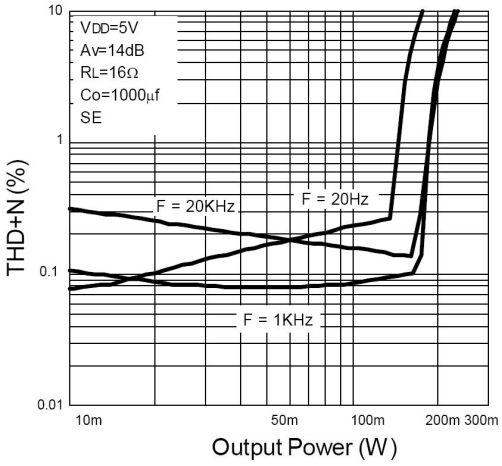
THD+N vs. Frequency



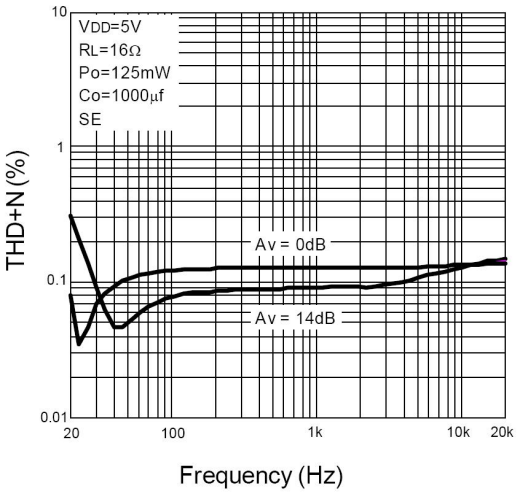
THD+N vs. Output Power



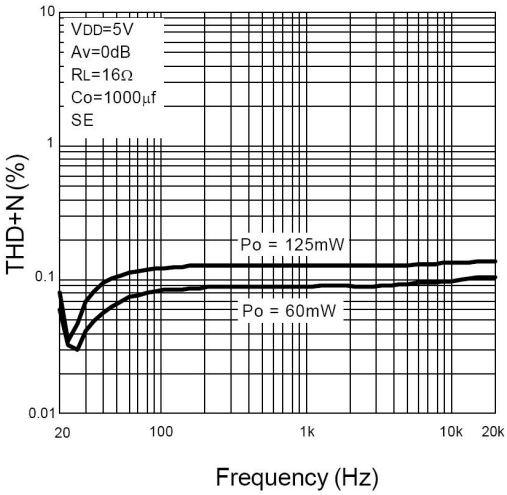
THD+N vs. Output Power



THD+N vs. Frequency



THD+N vs. Frequency



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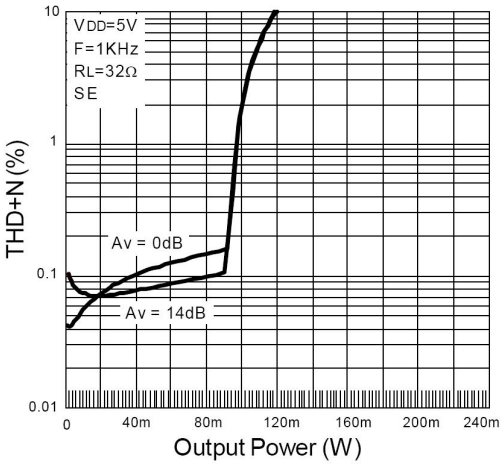
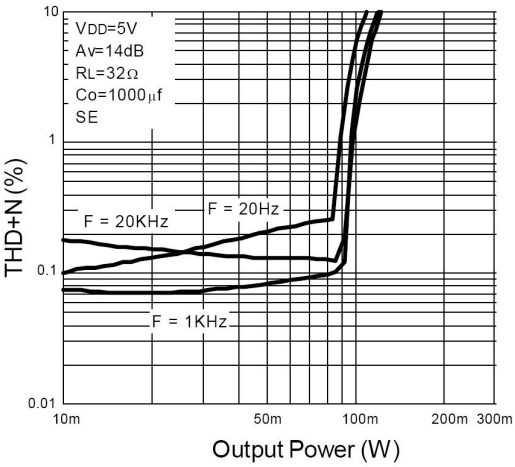
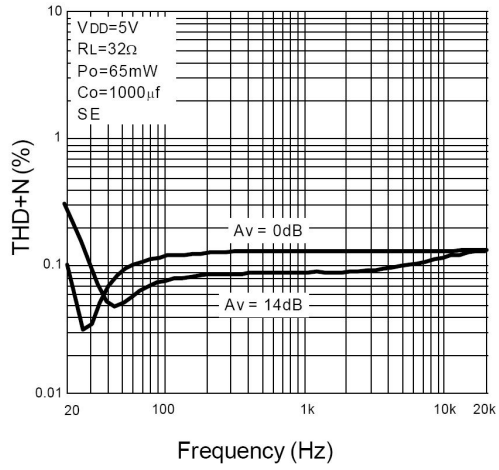


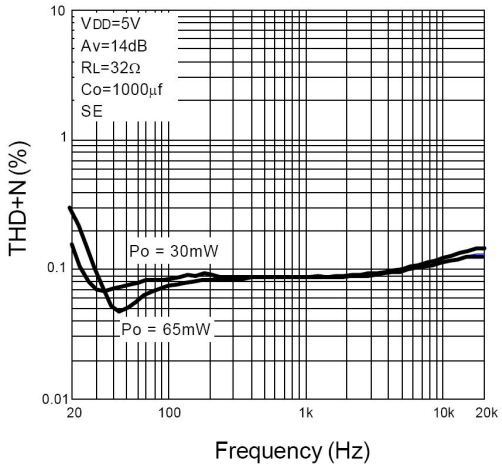
THD+N vs. Output Power



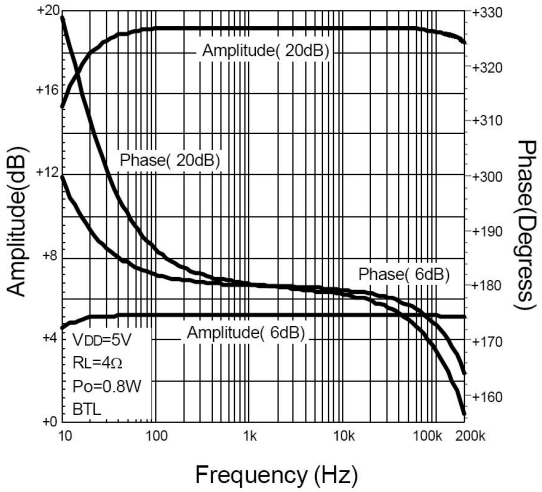
THD+N vs. Frequency



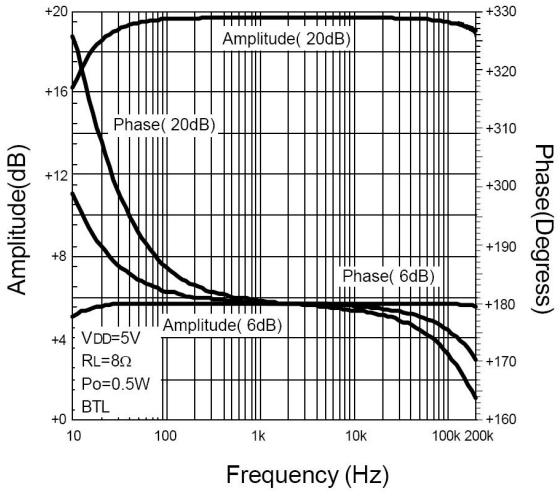
THD+N vs. Frequency



Frequency Response



Frequency Response



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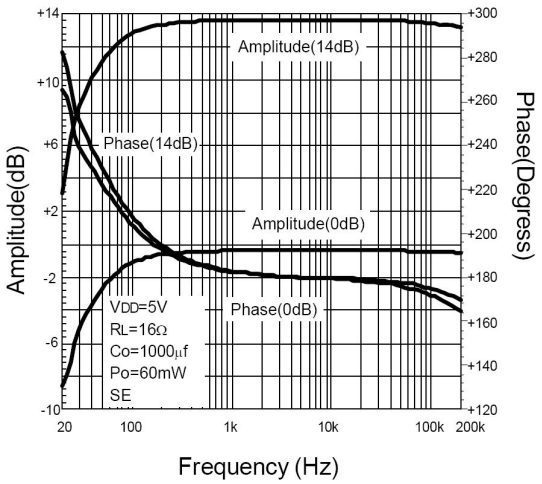

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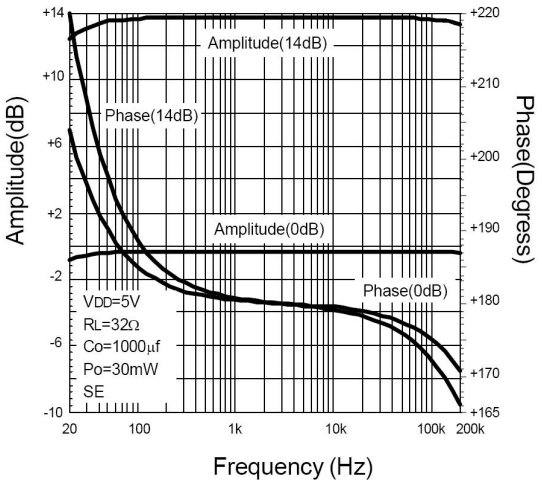
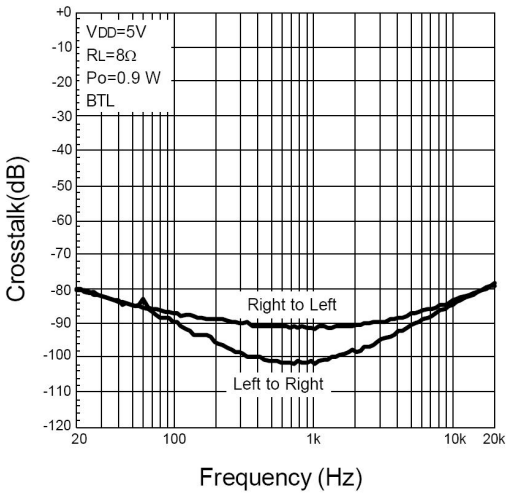
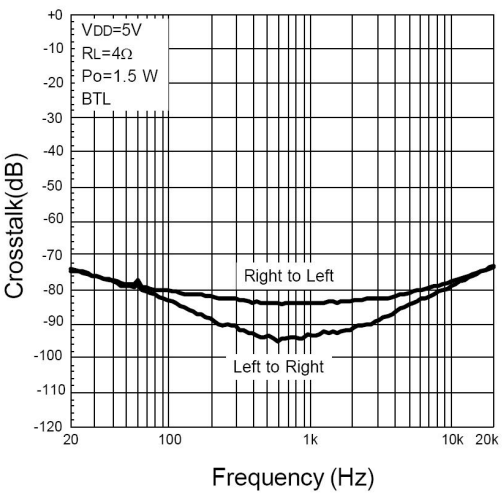


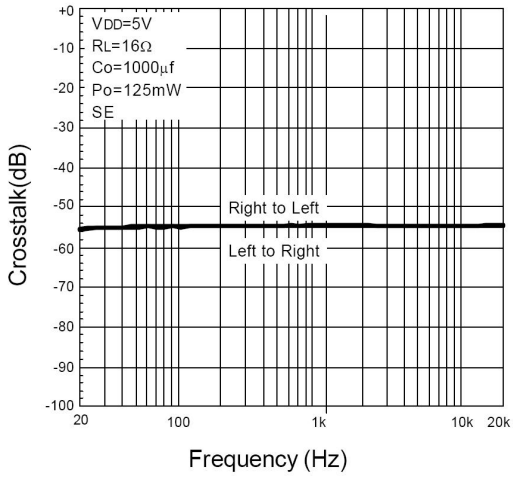
Crosstalk vs. Frequency



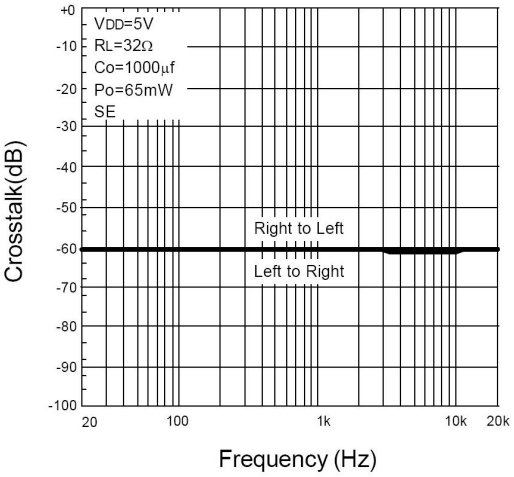
Crosstalk vs. Frequency



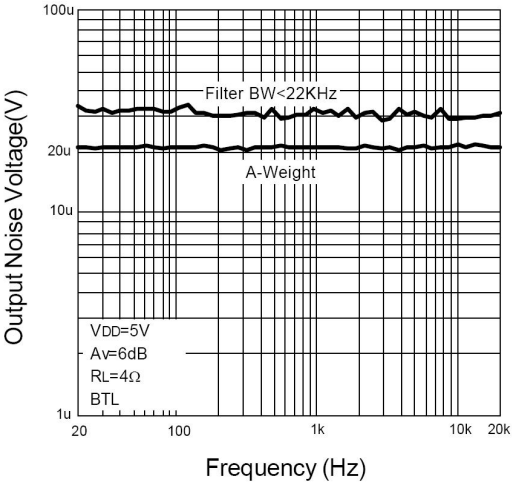
Crosstalk vs. Frequency



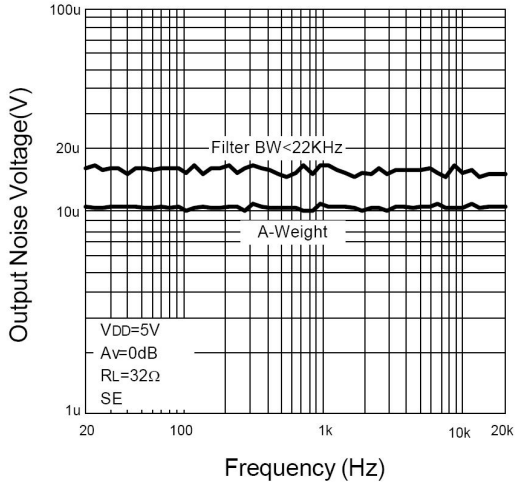
Crosstalk vs. Frequency



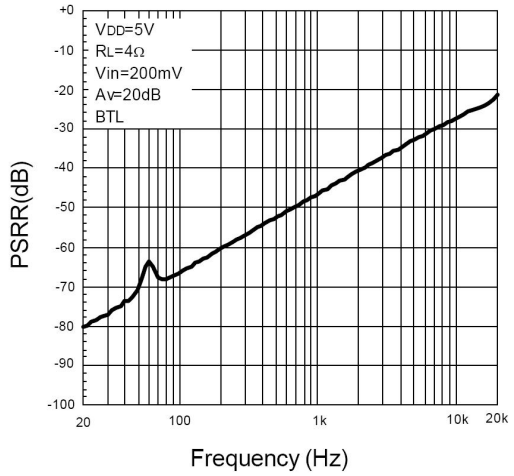
Output Noise Voltage vs. Frequency



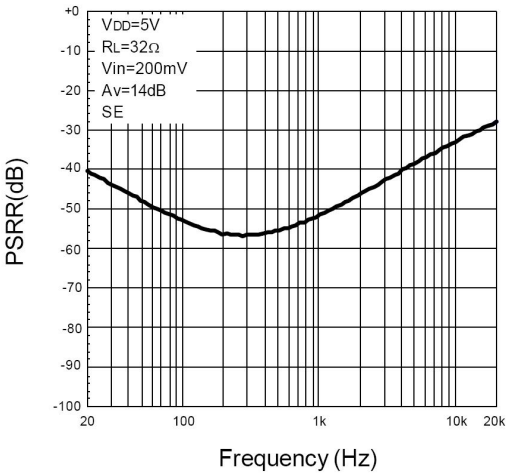
Output Noise Voltage vs. Frequency



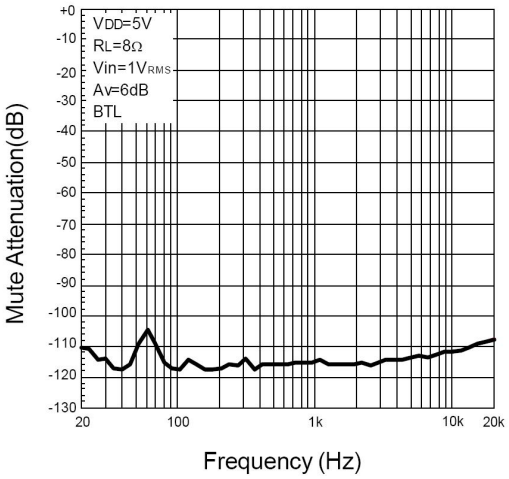
PSRR vs. Frequency



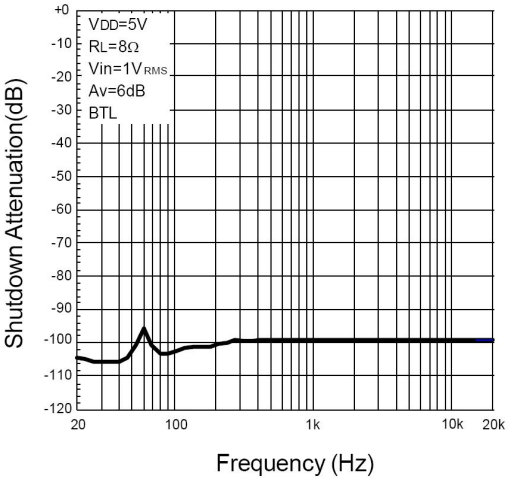
PSRR vs. Frequency



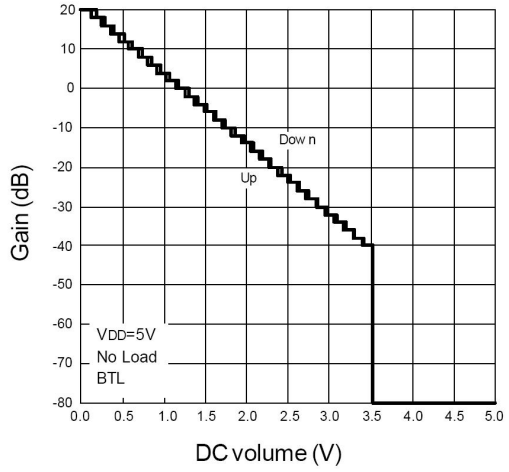
Mute Attenuation vs. Frequency



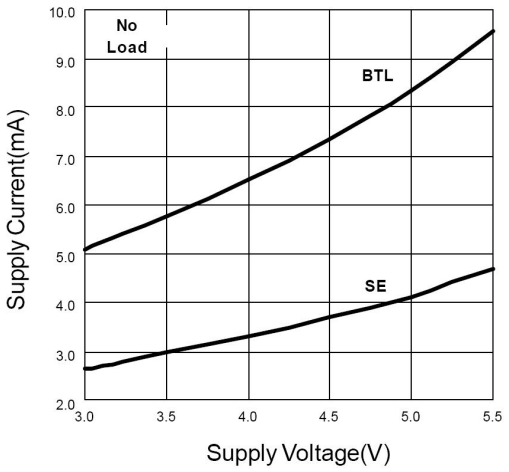
Shutdown Attenuation vs. Frequency



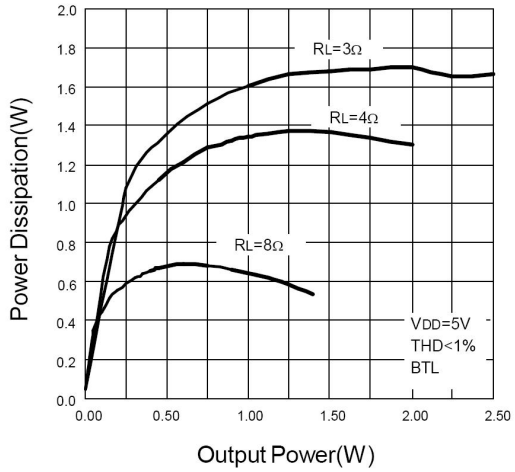
Gain vs. DC volume Voltage



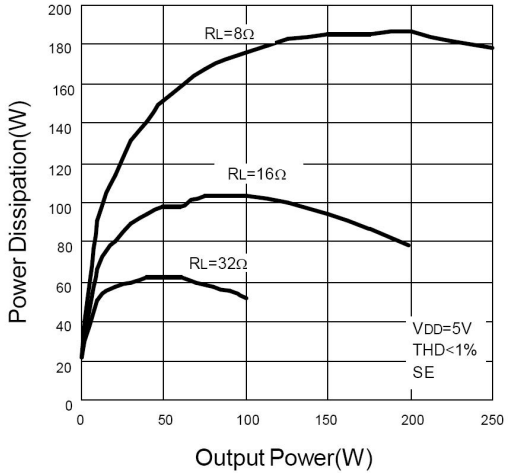
Supply Current vs. Supply Voltage



Power Dissipation vs. Output Power

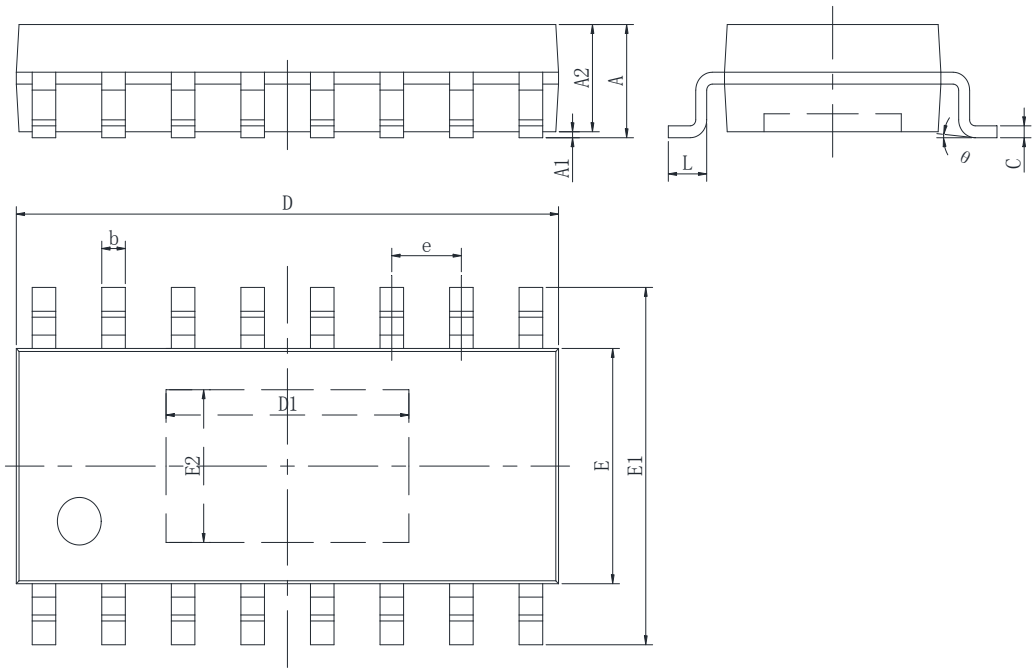


Power Dissipation vs. Output Power



OUTLINE DRAWING

ESOP16 Unit: mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.370	1.750	0.053	0.069
A1	0.020	0.080	0.001	0.003
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	-	10.200	-	0.402
D1	4.600(REF)		0.181	
E	-	4.000	-	0.157
E1	6.200	6.500	0.244	0.256
E2	2.400(REF)		0.094	
e	1.270(BSC)		0.050(BSC)	
L	0.350	0.650	0.013	0.026
θ	0°	8°	0°	8°

Statements

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