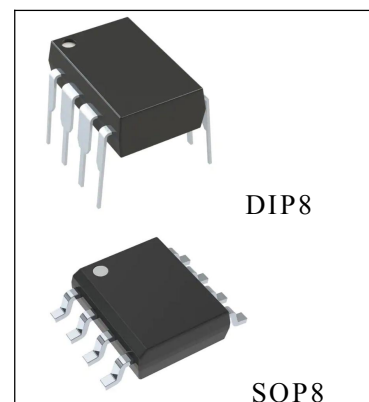


DESCRIPTION

The D4310 is a monolithic IC that includes one independent op-amp and another op-amp for which the non inverting input is wired to a 2.5V fixed Voltage Reference. This device is offering space and cost saving in many applications like power supply management or data acquisition systems.

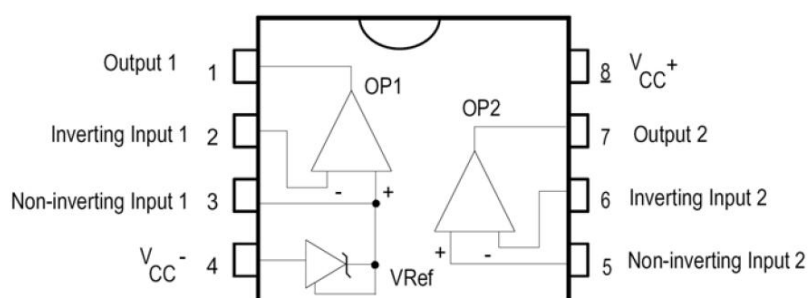
The D4310 is available in DIP8 and SOP8 packages.



FEATURES

- Low input offset voltage: 0.5mV typ.
- Low supply current : 350 μ A/op. (@ Vcc = 5V)
- Medium bandwidth (unity gain) : 0.9MHz
- Large output voltage swing : 0V to (Vcc - 1.5V)
- Input common mode voltage range includes ground
- Wide power supply range: 3 to 32V $\pm$ 1.5 to $\pm$ 16V
- Fixed output voltage reference 2.5V
- 0.4% and 1% Voltage precision
- Sink current capability : 1 to 100mA
- Typical output impedance: 0.2 Ω

PIN CONFIGURATION



Package Information

PART NO.	PACKAG DESCRIPTION	PACKAGE MARKING	PACKAGE OPTION
D4310	DIP8	CHMC D4310 SXXXX	50/Tube
D4310F	SOP8	CHMC D4310F SXXXX	4000/Reel 100/Tube

CHMC:Trademark

D4310/D4310F:Part NO.

SXXXX:Lot NO.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply voltage	V _{CC}	36	V
Differential input voltage	V _{ID}	36	V
Input voltage	V _I	-0.3 ~ +36	V
Operating free-air temperature range	T _{oper}	-40 ~ +125	°C
Max junction Temperature	T _j	150	°C
Thermal resistance junction to ambient (SOP8)	R _{thja}	175	°C/W

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min	Typ	Max	Unit
Total supply current, excluding current in the voltage reference	I _{cc}	V _{cc} ⁺ =5V,no load T _{min} <T _{amb} <T _{max}		0.7	1.2	mA
		V _{cc} ⁺ =30V,no load T _{min} <T _{amb} <T _{max}			2.0	
Independent Op-amp (unless otherwise specified: V _{cc} ⁺ =5V,V _{cc} =Ground,T _{amb} =25°C)						
Input offset voltage	V _{io}	T _{amb} =25°C T _{min} ≤T _{amb} ≤T _{max}		1	4 5	mV
Input offset voltage drift	DV _{io}			7		μV/°C
Input offset current	I _{io}	T _{min} ≤T _{amb} ≤T _{max}		2	30 50	nA
Large signal voltage gain	A _{vd}	V _{cc} =15V,R _L =2k V _o =1.4V to 11.4V T _{min} ≤T _{amb} ≤T _{max}	50 25	100		V/mV
Supply voltage rejection ratio	SVR	V _{cc} =5V to 30V	65	100		dB
Input common mode voltage range	V _{icm}	V _{cc} =+30V *1 T _{min} ≤T _{amb} ≤T _{max}	0 0		(V _{cc} +) -1.5 (V _{cc} +) -2	V
Common mode rejection ratio	CMR	T _{min} ≤T _{amb} ≤T _{max}	70 60	85		dB
Output current source	I _{source}	V _{cc} =15V,V _o =2V, V _{id} =1V	20	40		mA
Short circuit to ground	I _o	V _{cc} =15V		40	60	mA
Output current sink	I _{sink}	V _{id} =-1V V _{cc} =15V,V _o =2V	10	20		mA
High level output voltage	V _{OH}	V _{cc} ⁺ =30V, R _L =10k T _{amb} =25°C T _{min} ≤T _{amb} ≤T _{max}	27 27	28		V
Low level output voltage	V _{OL}	R _L =10k T _{min} ≤T _{amb} ≤T _{max}		5	20 20	mV
Slew rate at unity gain	SR	V _i =0.5 to 3V, V _{cc} =15V R _L =2k, C _L =100pF	0.2	0.4		V/μs

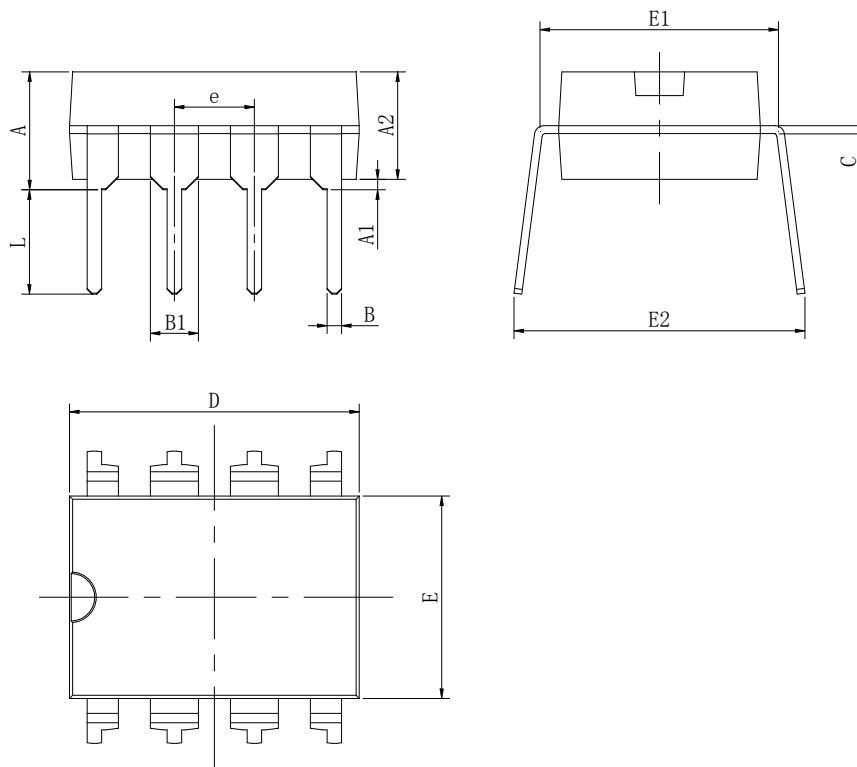
Gain bandwidth product	GBP	$V_{CC}=30V, R_L=2k$ $C_L=100pF, f=100kHz$ $V_{in}=10mV$	0.5	0.9		MHz
Total harmonic distortion	THD	$f=1kHz, A_v=20dB$ $R_L=2k, V_{CC}=30V$ $C_L=100pF, V_o=2V_{pp}$		0.02		%
Op-amp with non-inverting input connect to the internal Vref (unless otherwise specified: $V_{CC}^+=5V, V_{CC}=Ground, T_{amb}=25^{\circ}C$)						
Input offset voltage	V_{io}	$V_{icm}=0V, T_{amb}=25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$		1	4 5	mV
Input offset voltage drift	DV_{io}			7		$\mu V/^{\circ}C$
Input bias current negative input	I_{io}			20		nA
Large signal voltage gain	A_{vd}	$V_{CC}=15V, R_L=2k$ $V_{icm}=0V$		100		V/mV
Supply voltage rejection ratio	SVR	$V_{icm}=0V$ $V_{CC}^+=5V$ to 30V	65	100		dB
Output current source	I_{source}	$V_{CC}=15V, V_o=2V,$ $V_{id}=1V$	20	40		mA
Short circuit to ground	I_o	$V_{CC}=15V$		40	60	mA
Output current sink	I_{sink}	$V_{id}=-1V$ $V_{CC}=15V, V_o=2V$	10	20		mA
High level output voltage	V_{OH}	$V_{CC}^+=30V, R_L=10k$ $T_{amb}=25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$	27 27	28		V
Low level output voltage	V_{OL}	$R_L=10k$ $T_{min} \leq T_{amb} \leq T_{max}$		5	20 20	mV
Slew rate at unity gain	SR	$V_i=0.5$ to 2V, $V_{CC}=15V$ $R_L=2k, C_L=100pF$	0.2	0.4		V/ μs
Gain bandwidth product	GBP	$V_{CC}=30V, R_L=2k$ $C_L=100pF, f=100kHz$ $V_{in}=10mV$	0.5	0.9		MHz
Total harmonic distortion	THD	$f=1kHz, A_v=20dB$ $R_L=2k, V_{CC}=30V$ $C_L=100pF, V_o=2V_{pp}$		0.02		%
Cathode current	I_k		1		100	mA
Reference input voltage	V_{ref}	$T_{amb}=25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$	2.475 2.45	2.5	2.525 2.55	V
Reference input voltage deviation over temperature range	ΔV_{ref}	$V_{KA}=V_{ref}, I_k=10mA$ $T_{min} \leq T_{amb} \leq T_{max}$		7	30	mV
Minimum cathode current for regulation	I_{min}	$V_{KA}=V_{ref}$		0.5	1	mA
Dynamic impedance *2	$ Z_{KA} $	$V_{KA}=V_{ref}, \Delta I_k=1$ to 100mA, $f<1kHz$		0.2	0.5	Ω

*1 The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V_{CC}+-1.5V$. But either of both inputs can go to +36V without damage. *2 The dynamic impedance is defined as $|Z_{KA}| = \Delta V_{KA} / \Delta I_k$

OUTLINE DRAWING

DIP8:

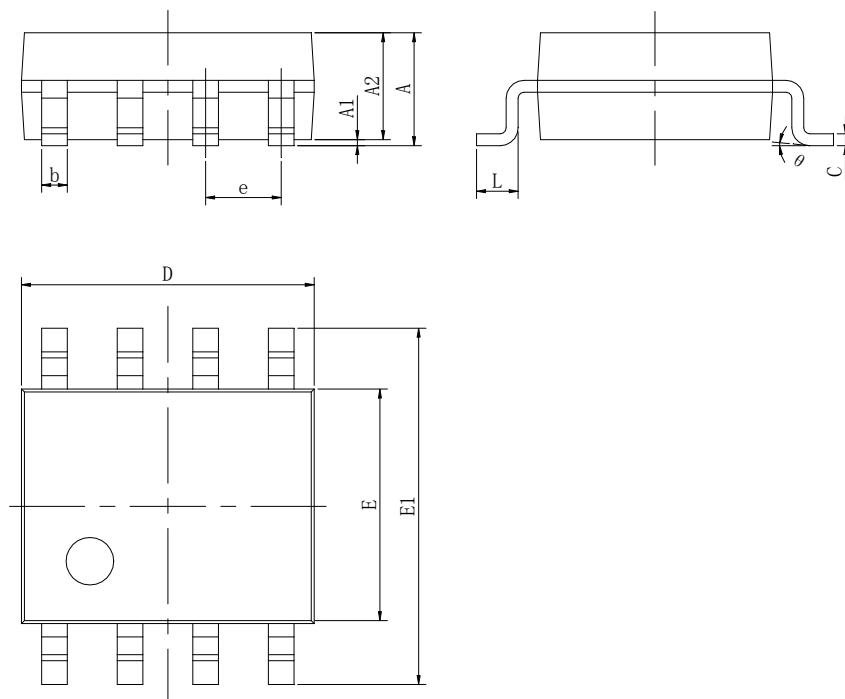
Unit: mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

SOP8:

Unit: mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.800	0.053	0.071
A1	0.050	0.250	0.004	0.010
A2	1.250	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.780	5.000	0.185	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Statements

- Silicore Technology reserves the right to make changes without further notice to any products or specifications herein. Before customers place an order, customers need to confirm whether datasheet obtained is the latest version, and to verify the integrity of the relevant information.
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