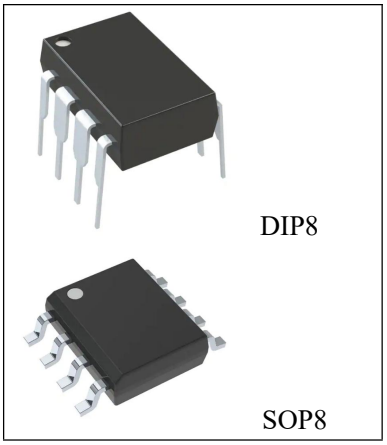
D3842/3/4/5
Current Mode PWM Controller

General Description

The D3842/3/4/5 family of control devices provides the necessary features to implement off-line or DC-to-DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 0.2mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state.



Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The D3842 and D3844 have UVLO thresholds of 16 V_{ON} and 10 V_{OFF}, ideally suited to off-line applications. The corresponding thresholds for the D3843 and D3845 are 8.4 V and 7.6 V. The D3842 and D3843 can operate to duty cycles approaching 100%. A range of zero to 50% is obtained by the D3844 and D3845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

D3842/3/4/5 is available in DIP8 and SOP8 package.

Features

- Optimized For Off-line and DC-to-DC Converters
- Low Start-up Current (<0.2mA)
- Automatic Feed Forward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- Current Mode Operation to 500KHz
- Low R_O Error Amp

Package Information

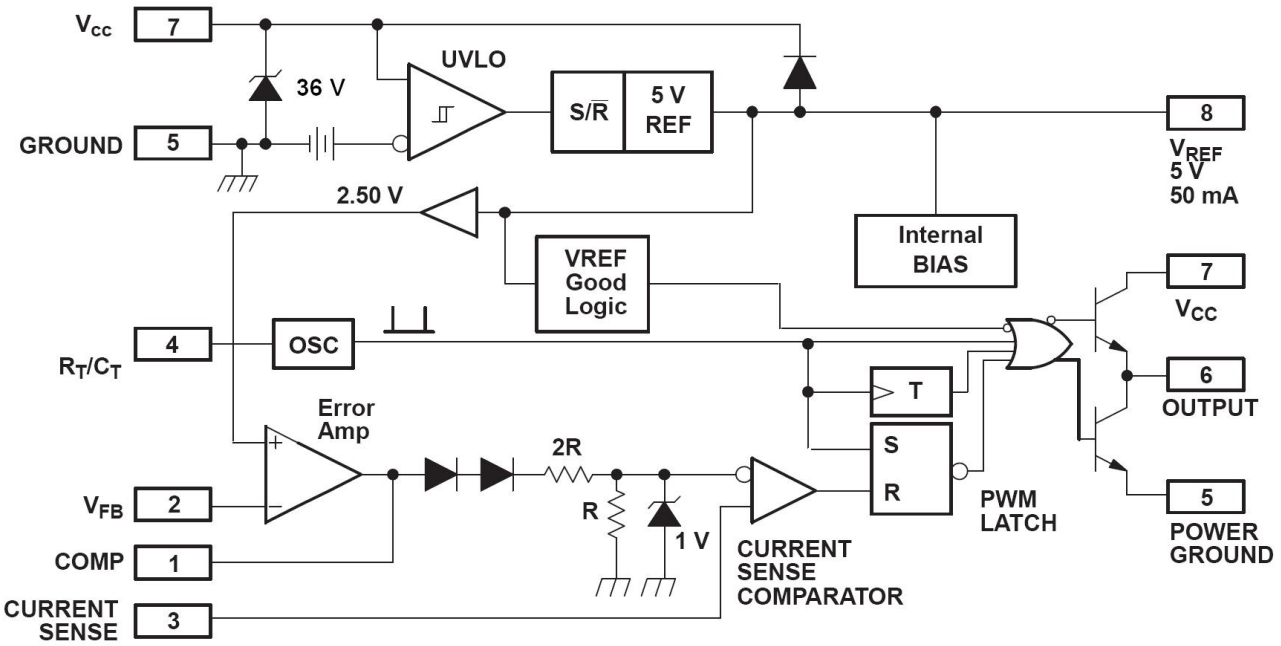
Part NO.	Order NO.	Package Description	Package Marking	Package Option
D3842	D3842	DIP8	CHMC SXX D3842	50/Tube
D3842	D3842F	SOP8	CHMC SXX D3842	100/Tube 4000/Reel
D3843	D3843	DIP8	CHMC SXX D3843	50/Tube
D3843F	D3843F	SOP8	CHMC SXX D3843F	100/Tube 4000/Reel
D3844	D3844	DIP8	CHMC SXX D3844	50/Tube
D3844	D3844F	SOP8	CHMC SXX D3844	100/Tube 4000/Reel
D3845	D3845	DIP8	CHMC SXX D3845	50/Tube
D3845	D3845F	SOP8	CHMC SXX D3845	100/Tube 4000/Reel

CHMC:Trademark D3842/D3843/D3843F/D3844/D3845:Part NO. SXX:Lot NO.

Applications

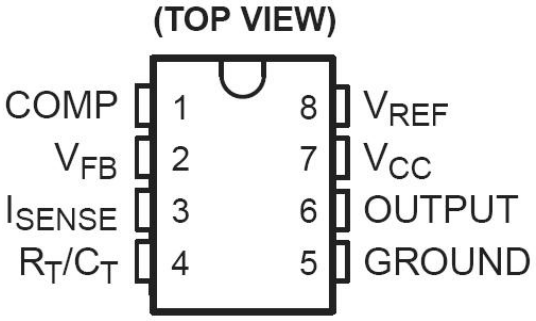
- Off-line Switched Mode Power Supplies
- DC-to-DC Converters
- DVD/STB Power Supply
- Power Adapter

Functional Block Diagram



Note : Toggle flip flop used only in D3844 and D3845

Pin Configuration



D3842/3/4/5(DIP8/SOP8)

Pin Description

Pin Number	Pin Name	Function Description
1	Comp	This pin is Error Amplifier output and is made available for loop compensation.
2	V_{FB}	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I_{SENSE}	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to Vref and capacitor C_T to ground. Operation to 500 kHz is possible.
5	Ground	This pin is the combined control circuitry and power ground.
6	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	V_{CC}	This pin is the positive supply of the control IC.
8	V_{REF}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.

Thermal Data (over operating free-air temperature range (unless otherwise noted)

Parameter Name	Symbol	DIP8	SOP8	Unit
Thermal Resistance Junction-case	θ-JC	25	42	°C/W
Thermal Resistance Junction-ambient	θ-JA	110	160	°C/W

Absolute Maximum Ratings (1)

Parameter Name		Symbol	Value	Unit
Supply Voltage (low impedance source)		V_{CC}	30	V
Supply Voltage (Icc< 30mA)		V_{CC}	Self Limiting	
Output Current		I_O	±1	A
Output Energy (capacitive load)		W	5	μJ
Analog inputs (Pins2, 3)		V_{IN}	-0.3~6.3	V
Error Amplifier Output Sink Current		I_O	10	mA
Power Dissipation at Tamb ≤ 25 °C	DIP8	P_D	1000	mW
	SOP8		650	mW
Junction Operating Temperature		T_J	150	°C
Operating Ambient Temperature		T_A	-25~85	°C
Storage Temperature Range		Ts	-65~150	°C
Lead Temperature (soldering 10s)		T_L	300	°C

(1) All voltages are with respect to Pin 5. All currents are positive into the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

Electrical Characteristics(Unless otherwise stated, V_{CC}=15V(1); R_T=10kΩ; C_T=3.3nF, T_A=T_J.)

Parameter Name	Test Conditions	Symbol	Min	Typ	Max	Unit
Reference Section						
Output Voltage	T_J=25°C,I_O=1mA	V_{REF}	4.95	5.00	5.05	V
Line Regulation	12V≤V_{IN}≤25V	ΔV_{REF}		6	20	mV
Load Regulation	1mA≤I_O≤20mA	ΔV_{REF}		6	25	mV
Temp. Stability	See(2)(3)	T_S		0.2		mV/°C
Total Output Variation	Line, load, Temperature(2)	V_{REF}	4.85		5.15	V
Output Noise Voltage	10Hz≤f≤10kHz,T_J=25°C (2)	V_N		50		μV
Long Term Stability	T_A=125°C,1000Hrs(2)	S		5	25	mV
Output Short Circuit		I_{SC}	-30	-100	-180	mA
Oscillator Section						
Frequency	T_J=25°C(4)	f_{OSC}	47	52	57	kHz
Voltage Stability	12V≤V_{CC}≤25V	$\Delta f_{OSC}/\Delta V$		0.2	1.0	%
Temp. Stability	T_{MIN}≤T_A≤T_{MAX}(2)	$\Delta f_{OSC}/\Delta T$		5		%
Oscillator Voltage Swing	V_{PIN4} peak-to-peak(2)	V_{OSC}		1.6		V
Error AMP Section						
Input Voltage	V_{PIN1}=2.5V	V_{FB}	2.42	2.50	2.58	V
Input Bias Current		I_{IB}		-2.0	-10.0	μA
Open Loop Voltage Gain	2V≤V_O≤4V	A_{VOL}	65	90		dB
Unity Gain Bandwidth	Tj=25°C(5)	BW	0.7	1.0		MHz
Power Supply Rejection Ratio	12V≤V_{CC}≤25V	PSRR	60	70		dB
Output Sink Current	V_{PIN2}=2.7V,V_{PIN1}=1.1V	I_{SINK}	2	6		mA
Output Source Current	V_{PIN2}=2.3V,V_{PIN1}=5V	I_{SOURSE}	-0.5	-1.0		mA
Output Voltage Swing High State	V_{PIN2}=2.3V,R_L=15kΩ to Gnd	V_{OH}	5.0	6.0		V
Output Voltage Swing Low State	V_{PIN2}=2.7V,R_L=15kΩ to Vref	V_{OL}		0.7	1.1	V
Current Sense Section						
Gain	See(6)(7)	A_V	2.85	3.00	3.15	V/V
Maximum Input Signal	V_{PIN1}=5V(6)	V_{th}	0.9	1.0	1.1	V
Power Supply Rejection Ratio	12V≤V_{CC}≤25V(5)(6)	PSRR		70		dB
Input Bias Current		I_{IB}		-2	-10	μA
Delay to Output	V_{PIN3}=0V to 2V(5)	T_{PLH}(in/out)		150	300	ns

Characteristics	Test conditions	Symbol	Min	Typ	Max	Unit
Output Section						
Output Low Level	I_{SINK}=20mA	$V_{OL=20mA}$		0.1	0.4	V
	I_{SINK}=200mA	$V_{OL=200mA}$		1.5	2.2	V
Output High Level	I_{SOURSE}=20mA	$V_{OH=20mA}$	13.0	13.5		V
	I_{SOURSE}=200mA	$V_{OH=200mA}$	12.0	13.5		V
Rise Time	T_J=25°C,C_L=1nF(5)	t_R		50	150	ns
Fall Time		t_F		50	150	ns
Under-Voltage Lockout Section						
Start Threshold	D3842/4	V_{TH}	14.5	16.0	17.5	V
	D3843/5		7.8	8.4	9.0	
Min. Operating Voltage After Turn On	D3842/4	$V_{CC(min)}$	8.5	10.0	11.5	V
	D3843/5		7.0	7.6	8.2	
PWM Section						
Maximum Duty Cycle	D3842/3	D_{MAX}	94	96	100	%
	D3844/5		47	48	50	
Minimum Duty Cycle		D_{MIN}			0	%
Total Standby Current						
Start-up Current		I_{ST}		0.1	0.2	mA
Operating Supply Current	V_{PIN2}=V_{PIN3}=0V	I_{CC}		12	17	mA
Zener voltage	I_{CC}=25mA	V_Z	30	36		V

(1) Adjust V_{CC} above the start threshold before setting at 15 V.

(2) These parameters, although specified, are not 100% tested in production.

(3) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

Temp Stability= $\frac{V_{REF}(\max)-V_{REF}(\min)}{T_J(\max)-T_J(\min)}$ V_{REF}(max) and V_{REF}(min) are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.

(4) Output frequency equals oscillator frequency for the D3842 and D3843.
Output frequency is one half oscillator frequency for the D3844 and D3845.

(5) These parameters, although specified, are not 100% tested in production.

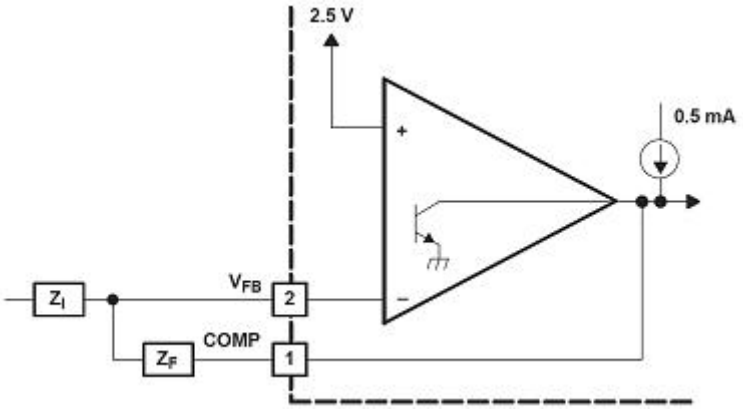
(6) Parameter measured at trip point of latch with V_{PIN2} = 0.

(7) Gain defined as: $A=\frac{\Delta V_{PIN1}}{\Delta V_{PIN3}}$, 0≤$V_{PIN3}$≤0.8V.

Application Information

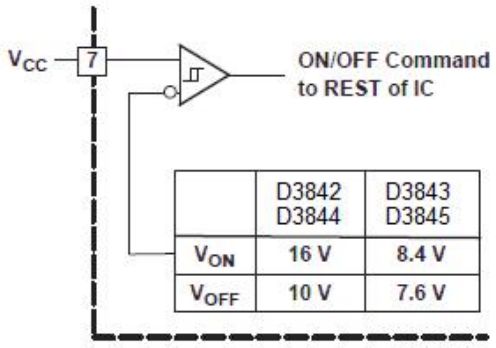
Error AMP Configuration

Error AMP can source or sink up to 0.5mA.

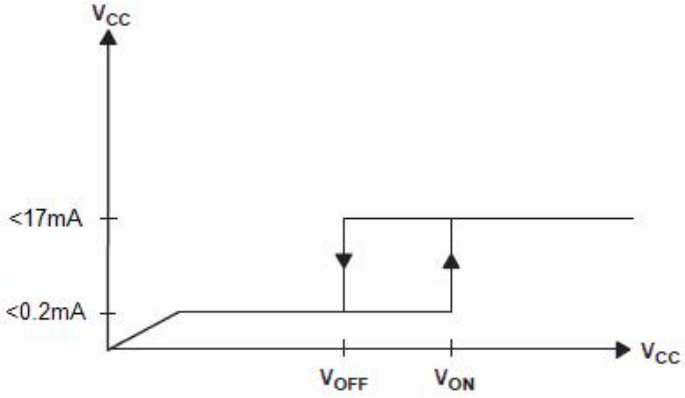


Under-Voltage Lockout

During under-voltage lock-out, the output drive is biased to sink minor amounts of current. Pin6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

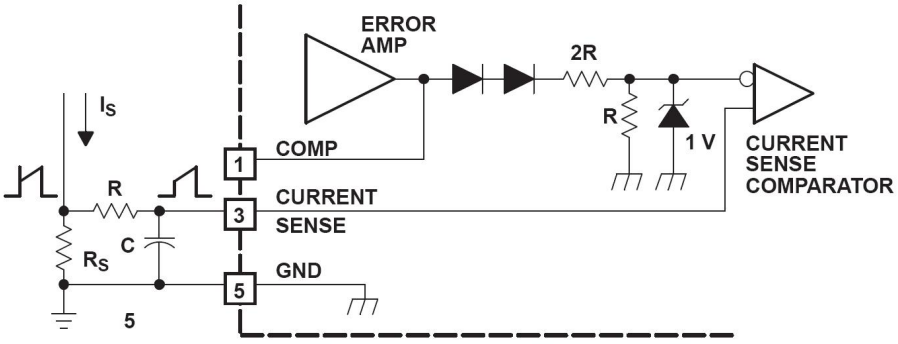


	D3842 D3844	D3843 D3845
V_{ON}	16 V	8.4 V
V_{OFF}	10 V	7.6 V



Current Sense Circuit

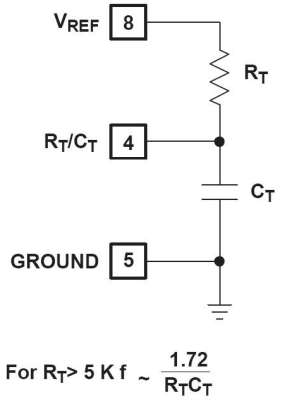
A small RC filter may be required to suppress switch transients.

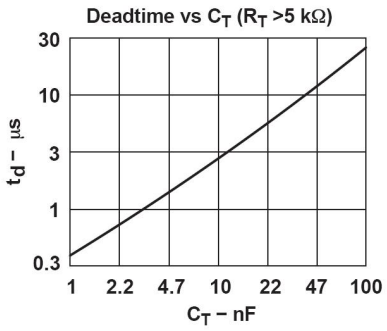


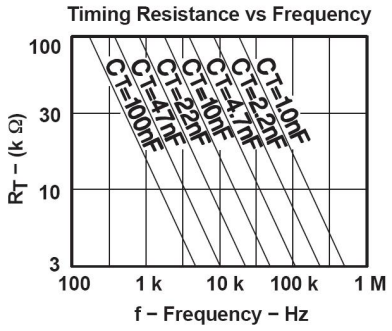
Peak Current (I_S) is Determined By The Formula

$$I_{SMAX} \approx \frac{1.0\ V}{RS}$$

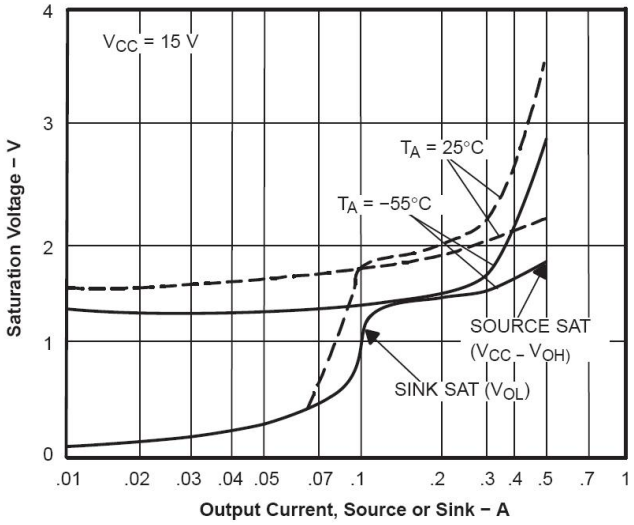
Oscillator Section



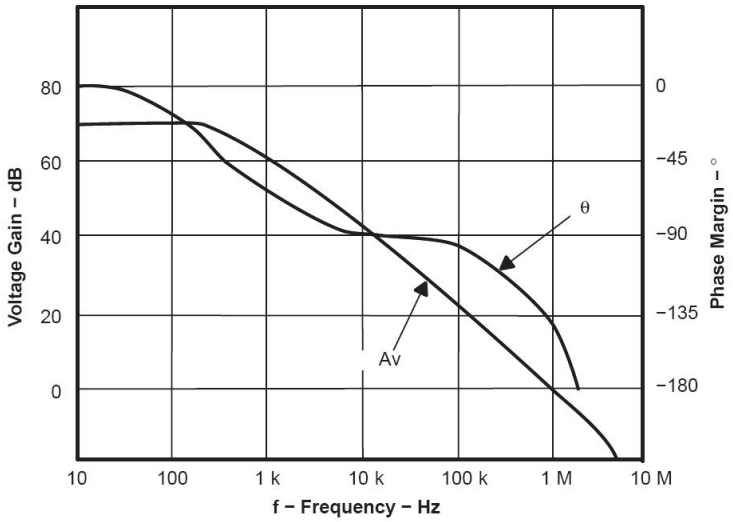




Output Saturation Characteristics

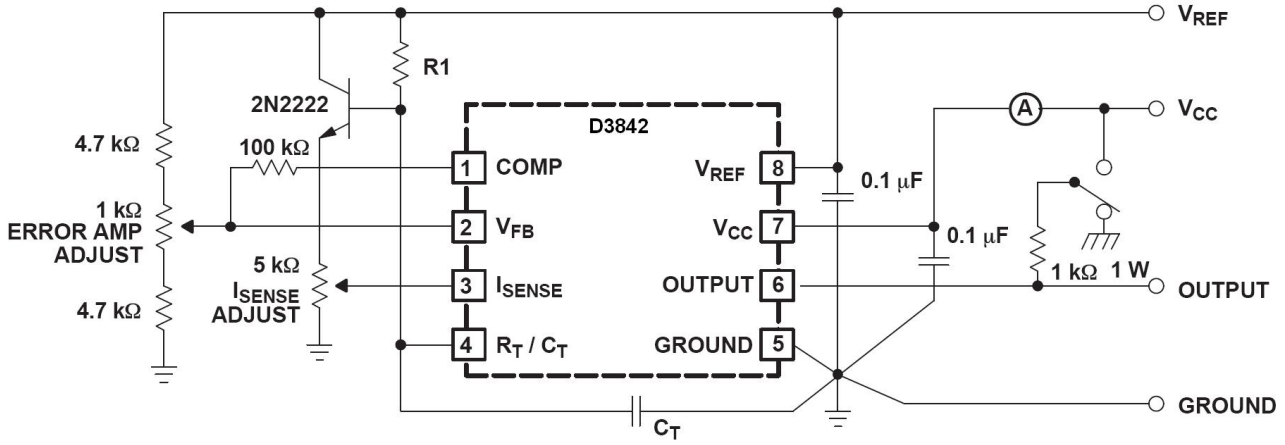


Error Amplifier Open-Loop Frequency Response



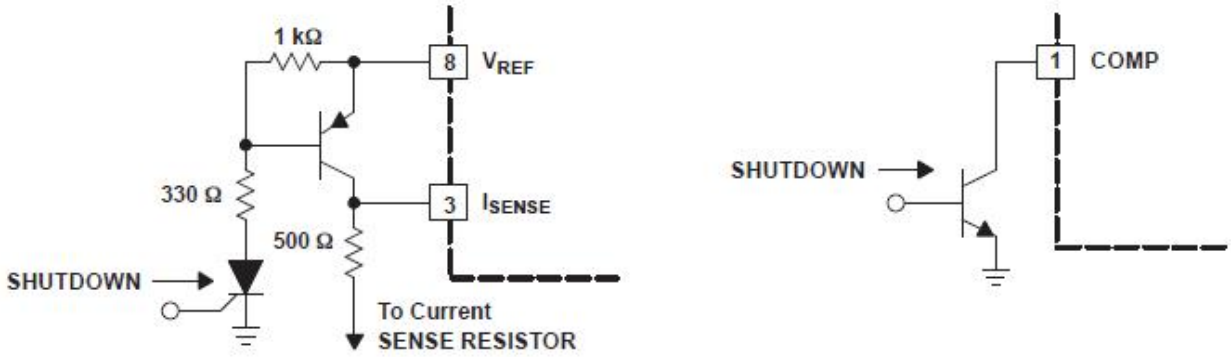
Open-Loop Laboratory Fixture

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin3.

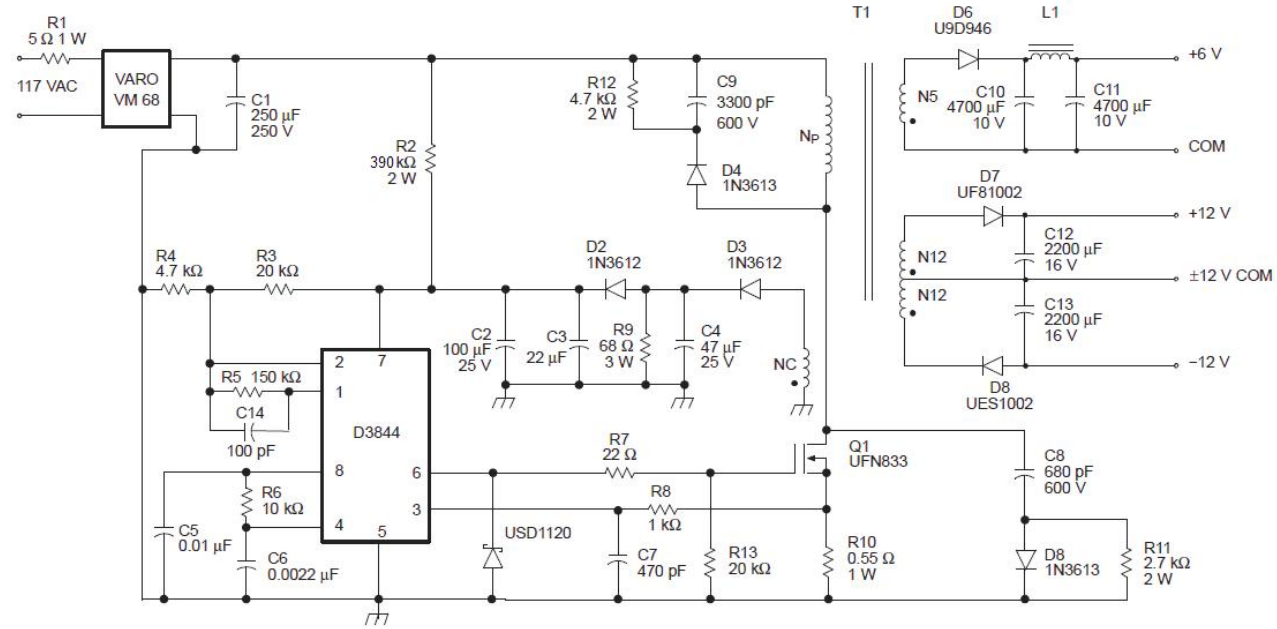


Shutdown Techniques

Shutdown of the D3842 can be accomplished by two methods; either raise pin3 above 1V or pull pin1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pin1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower UVLO threshold. At this pint the reference turns off, allowing the SCR to reset.



Offline Flyback Regulator

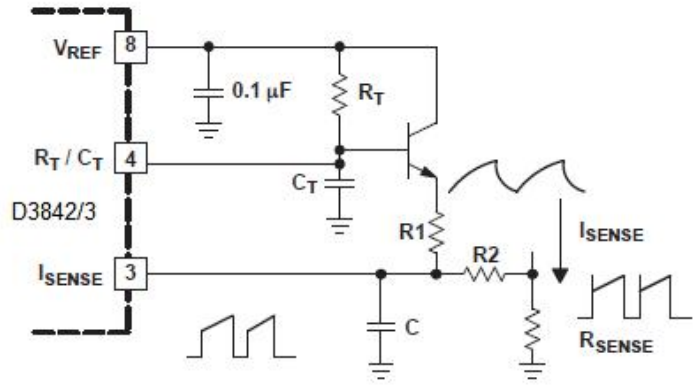


Power Supply Specifications

1. Input Voltages $95V_{AC}$ to $130V_{AC}$ (50Hz/60Hz)
2. Line Isolation: 3750V
3. Switching Frequency: 40kHz
4. Efficiency at Full Load 70%
5. Output Voltage: a. +5 V, ±5%; 1A to 4A load Ripple voltage: $50mV_{P\text{-}P\ Max}$
   b. +12 V, ±3%; 0.1A to 0.3A load Ripple voltage: $100mV_{P\text{-}P\ Max}$
   c. –12 V, ±3%; 0.1A to 0.3A load Ripple voltage: $100mV_{P\text{-}P\ Max}$

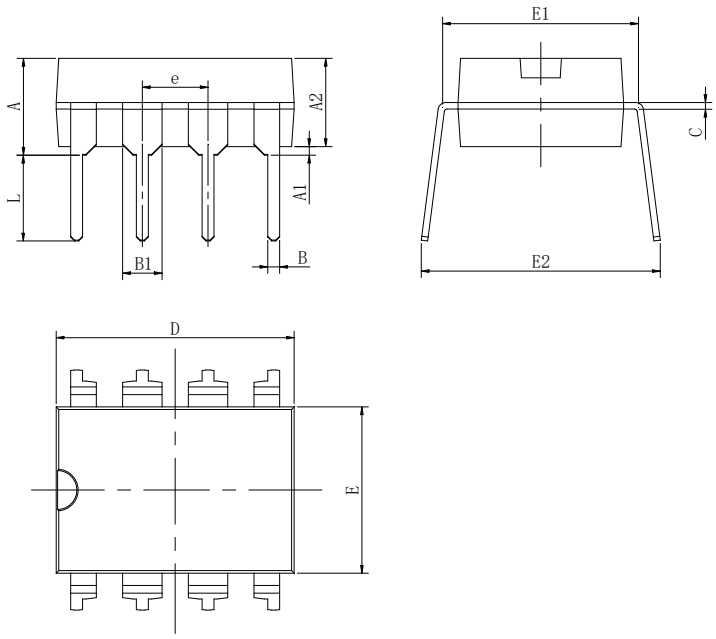
Slope Compensation

A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.



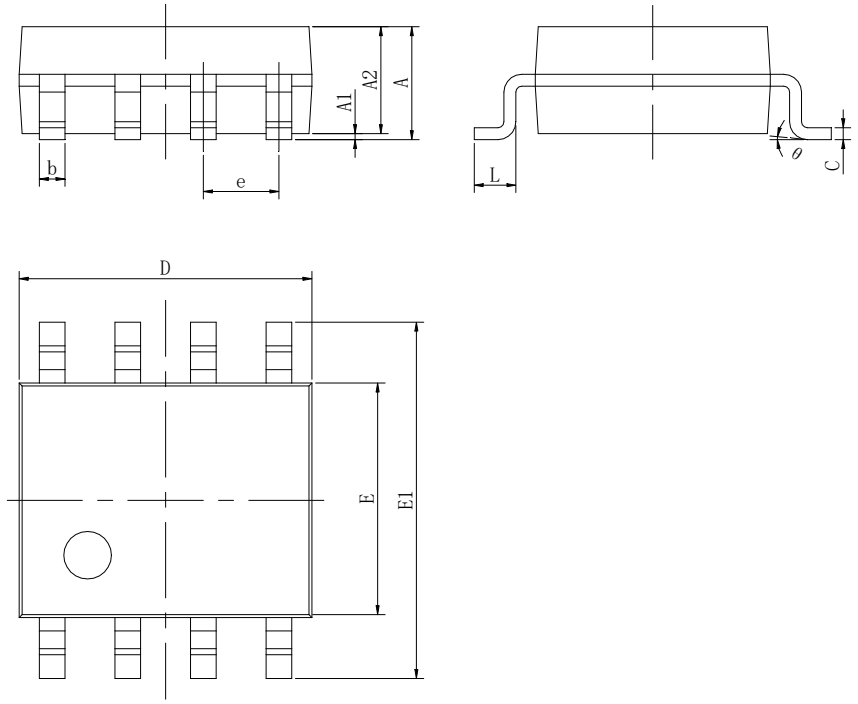
Outline Dimensions

DIP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	7.800	9.000	0.307	0.354

SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.800	0.053	0.071
A1	0.000	0.250	0.000	0.010
A2	1.250	1.550	0.053	0.061
b	0.300	0.510	0.011	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Statements

- Silicore Technology reserves the right to make changes without further notice to any products or specifications herein. Before customers place an order, customers need to confirm whether datasheet obtained is the latest version, and to verify the integrity of the relevant information.

- Failure or malfunction of any semiconductor products may occur under particular conditions, customers shall have obligation to comply with safety standards when customers use Silicore Technology products to do their system design and machine manufacturing, and take corresponding safety measures in order to avoid potential risk of failure that may cause personal injury or property damage.

- The product upgrades without end, Silicore Technology will wholeheartedly provide customers integrated circuits that have better performance and better quality.