1 General description

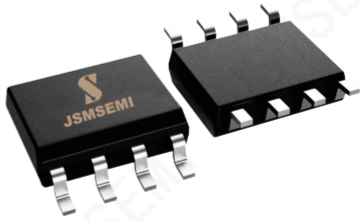
The TJA1044 is part of the Mantis family of high-speed CAN transceivers. It provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing the differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.
The TJA1044 offers a feature set optimized for 12V automotive applications, with significant improvements over such as the TJA1040 and TJA1042, and excellent ElectroMagnetic Compatibility (EMC) performance.
Additionally, the TJA1044 features:

- Ideal passive behavior to the CAN bus when the supply voltage is off
- A very low-current Standby mode with bus wake-up capability
- Excellent EMC performance at speeds up to 500kbit/s, even without a common mode choke
- TJA1044T/3 and TJA1044TK/3 can be interfaced directly to microcontrollers with supply voltages from 2.2V to 5.5V

These features make the TJA1044 an excellent choice for all types of HS-CAN networks, in nodes that require a low-power mode with wake-up capability via the CAN bus.
The TJA1044 implements the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5. The TJA1044T is specified for data rates up to 1 Mbit/s. Additional timing parameters defining loop delay symmetry are specified for the other variants. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

2 Features and benefits

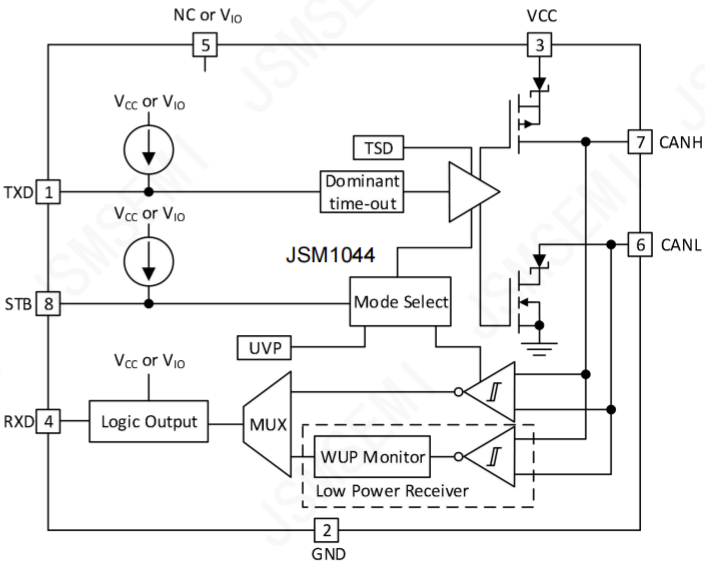
- Fully ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant
- Very low-current Standby mode with host and bus wake -up capability
- Optimized for use in 12 V automotive systems
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)
- V_{IO} input on TJA1044x/3 variants allows for direct interfacing with 3 V to 5 V microcontrollers. Variants without a V_{IO} pin can interface with 3.3 V and 5 V-supplied microcontrollers, provided the microcontroller I/Os are 5 V tolerant.



- Both V_{IO} and non-V_{IO} variants are available in SOP-8 and leadless DFN-8 (3.0× 3.0 mm) packages; DFN-8 with improved Automated Optical Inspection (AOI) capability.
- Functional behavior predictable under all supply conditions
- Transceiver disengages from bus when not powered (zero load)
- Transmit Data (TXD) and bus dominant time-out functions
- Internal biasing of TXD and STB input pins
- High ESD handling capability on the bus pins
- Bus pins protected against transients in automotive environments
- Undervoltage detection on pins V_{CC} and V_{IO}
- Thermally protected

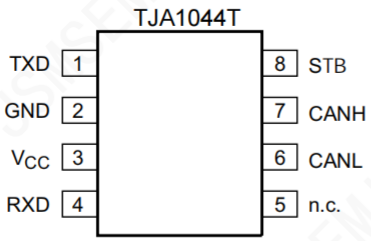
3 Applications

- Automotive and transportation
- Body control modules
- Automotive gateway
- Advanced driver assistance system (ADAS)

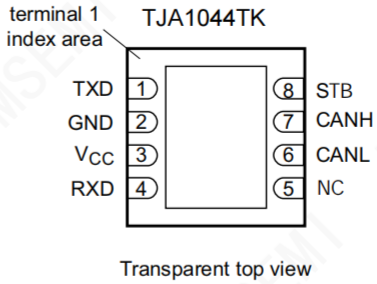


Simplified Schematic

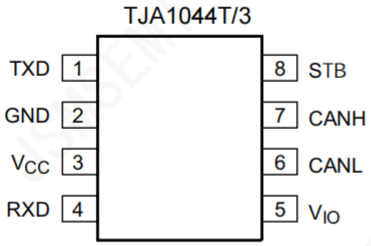
4 Pinning information



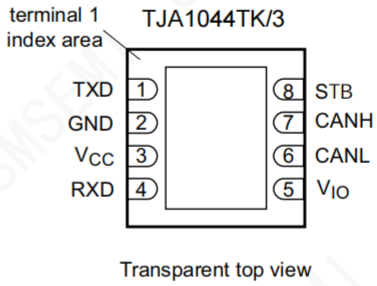
a. TJA1044T: SOP-8



b. TJA1044TK: SOP-8



c. TJA1044T/3: SOP-8



d. TJA1044TK/3: DFN-8

Table 4-1 Pin Functions

Pins		Type	Description
Name	No.		
TXD	1	Digital Input	CAN transmit data input; integrated pull-up
GND	2	GND	Ground connection
V_{CC}	3	POWER	Transceiver 5V supply voltage
RXD	4	DIGITAL OUTPUT	CAN receive data output, tri-stated when device powered off
NC	5	-	Not internally connected; Devices without V_{IO}
V_{IO}	5	Supply	I/O supply voltage For devices in this series with V_{IO} ports,
CANL	6	Bus IO	Low-level CAN bus input/output line
CANH	7	Bus IO	High-level CAN bus input/output line
STB	8	Digital Input	Standby input for mode control; integrated pull-up
Thermal Pad (DFN8 only)		-	Connect the thermal pad to any internal PCB ground plane using multiple vias for optimal thermal performance.

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
TJA1044T-JSM	SOP-8	JSM1044T	-40 to 125°C	3	T&R,2500	Rohs
TJA1044TK-JSM	DFN-8	JSM1044	-40 to 125°C	3	T&R,3000	Rohs
TJA1044T/3-JSM	SOP-8	JSM1044T/3	-40 to 125°C	3	T&R,2500	Rohs
TJA1044TK/3-JSM	DFN-8	A1044/3	-40 to 125°C	3	T&R,3000	Rohs

5 Specifications

Absolute Maximum Ratings

See Note (1)(2)

Parameter	Description	MIN	MAX	UNIT
V_{CC}	Supply voltage	-0.3	7	V
V_{IO}	Supply voltage I/O level shifter	-0.3	7	V
V_{BUS}	CAN Bus I/O voltage	-70	70	V
V_{DIFF}	Max differential voltage between CANH and CANL	-45	45	V
V_{Logic_input}	Logic input terminal voltage	-0.3	7	V
V_{RXD}	RXD output terminal voltage range	-0.3	7	V
$I_{O(RXD)}$	RXD output current	-8	8	mA
T_J	Junction temperature	-40	165	°C
T_{STG}	Storage temperatur	-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

ESD Ratings

	Test Conditions	VALUE	UNIT
Human Body Model (HBM) ESD stress voltage	All terminals	±8000	V
	CAN bus terminals (CANH, CANL)	±15000	
Charged Device Model (CDM) ESD stress voltage	All terminals	±2000	V
IEC Contact Discharge (IEC 61000-4-2)	CAN bus terminals (CANH, CANL)	±8000	

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IO}	Supply voltage for I/O Level-Shifting	1.7		5.5	
$I_{OH(RXD)}$	RXD terminal high-level output current, Devices with V_{IO}	-1.5			mA
$I_{OL(RXD)}$	RXD terminal low-level output current, Devices with V_{IO}			1.5	
$I_{OH(RXD)}$	RXD terminal high-level output current, Devices without V_{IO}	-2			
$I_{OL(RXD)}$	RXD terminal low-level output current, Devices without V_{IO}			2	

Supply Characteristics

Over recommended operating conditions with T_J = -40°C to 150°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current Normal mode	Dominant	STB = 0V, TXD = 0V, R_L = 60Ω, C_L = open, See Figure 6-1		40	70	mA
			STB = 0V, TXD = 0V, R_L = 50Ω, C_L = open, See Figure 6-1		45	80	mA
		Recessive	STB = 0V, TXD = V_{CC} or V_{IO}, R_L = 50Ω, C_L = open See Figure 6-1		0.6	1	mA
		Dominant with bus fault	STB = 0V, TXD = 0V, CANH = CANL = ±25V, R_L = open, C_L = open, See Figure 6-1			130	mA
	Supply current Standby mode Devices with V_{IO}		STB = TXD = V_{IO}, R_L = 50 Ω, C_L = open, See Figure 6-1		2.2	5	μA
	Supply current Standby mode Devices without V_{IO}		STB = TXD = V_{CC}, R_L = 50Ω, C_L = open, See Figure 6-1			15	μA
I_{IO}	I/O supply current Normal mode	Dominant	STB = 0V, TXD = 0V, RXD floating		100	300	μA
	I/O supply current Normal mode	Recessive	STB = 0V, TXD = 0V, RXD floating			48	μA
	I/O supply current Standby mode		STB = V_{IO}, TXD = 0V, RXD floating		2.2	5	μA
UV_{CC}	Rising undervoltage detection on V_{CC} for protected mode				3.2	3.4	V
	Falling undervoltage detection on V_{CC} for protected mode			2.8	3.0	3.25	V
$V_{HYS(UVCC)}$	Hysteresis voltage on UV_{CC}				200		mV
UV_{VIO}	Rising undervoltage detection on V_{IO} (Devices with V_{IO})				2.2	2.65	V
	Falling undervoltage detection on V_{IO} (Devices with V_{IO})			1.3	2.0	2.2	V
$V_{HYS(UVIO)}$	Hysteresis voltage on UV_{IO}				200		mV

Electrical Ratings

Over recommended operating conditions (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics							
$V_{O(DOM)}$	Dominant output voltage Normal mode	CANH	STB = 0V, TXD = 0V, 50Ω ≤ R_L ≤ 65Ω C_L = open, R_{CM} = open See Figure 6-2 and Figure 7-3	2.75		4.5	V
		CANL		0.5		2.25	V
$V_{O(REC)}$	Recessive output voltage Normal mode	CANH and CANL	STB = 0V, TXD = V_{IO}, R_L = open (no load), R_{CM} = open See Figure 6-2 and Figure 7-3	2	0.5V_{CC}	3	V
V_{SYM}	Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}		STB = 0V, TXD = 250kHz, 1MHz, 2.5MHz, R_L = 60Ω, C_{SPLIT} = 4.7nF, C_L = open, R_{CM} = open See Figure 6-2 and Figure 8-2	0.9		1.1	V/V
V_{SYM_DC}	DC output symmetry (V_{CC} - $V_{O(CANH)}$ - $V_{O(CANL)}$)		STB = 0V, R_L = 60Ω, C_L = open See Figure 6-2 and Figure 7-3	-400		400	mV
$V_{OD(DOM)}$	Differential output voltage Normal mode Dominant	CANH - CANL	STB = 0V, TXD = 0V, 50Ω ≤ R_L ≤ 65Ω, CL = open, See Figure 6-2 and Figure 7-3	1.5		3	V
			STB = 0V, TXD = 0V, 45Ω ≤ R_L ≤ 70Ω, C_L = open, See Figure 6-2 and Figure 7-3	1.4		3.3	V
			STB = 0V, TXD = 0V, R_L = 2240Ω, C_L = open, See Figure 6-2 and Figure 7-3	1.5		5	V
$V_{OD(REC)}$	Differential output voltage Normal mode Recessive	CANH - CANL	STB = 0V, TXD = V_{IO}, R_L = 60Ω, C_L = open See Figure 6-2 and Figure 7-3	-120		12	mV
			STB = 0V, TXD = V_{IO}, R_L = open, C_L = open See Figure 6-2 and Figure 7-3	-50		50	mV
$V_{O(STB)}$	Bus output voltage Standby mode	CANH	STB = V_{IO} , R_L = open See Figure 6-2 and Figure 7-3	-0.1		0.1	V
		CANL		-0.1		0.1	V
		CANH and CANL		-0.2		0.2	V
$I_{OS(SS\_DOM)}$	Short-circuit steady-state output current, dominant Normal mode		STB = 0 V, TXD = 0V $V_{(CANH)}$ = -15V to 40V, CANL = open See Figure 6-7 and Figure 7-3	-115			mA
			STB = 0 V, TXD = 0V $V_{(CAN\_L)}$ = -15V to 40V, CANH = open See Figure 6-7 and Figure 7-3			115	mA
$I_{OS(SS\_REC)}$	Short-circuit steady-state output current, recessive Normal mode		STB = 0V, TXD = V_{IO}, –27V ≤ V_{BUS} ≤ 32V, where V_{BUS} = CANH = CANL See Figure 6-7 and Figure 7-3	-5		5	mA

Electrical Characteristics(continued)

Over recommended operating conditions with T_J = -40°C to 150°C (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
Receiver Electrical Characteristics						
V_{IT}	Input threshold voltage Normal mode	STB = 0V, -12V ≤ V_{CM} ≤ 12V See Figure 6-3 and Table 7-6	500		900	mV
$V_{IT(STB)}$	Input threshold Standby mode	STB = V_{IO}, -12V ≤ V_{CM} ≤ 12V See Figure 6-3 and Table 7-6	400		1150	mV
V_{DOM}	Dominant state differential input voltage range Normal mode	STB = 0V, -12V ≤ V_{CM} ≤ 12V See Figure 6-3 and Table 7-6	0.9		9	V
V_{REC}	Recessive state differential input voltage range Normal mode	STB = 0V, -12V ≤ V_{CM} ≤ 12V See Figure 6-3 and Table 7-6	-4		0.5	V
$V_{DOM(STB)}$	Dominant state differential input voltage range Standby mode	STB = V_{IO}, -12V ≤ V_{CM} ≤ 12V See Figure 6-3 and Table 7-6	1.15		9	V
$V_{REC(STB)}$	Recessive state differential input voltage range Standby mode	STB = V_{IO}, -12V ≤ V_{CM} ≤ 12V See Figure 6-3 and Table 7-6	-4		0.4	V
V_{HYS}	Hysteresis voltage for input threshold Normal mode	STB = 0V, -12V ≤ V_{CM} ≤ 12V See Figure 6-3 and Table 7-6		120		mV
V_{CM}	Common-mode range Normal and standby modes	See Figure 6-3 and Table 7-6	-30		30	V
$I_{LKG(IOFF)}$	Unpowered bus input leakage current	CANH = CANL = 5V, V_{CC} = V_{IO} = GND			5	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{IO} (1)			20	pF
C_{ID}	Differential input capacitance				10	pF
R_{ID}	Differential input resistance	STB = 0V, TXD = V_{IO} (1) -12V ≤ V_{CM} ≤ 12V	20	30	50	kΩ
R_{IN}	Single-ended input resistance (CANH or CANL)		10	15	25	kΩ
$R_{IN(M)}$	Input resistance matching [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 %	$V_{(CAN\_H)}$ = $V_{(CAN\_L)}$ = 5V	-1		1	%
TXD Terminal (CAN Transmit Data Input)						
V_{IH}	High-level input voltage	Devices without V_{IO}	0.7V_{CC}			V
V_{IH}	High-level input voltage	Devices with V_{IO}	0.7V_{IO}			V
V_{IL}	Low-level input voltage	Devices without V_{IO}			0.3V_{CC}	V
V_{IL}	Low-level input voltage	Devices with V_{IO}			0.3V_{IO}	V
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 5.5V	-2.5	0	1	µA
I_{IL}	Low-level input leakage current	TXD = 0V, V_{CC}= V_{IO} = 5.5V	-100	-40	-7	µA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5V, V_{CC}= V_{IO} = 0V	-1	0	1	µA
C_I	Input capacitance	V_{IN} = 0.4×sin(2×π×2×10^6×t)+2.5V		5		pF

Electrical Characteristics (continued)

Over recommended operating conditions with T_J = -40°C to 150°C (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
RXD Terminal (Can Receive Data Output)						
V_{OH}	High-level output voltage	I_O = –2mA, Devices without V_{IO}, See Figure 6-3	0.8V_{CC}			V
		I_O = –1.5mA, Devices with V_{IO} See Figure 6-3	0.8V_{IO}			
V_{OL}	Low-level output voltage	I_O = 2mA, Devices without V_{IO} See Figure 6-3			0.2V_{CC}	
		I_O = 1.5mA, Devices with V_{IO} See Figure 6-3			0.2V_{IO}	
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.5V, V_{CC} = V_{IO} = 0V	-1	0	-1	µA
STB Terminal (Standby Mode Input)						
V_{IH}	High-level input voltage	Devices without V_{IO}	0.7V_{CC}			V
		Devices with V_{IO}	0.7V_{IO}			V
V_{IL}	Low-level input voltage	Devices without V_{IO}			0.3V_{CC}	V
		Devices with V_{IO}			0.3V_{IO}	V
I_{IH}	High-level input leakage current	V_{CC} = V_{IO} = STB = 5.5V	-2		2	µA
I_{IL}	Low-level input leakage current	STB = 0V, V_{CC} = V_{IO} = 5.5V,	-20		-2	µA
$I_{LKG(OFF)}$	Unpowered leakage current	STB = 5.5V, V_{CC} = V_{IO} = 0V	-1	0	1	µA

(1) V_{IO} = V_{CC} in non-V variants of device

Switching Characteristics

Over recommended operating conditions (unless otherwise noted)

Parameter			Test Conditions	Min	Typ	Max	Unit
Device Switching Characteristics							
$t_{PROP(LOOP1)}$	Total loop delay, Driver input (TXD) to receiver output (RXD), recessive to dominant		STB = 0V, V_{IO} = 2.8V to 5.5V, R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF, See Figure 6-4		110	160	ns
			STB = 0V, V_{IO} = 1.7V, R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF, See Figure 6-4		150	220	
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive		STB = 0V, V_{IO} = 2.8V to 5.5V, R_L = 60 Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF, See Figure 6-4		150	220	
			STB = 0V, V_{IO} = 1.7V, R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF, See Figure 6-4		180	255	
t_{MODE}	Mode change time, from Normal to Standby or from Standby to Normal		See Figure 6-5		20	45	µs
t_{WK_FILTER}	Filter time for valid wake up pattern		See Figure 7-5	0.5		1.8	µs
$t_{WK\_TIMEOUT}$	Bus wake-up timeout			0.8		6	ms
Driver Switching Characteristics							
t_{pHR}	Propagation delay time,high TXD to driver recessive (dominant to recessive)		STB = 0V, R_L = 60Ω, C_L = 100pF See Figure 6-2		80		ns
t_{pLD}	Propagation delay time,low TXD to driver dominant (recessive to dominant)				65		
$t_{sk(p)}$	Pulse skew (|tpHR - tpLD|)				15		
t_R	Differential output signal rise time				45		
t_F	Differential output signal fall time				45		
t_{TXD_DTO}	Dominant timeout		See Figure 6-6	1.2		4.0	ms
Receiver Switching Characteristics							
t_{pRH}	Propagation delay time, bus recessive input to high output (Dominant to Recessive)		STB = 0V, $C_{L(RXD)}$ = 15pF See Figure 6-3		55		ns
t_{pDL}	Propagation delay time, bus dominant input to low output (Recessive to Dominant)				55		ns
t_R	RXD Output signal rise time				10		ns
t_F	RXD Output signal fall time				10		ns
FD Timing Characteristics							
$t_{BIT(BUS)}$	Bit time on CAN bus output pins	$t_{BIT(TXD)}$ = 500ns	STB = 0V, R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF, $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$ See Figure 6-4	435		530	ns
		$t_{BIT(TXD)}$ = 200ns		155		210	
		$t_{BIT(TXD)}$ = 125ns(1)		85		130	
$t_{BIT(RXD)}$	Bit time on RXD output pins	$t_{BIT(TXD)}$ = 500ns		400		550	
		$t_{BIT(TXD)}$ = 200ns		120		220	
		$t_{BIT(TXD)}$ = 125ns(1)		75		135	
Δt_{REC}	Receiver timing symmetry	$t_{BIT(TXD)}$ = 500 ns		-65		40	
		$t_{BIT(TXD)}$ = 200 ns		-40		15	
		$t_{BIT(TXD)}$ = 125 ns(1)		-40		10	

(1) Measured during characterization and not an ISO 11898-2:2016 parameter.

6 Parameter Measurement Information

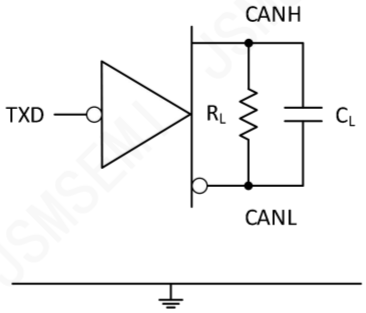


Figure 6-1. I_{CC} Test Circuit

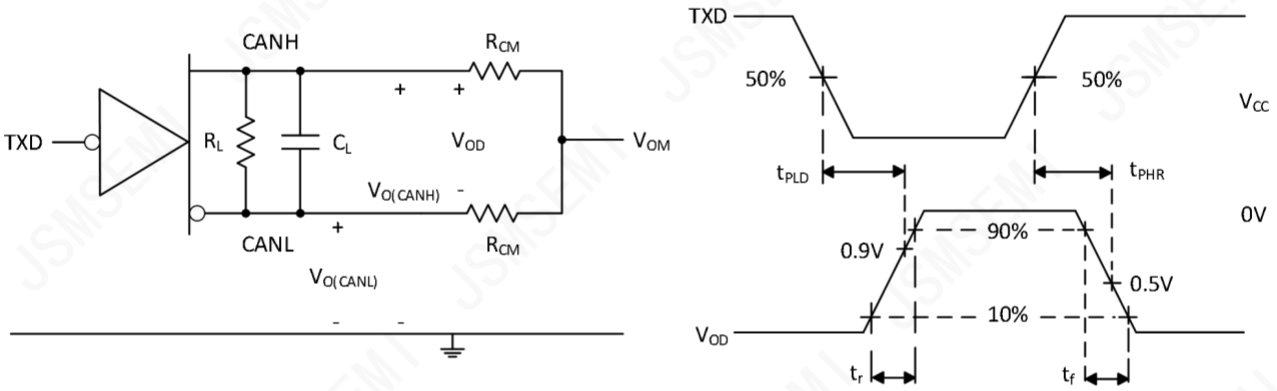


Figure 6-2.Driver Test Circuit and Measurement

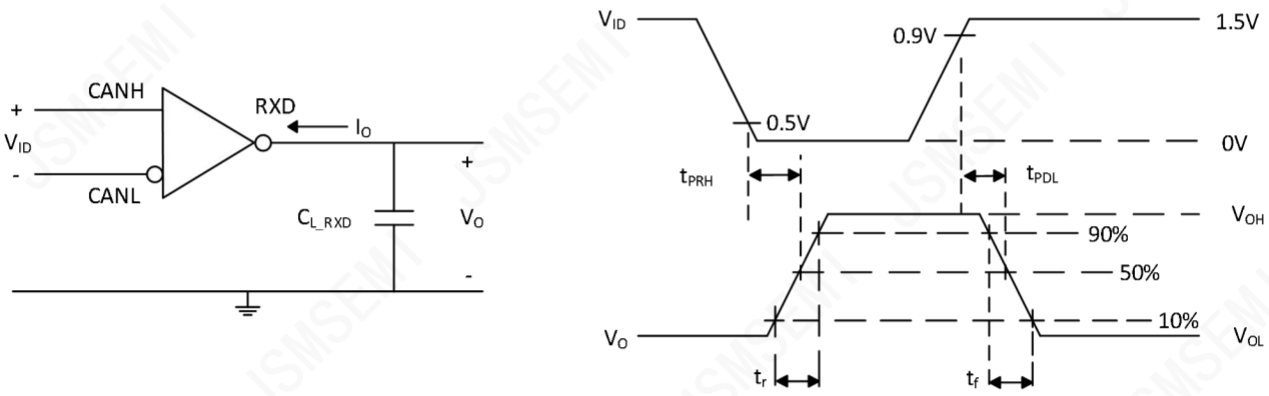


Figure 6-3. Receiver Test Circuit and Measurement

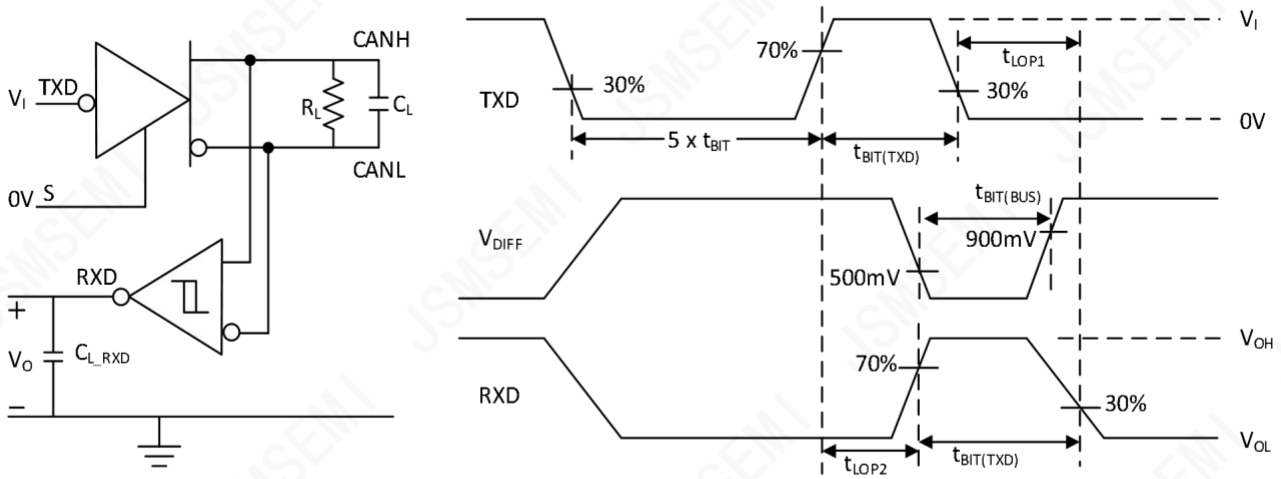


Figure 6-4. Transmitter and Receiver Timing Test Circuit and Measurement

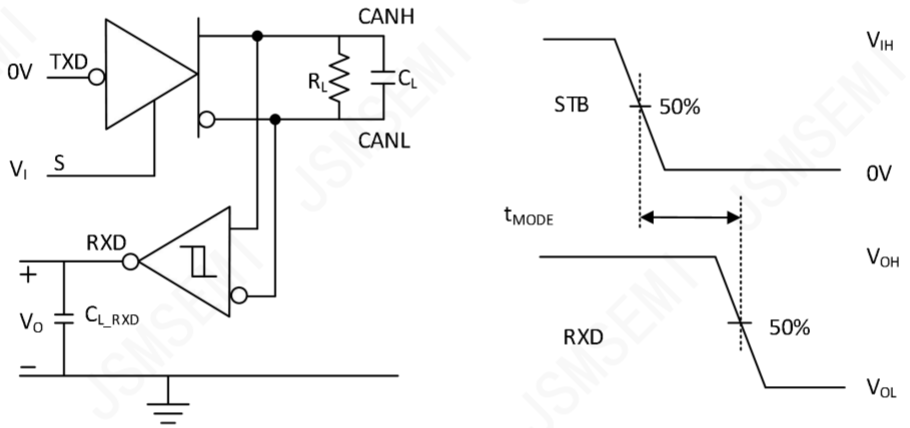


Figure 6-5. t_{MODE} Test Circuit and Measurement

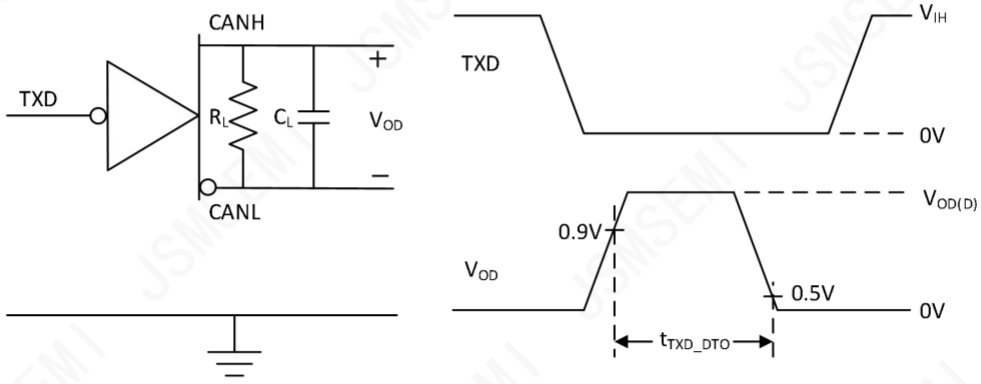


Figure 6-6. TXD Dominant Timeout Test Circuit and Measurement

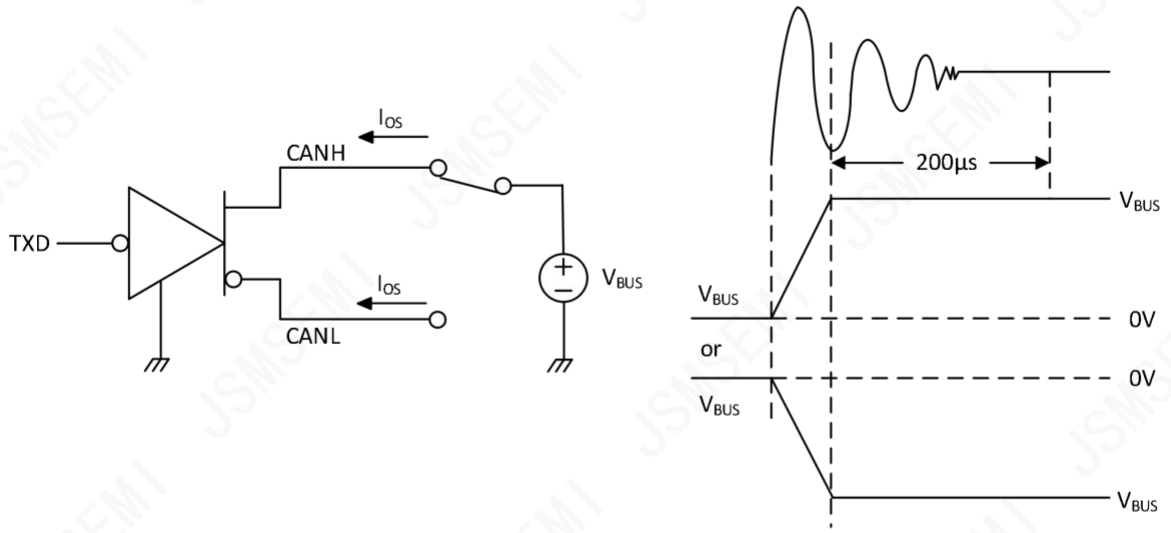


Figure 6-7. Driver Short Circuit Current Test and Measurement

7 Detailed Description

Overview

The TJA1044 devices meet or exceed the specifications of the ISO 11898-2:2016 high speed CAN (Controller Area Network) physical layer standard. The devices have been certified to the requirements of ISO 11898-2:2016 physical layer requirements according to the GIFT/ICT high speed CAN test specification. The transceivers provide a number of different protection features making them ideal for the stringent automotive system requirements while also supporting CAN FD data rates up to 8Mbps.

Feature Description

Pin Description

TXD

The TXD input is a logic-level signal, referenced to either V_{CC} or V_{IO} from a CAN controller to the transceiver.

GND

GND is the ground pin of the transceiver. The pin must be connected to the PCB ground.

V_{CC}

V_{CC} provides the 5V power supply to the CAN transceiver.

RXD

RXD is the logic-level signal, referenced to either V_{CC} or V_{IO}, from the TJA1044 to a CAN controller. This pin is only driven once V_{IO} is present.

V_{IO}

The V_{IO} pin provides the digital I/O voltage to match the CAN controller voltage thus avoiding the requirement for a level shifter. It supports voltages from 1.7V to 5.5V providing the widest range of controller support.

CANH and CANL

The CANH and CANL pins are the CAN high and CAN low differential bus pins. These pins are internally connected to the CAN transmitter, receiver and the low-power wake-up receiver.

STB (Standby)

The STB pin is an input pin used for mode control of the transceiver. The STB pin can be supplied from either the system processor or from a static system voltage source. If normal mode is the only intended mode of operation, the STB pin can be tied directly to GND.

CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 7-2 and Figure 7-3.
A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors (RIN) of the receiver and corresponds to a logic high on the TXD and RXD pins.
A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.
The TJA1044 transceiver implements a low-power standby (STB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high resistance internal resistors of the receiver. See Figure 7-2 and Figure 7-3.

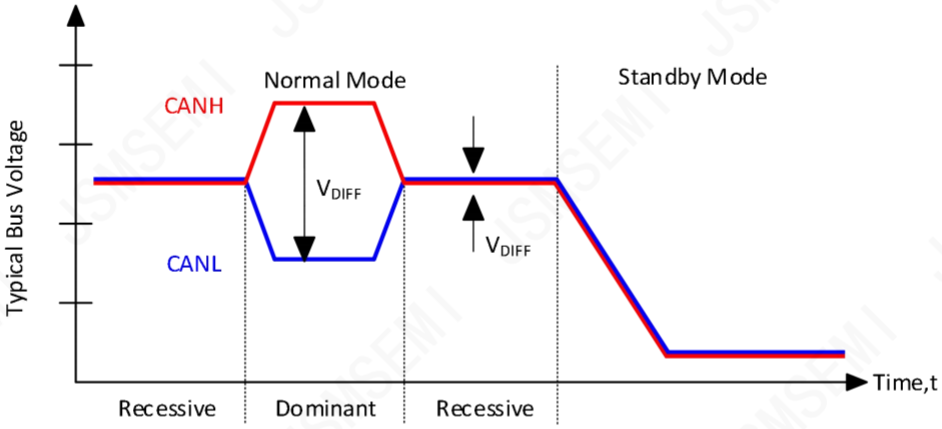
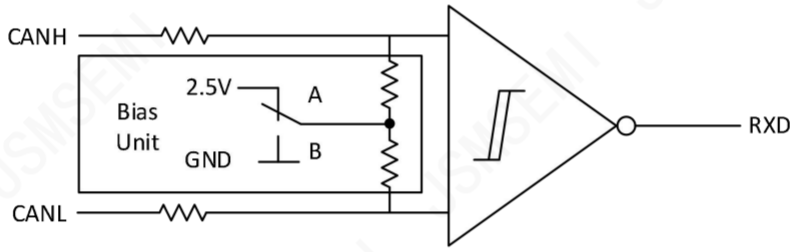


Figure 7-2. Bus States



A: A - Normal Mode
B: B - Standby Mode

Figure 7-3. Simplified Recessive Common Mode Bias Unit and Receiver

TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin, thus clearing the dominant time out. The receiver remains active and biased to $V_{CC}/2$ and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.
The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using Equation 1.

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD\_DTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2\text{kbps} \quad (1)$$

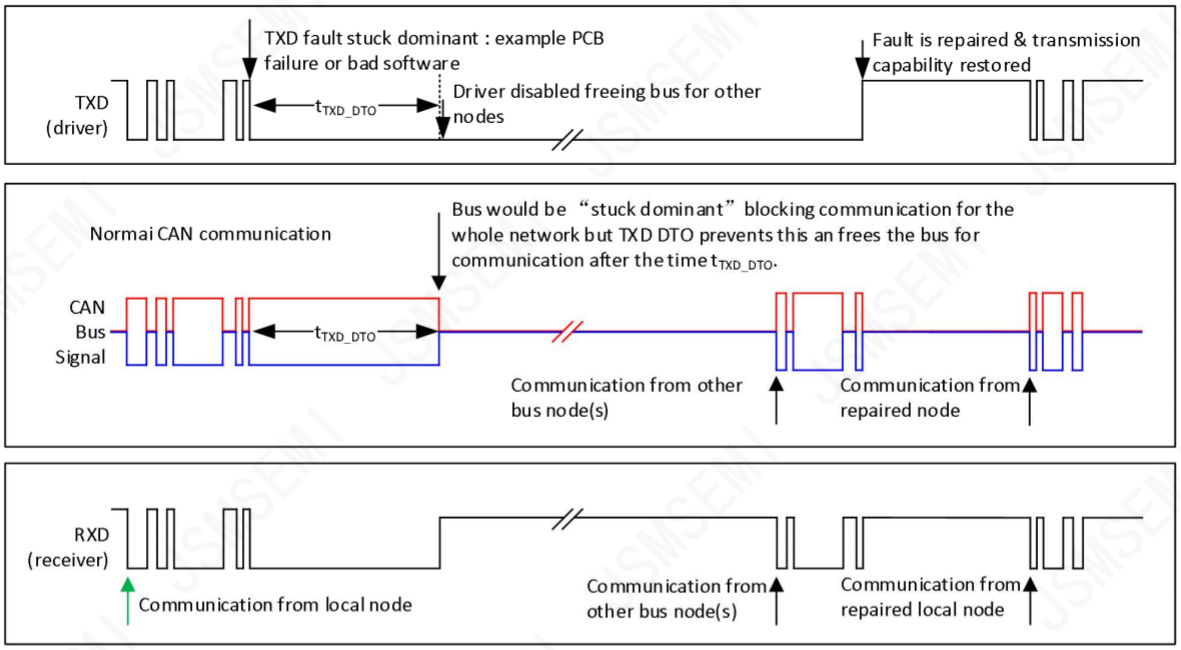


Figure 7-4. Example Timing Diagram for TXD DTO

Thermal Shutdown (TSD)

If the junction temperature of the TJA1044 exceeds the thermal shutdown threshold, T_{TSD}, the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD}. The CAN bus pins are biased to $V_{CC}/2$ during a TSD fault and the receiver to RXD path remains operational. The TJA1044 TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

Undervoltage Lockout

The supply pins, V_{CC} and V_{IO}, have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

Table 7-1. Undervoltage Lockout only Devices without V_{IO} pin

V_{CC}	Device State	Bus	RXD Pin
> UV_{VCC}	Normal	Per TXD	Mirrors Bus
< UV_{VCC}	Protected	High Impedance	High Impedance

Table 7-2. Undervoltage Lockout only Devices with V_{IO} pin

V_{CC}	V_{IO}	Device State	Bus Output	RXD Pin
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors Bus
< UV_{VCC}	> UV_{VIO}	STB = High: Standby Mode	Weak biased to GND	V_{IO}: Remote wake request See Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode
		STB =Low: Protected Mode	High Impedance	Recessive
> UV_{VCC}	< UV_{VIO}	Protected	High Impedance	High Impedance
< UV_{VCC}	< UV_{VIO}	Protected	High Impedance	High Impedance

Once the undervoltage condition is cleared and t_{MODE} has expired the TJA1044 will transition to normal mode and the host controller can send and receive CAN traffic again

Unpowered Device

The TJA1044 is designed to be an ideal passive or no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, so they do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.
The logic pins also have low leakage currents when the device is unpowered, so they do not load other circuits which may remain powered.

Floating Terminals

The TJA1044 has internal pull-ups on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.
When a CAN controller supporting open-drain outputs is used an adequate external pull-up resistor must be chosen. This ensures that the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See Table 7-3 for details on pin bias conditions.

Table 7-3. Pin Bias

Pin	Pull-up or Pull-down	Comment
TXD	Pull-up	Weakly biases TXD towards recessive to prevent bus blockage or TXD DTO triggering
STB	Pull-up	Weakly biases STB towards low-power standby mode to prevent excessive system power

Device Functional Modes

Operating Modes

The TJA1044 has two main operating modes; normal mode and standby mode. Operating mode selection is made by applying a high or low level to the STB pin.

Table 7-4. Operating Modes

STB	Device Mode	Driver	Receiver	RXD Terminal
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received See Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode
Low	Normal Mode	Disabled	Disabled	Mirrors bus state

Normal Mode

This is the normal operating mode of the TJA1044. The CAN driver and receiver are fully operational and CAN communication is bi-directional.
The driver is translating a digital input on the TXD input to a differential output on the CANH and CANL bus pins.
The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD output.

Standby Mode

This is the low-power mode of the TJA1044. The CAN driver and main receiver are switched off and bi-directional CAN communication is not possible. The low-power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. A wake-up request is output to RXD as shown in Figure 7-5.Pin RXD follows the bus after a wake-up request has been detected and the device will be reactivated to normal mode by pulling the STB pin low again. The CAN bus pins are weakly pulled to GND in this mode. The CAN bus pins are weakly pulled to GND in this mode; See Figure 7-2 and Figure 7-3.
In standby mode, only the V_{IO} supply is required therefore the V_{CC} may be switched off for additional system level current savings.

Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The TJA1044 supports a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2016 standard to qualify bus activity. Once a valid WUP has been received, the wake request is indicated to the controller by a falling edge and low period corresponding to a filtered dominant on the RXD output of the TJA1044.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. The first filtered dominant initiates the WUP, and the bus monitor then waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received the bus monitor is waiting for a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon reception of the second filtered dominant the bus monitor recognizes the WUP and drives the RXD output low every time an additional filtered dominant signal is received from the bus.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP and thus no wake request is generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a wake-up request may be generated. Bus state times greater than $t_{WK\_FILTER(MAX)}$ are always detected as part of a WUP, and thus a wake request is always generated. See Figure 7-5 for the timing diagram of the wake-up pattern.

The pattern and t_{WK_FILTER} time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any valid message to initiate a wake-up request.

The ISO 11898-2:2016 standard has defined times for a short and long wake-up filter time. The t_{WK_FILTER} timing for the device has been picked to be within the minimum and maximum values of both filter ranges. This timing has been chosen such that a single bit time at 500kbps, or two back-to-back bit times at 1Mbps triggers the filter in either bus state. Any CAN frame at 500kbps or less would contain a valid WUP.

For an additional layer of robustness and to prevent false wake-ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value $t \leq t_{WK\_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in its current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See Figure 7-5 for the timing diagram of the wake-up pattern with wake timeout feature.

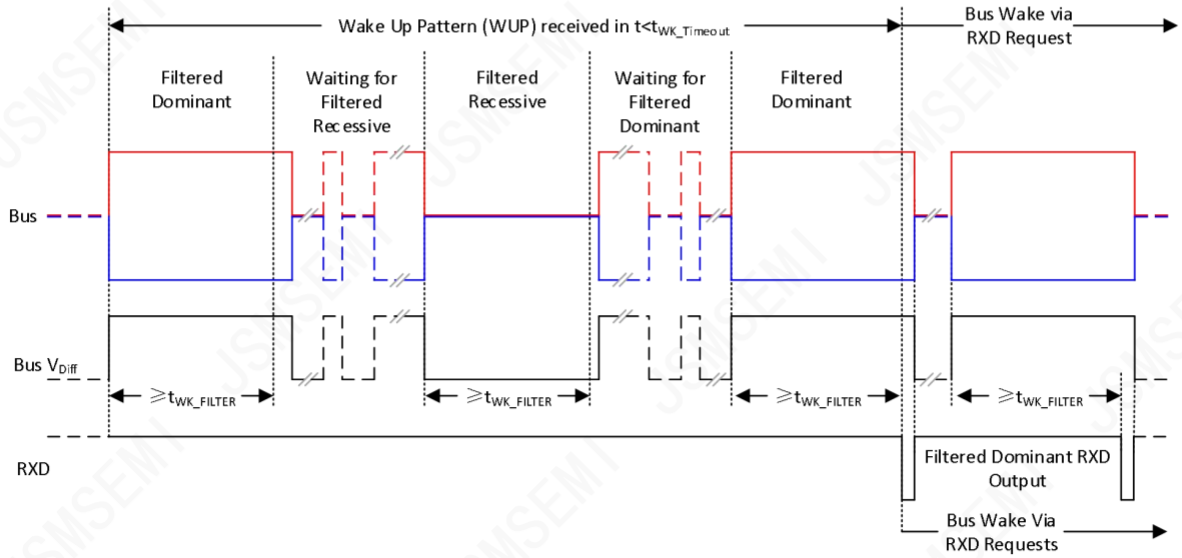


Figure 7-5. Wake-Up Pattern (WUP) with $t_{WK\_TIMEOUT}$

Driver and Receiver Function

The TJA1044 logic I/Os support CMOS levels with respect to either V_{CC} for 5V systems or V_{IO} for compatibility with MCUs that support 2.5V, 3.3V, or 5V systems.

Table 7-5. Driver Function Table

Device Mode	TXD Input(1)	Bus Outputs		Driven Bus State(2)
		CANH	CANL	
Normal	Low	High	Low	High impedance
	High or open	High impedance	High impedance	Biased recessive
Standby	X	High impedance	High impedance	Biased to ground

(1) X = irrelevant
(2) For bus state and bias see Figure 7-2 and Figure 7-3

Table 7-6. Receiver Function Table Normal and Standby Mode

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Pin
Normal	$V_{ID} \geq 0.9$ V	Dominant	Low
	0.5 V < V_{ID} < 0.9 V	Undefined	Undefined
	$V_{ID} \leq 0.5$ V	Recessive	High
Standby	$V_{ID} \geq 1.15$ V	Dominant	High Low if a remote wake event occurred See Figure 7-5
	0.4 V < V_{ID} < 1.15 V	Undefined	
	$V_{ID} \leq 0.4$ V	Recessive	
Any	Open ($V_{ID} \approx 0$ V)	Open	High

8 Application and Implementation

Typical Applications

The TJA1044 transceiver can be used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. Figure 8-1 shows a typical configuration for 5V controller applications. The bus termination is shown for illustrative purposes.

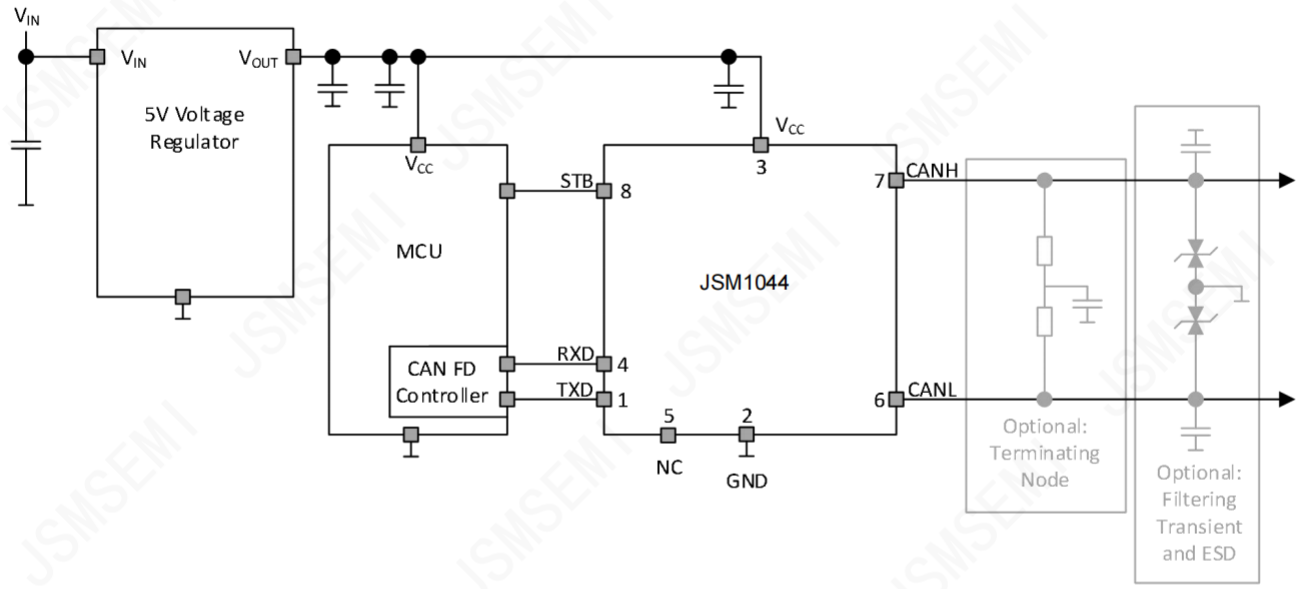


Figure 8-1. Transceiver Application Using 5V IO Connections

Design Requirements

CAN Termination

Termination may be a single 120Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination may be used, see Figure 8-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

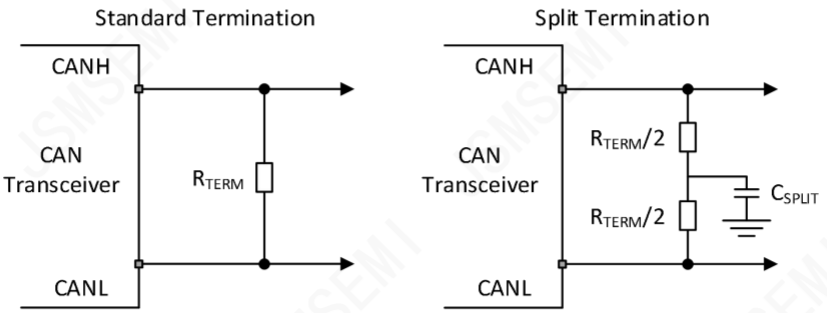


Figure 8-2. CAN Bus Termination Concepts

Detailed Design Procedures

Bus Loading, Length and Number of Nodes

The ISO 11898-2 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the TJA1042 family of transceivers.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2. They have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, DeviceNet and NMEA2000.

The TJA1044 family is specified to meet the 1.5V requirement with a 50Ω load, incorporating the worst case including parallel transceivers. The differential input resistance of the TJA1044 family is a minimum of 30kΩ. If 100 TJA1044 family transceivers are in parallel on a bus, this is equivalent to a 300Ω differential load worst case. That transceiver load of 300Ω in parallel with the 60Ω gives an equivalent loading of 50Ω. Therefore, the TJA1042 family theoretically supports up to 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. In using this flexibility comes the responsibility of good network design and balancing these tradeoffs.

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TJA1044

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification the driver differential output is specified with a bus load that can range from 50Ω to 65Ω where the differential output must be greater than 1.5V. The TJA1044 family is specified to meet the 1.5V requirement down to 50Ω and is specified to meet 1.4V differential output at 45Ω bus load. The differential input resistance of the TJA1044 is a minimum of 40kΩ. If 100 TJA1044 transceivers are in parallel on a bus, this is equivalent to a 400Ω differential load in parallel with the nominal 60Ω bus termination which gives a total bus load of approximately 52Ω. Therefore, the TJA1044 family theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets, and signal integrity thus a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design to ensure robust network operation.

Please refer to the application report SLLA270: Controller Area Network Physical layer requirements. This document discusses in detail all system design physical layer parameters.

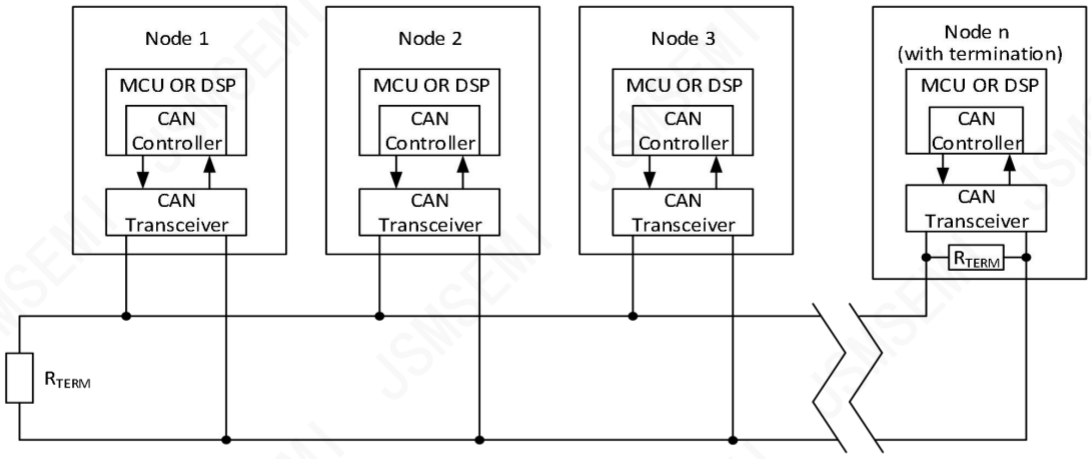


Figure 8-3. Typical CAN Bus

System Examples

The TJA1044 CAN transceiver is typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. A 2.5V, or 3.3V application is shown in Figure 8-4. The bus termination is shown for illustrative purposes.

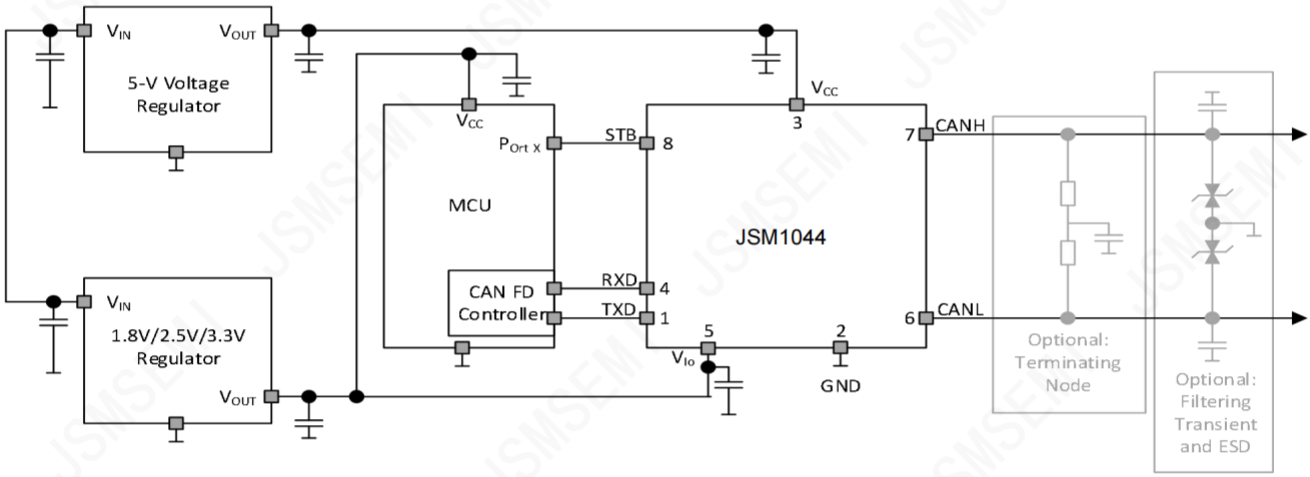


Figure 8-4. Typical CAN Bus Application Using 3.3V CAN Controller

9 Power Supply Recommendations

The TJA1044 transceiver is designed to operate with a main V_{CC} input voltage supply range between 4.5V and 5.5V. The TJA1044 implements an IO level shifting supply input, V_{IO}, designed for a range between 2.5V and 5.5V. Both the V_{CC} and V_{IO} inputs must be well regulated. In addition to the power supply filtering a decoupling capacitance, typically 100nF, should be placed near the CAN transceiver's main V_{CC} and V_{IO} supply pins.

10 Layout

Robust and reliable bus node design often requires the use of external transient protection device in order to protect against EFT and surge transients that may occur in industrial environments. Because ESD and transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design. The family comes with high on-chip IEC ESD protection, but if higher levels of system level immunity are desired external TVS diodes can be used. TVS diodes and bus filtering capacitors should be placed as close to the on-board connectors as possible to prevent noisy transient events from propagating further into the PCB and system.

Layout Guidelines

● Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. In this layout example a transient voltage suppression (TVS) device, D1, has been used for added protection. The production solution can be either bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C4 and C5. Additionally (not shown) a series common mode choke (CMC) can be placed on the CANH and CANL lines between the transceiver U1 and connector J1.

● Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.

● Use supply (V_{CC}) and ground planes to provide low inductance.

● Use at least two vias for supply (V_{CC}) and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

● Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver,

● examples are C1, C2 on the V_{CC} supply and C6 and C7 on the V_{IO} supply.

● Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R6 and R7, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to ensure the terminating node is not removed from the bus thus also removing the termination. See the application section for information on power ratings needed for the termination resistor(s).

● To limit current of digital lines, serial resistors may be used. Examples are R2, R3, and R4. These are not required.

● Terminal 1: R1 is shown optionally for the TXD input of the device. If an open drain host processor is used, this is mandatory to ensure the bit timing into the device is met.

● Terminal 5: For devices in this series with V_{IO} ports, bypass capacitors should be placed as close to the pin as possible (example C6 and C7). For device options without V_{IO} I/O level shifting, this pin is not internally connected and can be left floating or tied to any existing net, for example a split pin connection.

● Terminal 8: is shown assuming the mode terminal, STB, will be used. If the device will only be used in normal mode, R4 is not needed and R5 could be used for the pull down resistor to GND.

Layout Example

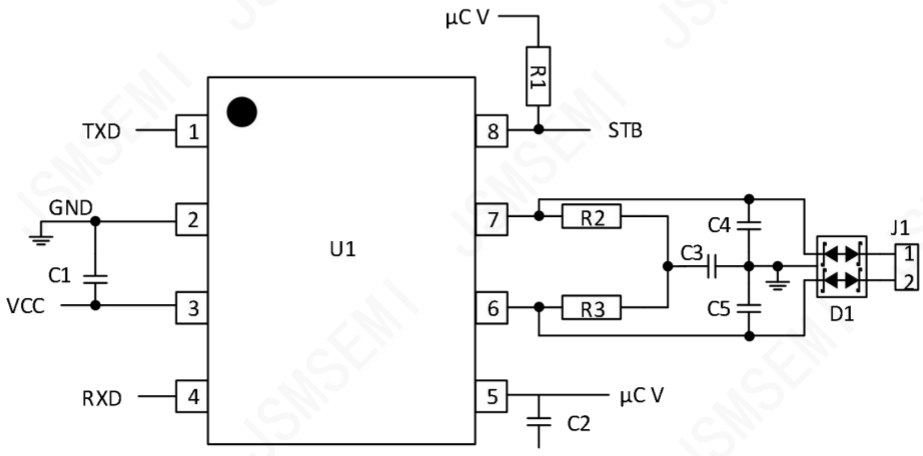
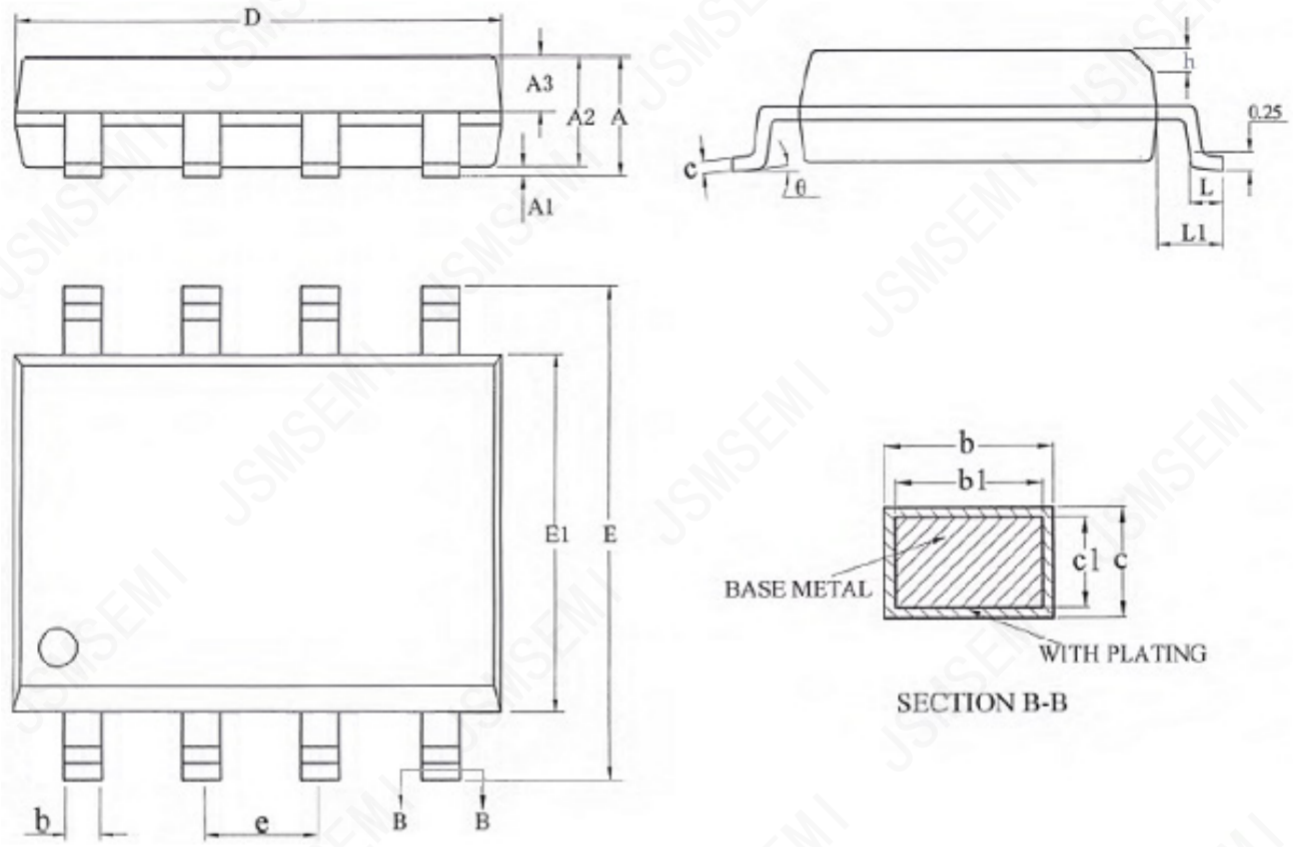


Figure 10-1. Layout Example

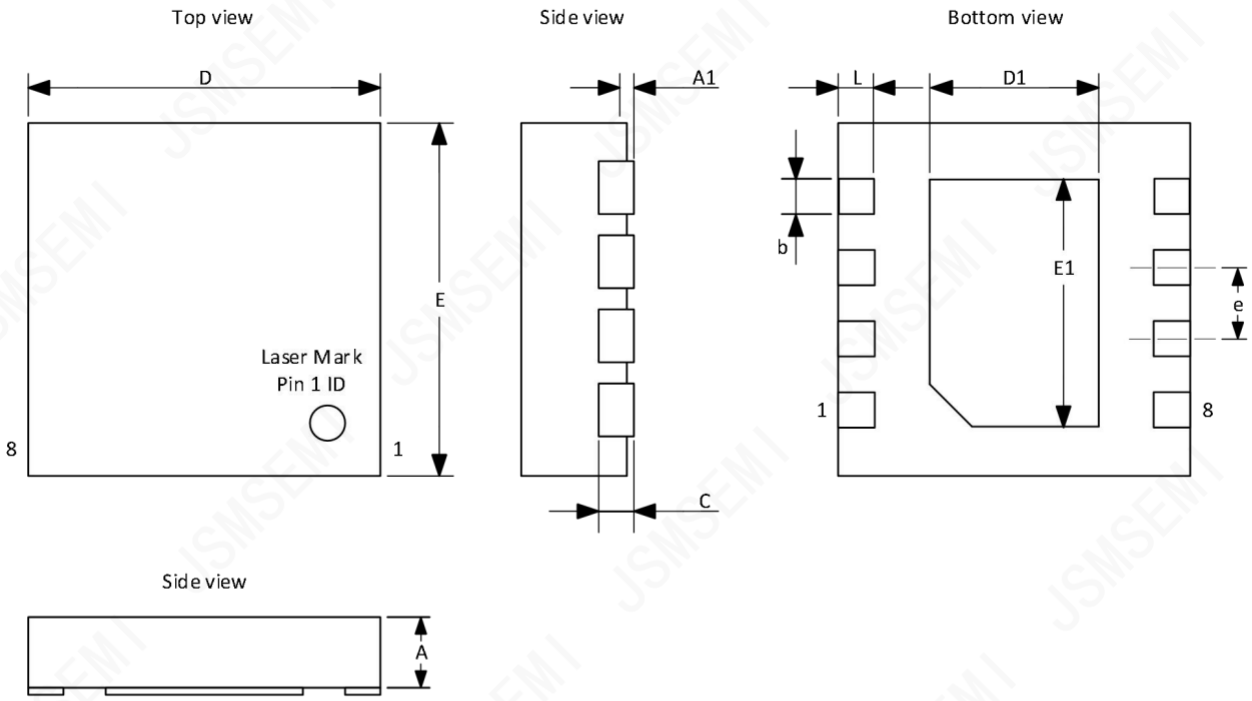
SOP8 Package Outlines



SOIC-8 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e		1.27BSC	
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L		0.50	
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

DFN8-EP(3x3)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
b	0.23	0.28	0.33
c		0.203REF	
D	2.925	3.00	3.075
D1	1.40	1.50	1.60
E	2.925	3.00	3.075
E1	2.20	2.30	2.40
e		0.650BSC	
L	0.25	0.30	0.35

Revision History

Rev.	Change	Date
V1.0	First-generation version	4/25/2023

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