Low Cost Low Power Instrumentation Amplifier

FEATURES

- Easy to use

  External resistance setting gain (1 to 10,000)

  Wide supply voltage range (±2V to ±19V)

  Higher performance compared to 3 OP-amp class instrument amplifiers

  8-PIN SOP package

  Low power consumption, 1.3mA static current

- Excellent DC performance

  Max. ±20μV, input offset voltage Max. 2.0nA, input bias current

  Minimum 108dB common-mode rejection ratio (G = 10)

- Low noise

  17nV/$\sqrt{\text{Hz}}$@1kHz, input noise voltage

  1.8μVPP (0.1Hz to 10Hz)

- Excellent AC performance

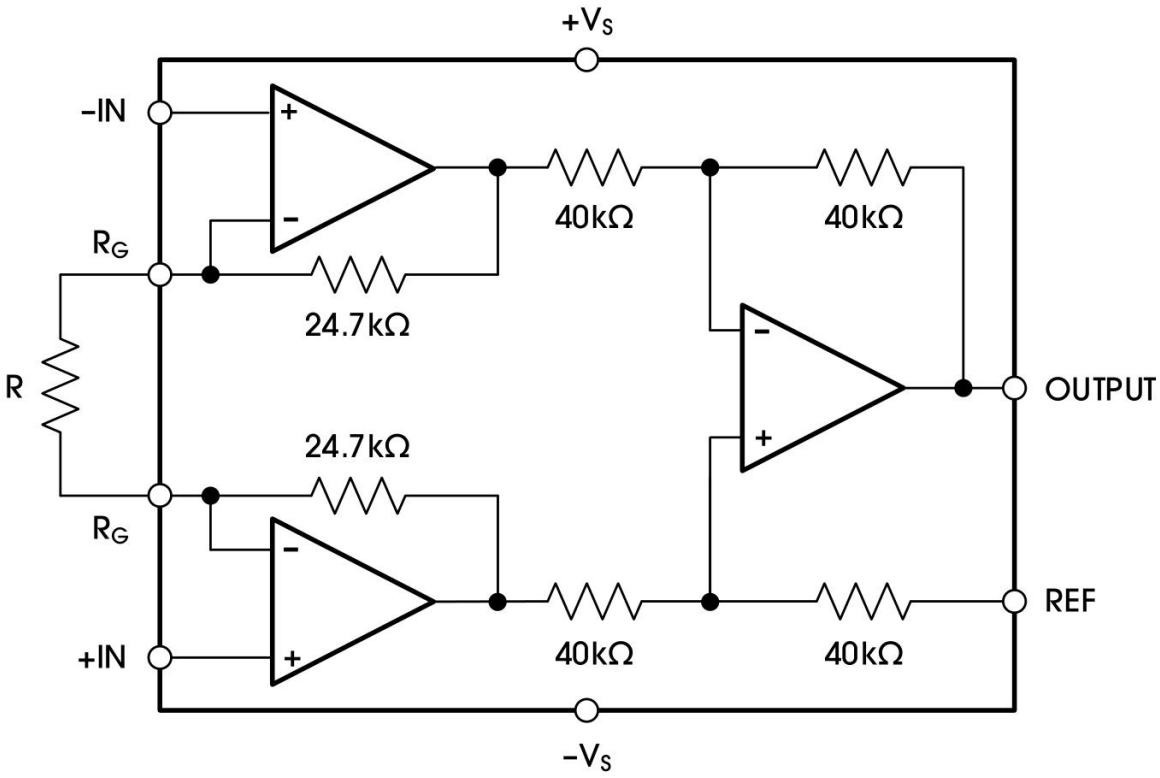
  2038kHz bandwidth (G = 1)

- Operating temperature

  - 40°C to 85°C

APPLICATION

- Measuring instruments
- ECG and medical applications
- Sensor interface
- Data acquisition system
- Industrial process control
- Batteries and mobile devices


+VS
–IN
RG
R
RG
+IN
24.7kΩ
24.7kΩ
40kΩ
40kΩ
40kΩ
40kΩ
OUTPUT
REF
–VS

PIN CONFIGURATIONS AND FUNCTIONS

Figure 1 illustrates the pin configuration.

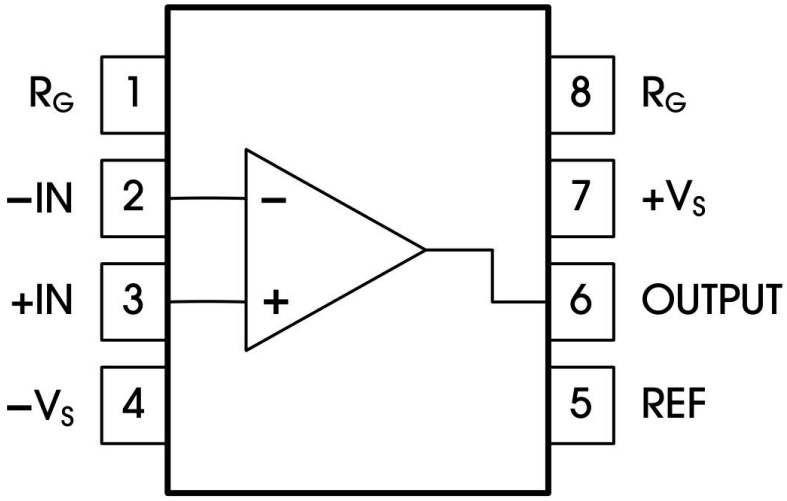


Figure 1. Pin Configuration

Table 3 lists the pin functions.

Table 3. Pin Functions

POSITION INA129UA/2K5	NAME	TYPE	DESCRIPTION
1, 8	R_G	Analog output	Connect a resistor between two R_G to set gain. See more information in the GAIN SELECTION section.
2	-IN	Analog input	Signal negative input
3	+IN	Analog input	Signal positive input
4	$-V_S$	Power supply	Negative power supply
5	REF	Analog input	Output reference voltage input
6	OUTPUT	Analog output	Output
7	$+V_S$	Power supply	Positive power supply

SPECIFICATIONS

Absolute Maximum Ratings

Table 4 lists the absolute maximum ratings of the INA129UA/2K5

Table 4. Absolute Maximum Ratings

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
Voltage	Supply		±20	V
	Input voltage	$-V_S$ - 0.3	$+V_S$ + 0.3	V
Current	Any pin except power supply	−10	+10	mA
Output Short-Circuit Duration		Indefinite		
Temperature	Operating, T_A	-40	85	°C
	Storage, T_{stg}, Q	-65	150	
	Soldering, 10s		300	

Note: Stresses beyond those listed under Table 4 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 6. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ESD Ratings

Table 5 lists the ESD ratings of the INA129UA/2K5

Table 5. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

Note 1: The JEDEC document JEP155 indicates that 500V HBM allows safe manufacturing with a standard ESD control process.

Note 2: The JEDEC document JEP157 indicates that 250V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Table 6 lists the recommended operating conditions for the INA129UA/2L5

Table 6. Recommended Operating Conditions

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNITS
Operating Voltage Range	Split supply	±2.25	±18	±19	V
	Single supply	4.5	36	38	V
Specified Temperature Range		-40		85	°C

Thermal information

Table 7 lists the thermal information for the INA129UA/2K5

Table 7. Thermal Information

PARAMETER	SYMBOL	SOP-8	UNITS
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	145	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	83.3	°C/W
Junction-to-Top Characterization Parameter	ψ_{JT}	1.7	°C/W
Junction-to-Board Characterization Parameter	ψ_{JB}	81.7	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC(top)}$	48.3	°C/W

Electrical Characteristics

Table 8 lists the electrical characteristics of INA129 Typical at 25°C, VS = ±18V, and RL = 2kΩ to GND, unless otherwise noted.

Table 8. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GAIN						
Gain Range		G = 1 + (49.4kΩ / R_G)	1		10K	
Gain Error(1)		V_{OUT} = ±10V, G = 1		0.2	0.2	%
		V_{OUT} = ±10V, G = 10		0.3	0.4	%
		V_{OUT} = ±10V, G = 100		0.3	0.7	%
		V_{OUT} = ±10V, G = 1000		0.3	0.5	%
Nonlinearity		V_{OUT} = −10V to +10V, G = 1, R_L = 10kΩ		0.8		ppm
		V_{OUT} = −10V to +10V, G = 10, R_L = 10kΩ		8		ppm
		V_{OUT} = −10V to +10V, G = 100, R_L = 10kΩ		15		ppm
		V_{OUT} = −10V to +10V, G = 1000, R_L = 10kΩ		30		ppm
Gain vs. Temperature		G = 1(5)		0.15	0.4	ppm/°C
		Gain > 1(1)(5)		9	32	ppm/°C
VOLTAGE OFFSET(2)						
Input Offset, V_{OSI}		V_S = ±18V		±4	±20	μV
		V_S = ±2V to ±19V, overtemperature(5)			±45	μV
		V_S = ±2V to ±19V, average TC(5)		±0.1		μV/°C
Output Offset, V_{OSO}		V_S = ±18V		±130	±300	μV
		V_S = ±2V to ±19V, overtemperature(5)			±450	μV
		V_S = ±2V to ±19V, average TC(5)		±0.4		μV/°C
Offset Referred to The Input vs. Supply (PSR)		V_S = ±2V to ±20V, G = 1	104	111		dB
		V_S = ±2V to ±20V, G = 1, overtemperature(5)	100			dB
		V_S = ±2V to ±20V, G = 10	123	131		dB
		V_S = ±2V to ±20V, G = 10, overtemperature(5)	120			dB
		V_S = ±2V to ±20V, G = 100	130	147		dB
		V_S = ±2V to ±20V, G = 100, overtemperature(5)	130			dB
		V_S = ±2V to ±20V, G = 1000	130	156		dB
		V_S = ±2V to ±20V, G = 1000, overtemperature(5)	130			dB
INPUT CURRENT						
Input Bias Current				0.6	2	nA
		Overtemperature(5)			10	nA
Input Offset Current				0.1	1	nA
		Overtemperature(5)			4.0	nA
INPUT						
Input Impedance		Differential		34 ‖ 5		GΩ_pF
		Common-Mode		34 ‖		GΩ_pF

				6		
Input Voltage Range[3]		V_S = ±2V to ±19V	$-V_S$ + 0.1		$+V_S$ – 2	V
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Rejection Ratio DC		V_{CM} = (-V_S + 0.1V) to (+V_S - 2V), G = 1	88	148		dB
		V_{CM} = (-V_S + 0.1V) to (+V_S - 2V), G = 1, overtemp[5]	83			dB
		V_{CM} = (-V_S + 0.1V) to (+V_S - 2V), G = 10	108	161		dB
		V_{CM} = (-V_S + 0.1V) to (+V_S - 2V), G = 10, overtemp[5]	103			dB
		V_{CM} = (-V_S + 0.1V) to (+V_S - 2V), G = 100	129	163		dB
		V_{CM} = (-V_S + 0.1V) to (+V_S - 2V), G = 100, overtemp[5]	123			dB
		V_{CM} = (-V_S + 0.1V) to (+V_S - 2V), G = 1000	143	163		dB
		V_{CM} = (-V_S + 0.1V) to (+V_S - 2V), G = 1000, overtemp[5]	136			dB
Output Swing		R_L = 10kΩ, V_S = ±2V to ±19V, overtemperature[5]	$-V_S$ + 0.2		$+V_S$ - 0.3	V
Short Circuit Current		Overtemperature		±19		mA
Small Signal -3dB Bandwidth		G = 1		2038		kHz
		G = 10		417		kHz
		G = 100		53		kHz
		G = 1000		4		kHz
Slew Rate		G = 1, 10V step		2		V/µs
		G = 100, 10V step		1		V/µs
Voltage Noise, 1kHz[4]		Input, Voltage Noise, e_{ni}		17		nV/√Hz
		Output, Voltage Noise, e_{no}		63		nV/√Hz
RTI, 0.1Hz to 10Hz		G = 1		1.8		μV_{PP}
		G = 100		0.4		μV_{PP}
Current Noise		f = 1kHz		450		fA/√Hz
R_{IN}				80		kΩ
Voltage Range			$-V_S$		$+V_S$	V
Reference Gain to Output				10	41	µV/V
Operating Range			±2		±19	V
Quiescent Current		V_S = ±2V to ±19V		1.3	1.5	mA
Overtemperature					1.6	mA
For Specified Performance			-40		+125	°C

Detailed Description

TA = 25°C, VS = ±18V, RL = 2kΩ, unless otherwise noted.

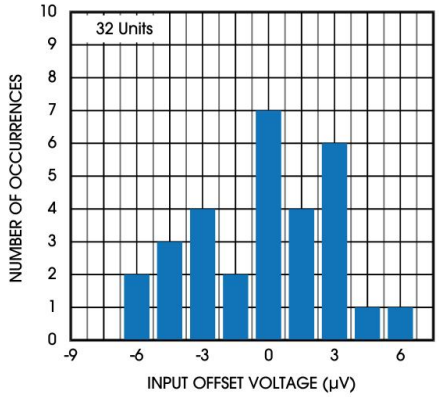


Figure 2. Typical Distribution of Input Offset Voltage

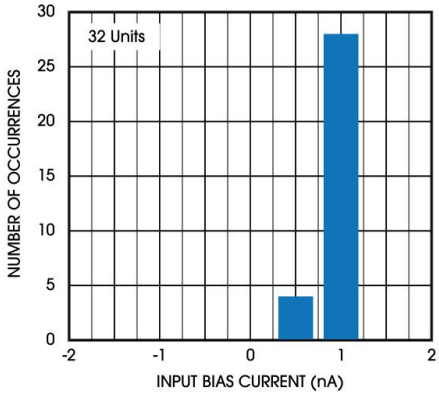


Figure 3. Typical Distribution of Input Bias Current

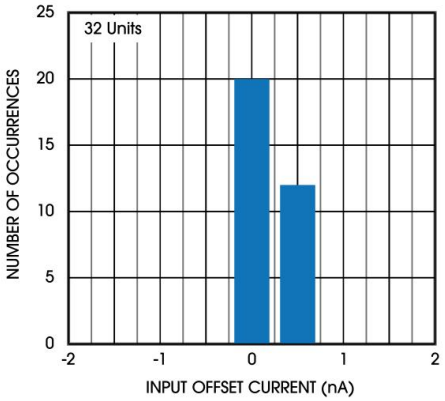


Figure 4. Typical Distribution of Input Offset Current

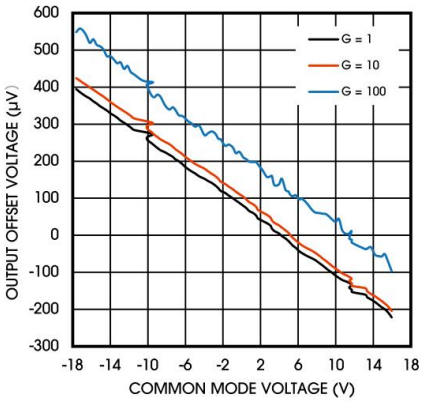


Figure 5. Input Offset Voltage vs. Common Mode Voltage

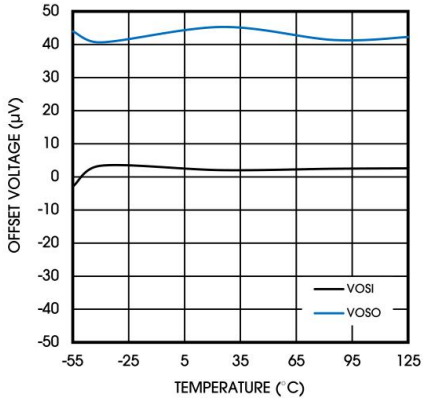


Figure 6. Input Offset Voltage vs. Temperature

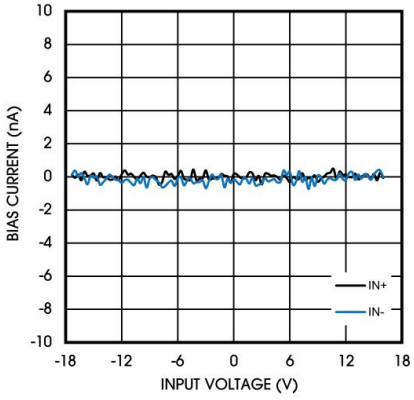


Figure 7. Input Bias Current vs. Common Mode Voltage (25°C)

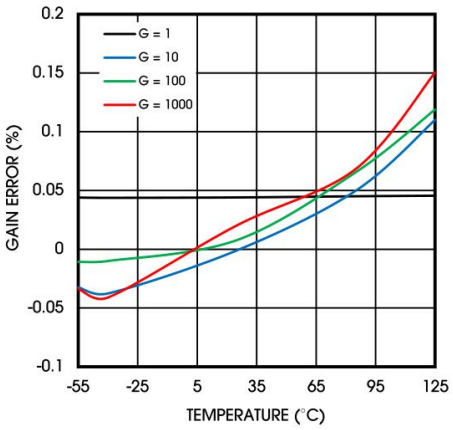


Figure 8. Gain vs. Temperature

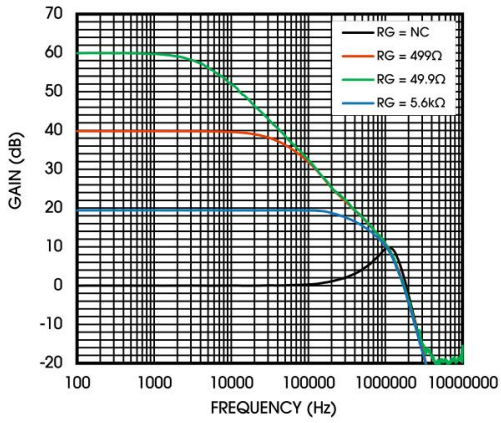


Figure 9. Gain vs. Frequency

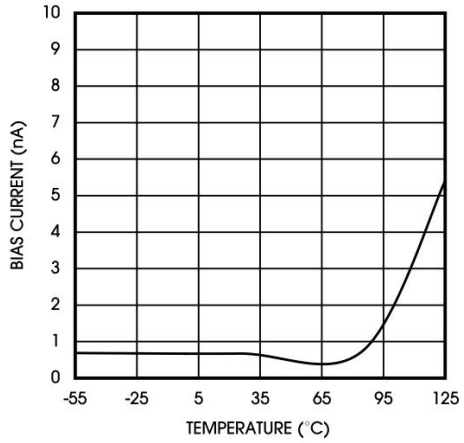


Figure 10. Bias Current vs. Temperature

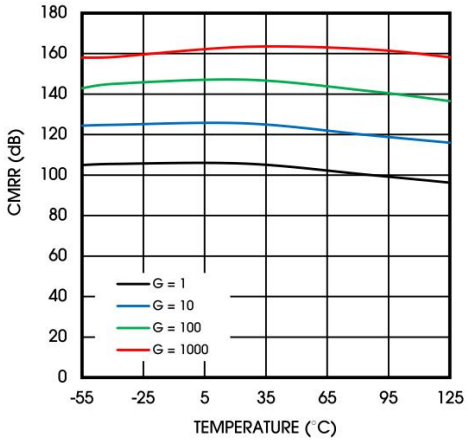


Figure 11. CMRR vs. Temperature

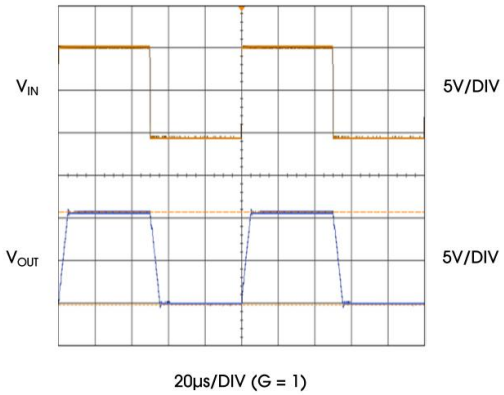


Figure 12. Large Signal Response (G = 1)

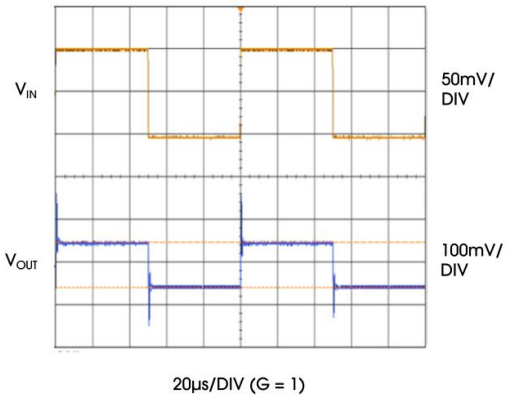


Figure 13. Small Signal Response (G = 1)

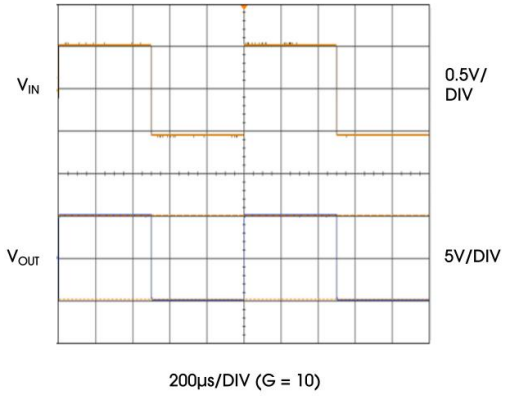


Figure 14. Large Signal Response (G = 10)

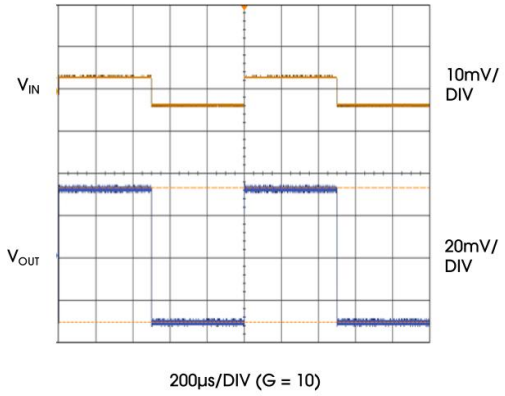


Figure 15. Small Signal Response (G = 10)

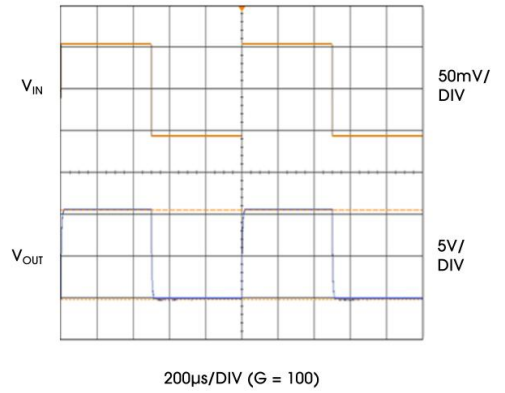


Figure 16. Large Signal Response (G = 100)

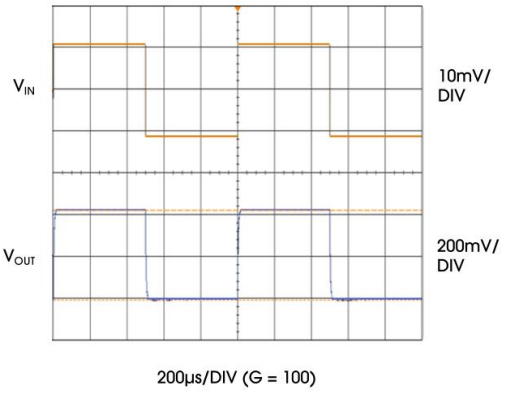


Figure 17. Small Signal Response (G = 100)

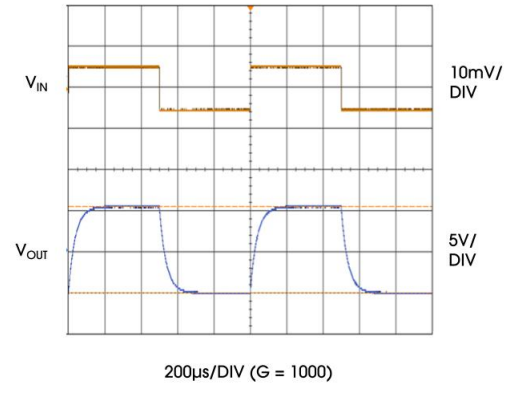


Figure 18. Large Signal Response (G = 1000)

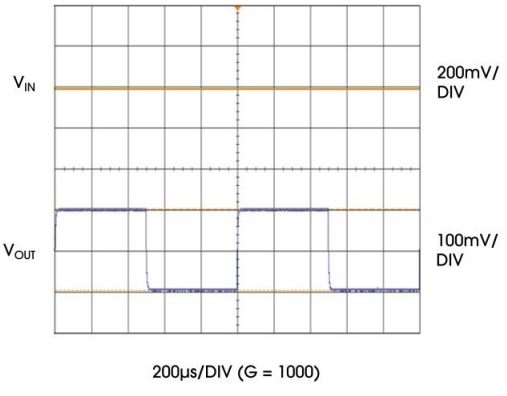


Figure 19. Small Signal Response (G = 1000)

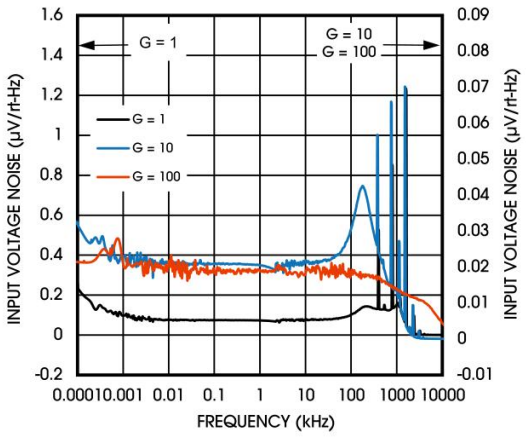


Figure 20. Input Voltage Noise Density

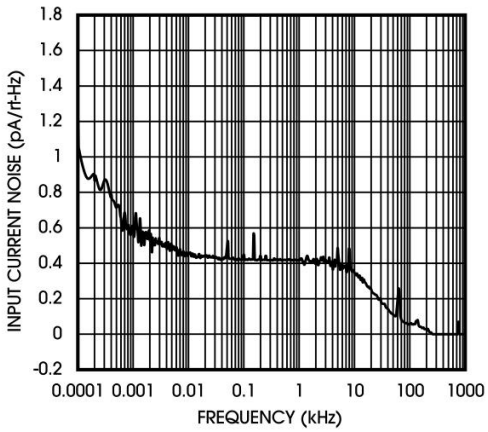


Figure 21. Input Current Noise Density

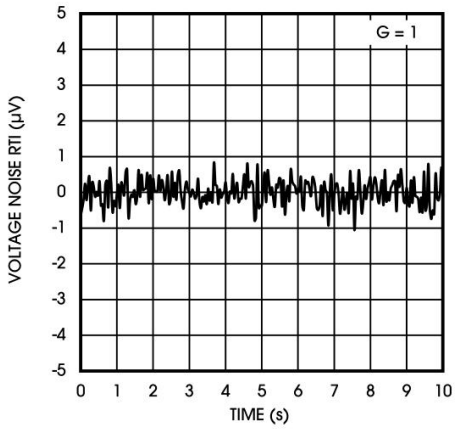


Figure 22. 0.1Hz to 10Hz RTI Voltage Noise

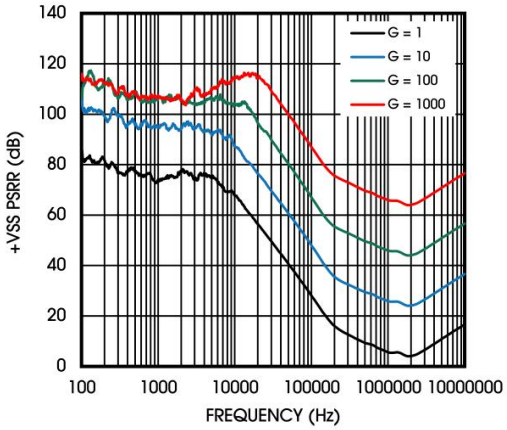


Figure 23. Positive PSR vs. Frequency

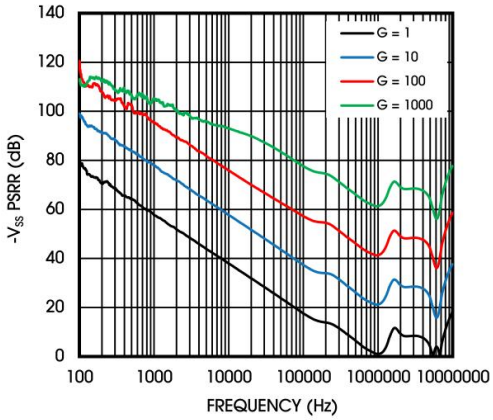


Figure 24. Negative PSR vs. Frequency

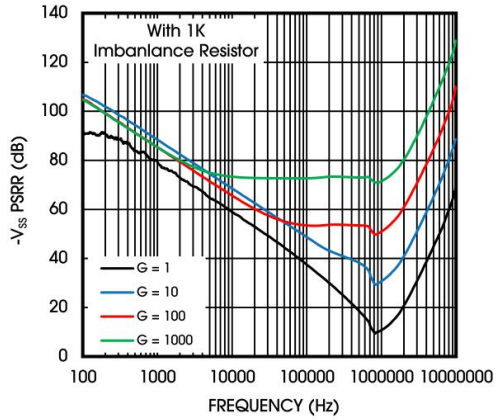


Figure 25. Imbalance CMRR vs. Frequency

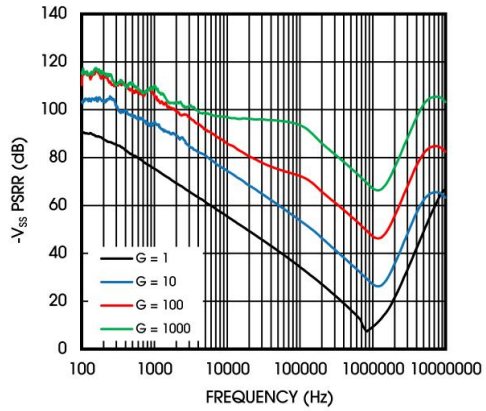


Figure 26. CMRR vs. Frequency

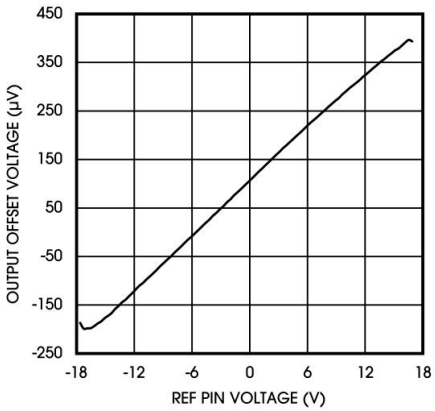


Figure 27. Reference Voltage vs. Output Offset Voltage

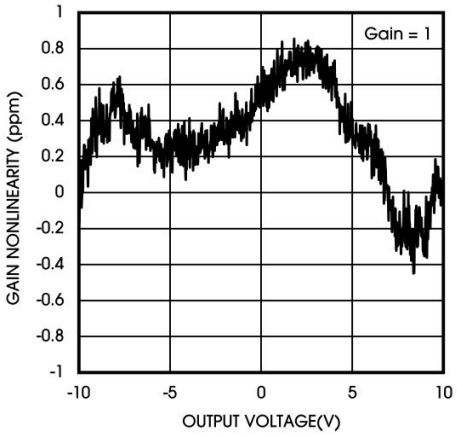


Figure 28. Gain Nonlinearity (G = 1)

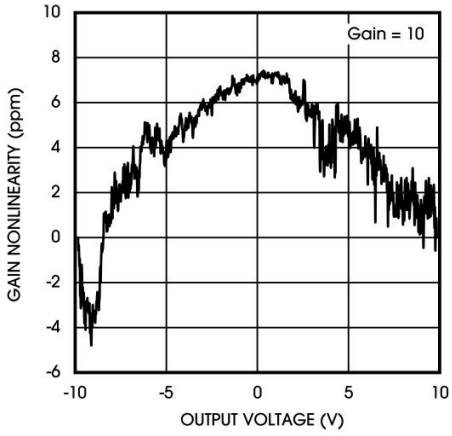


Figure 29. Gain Nonlinearity (G = 10)

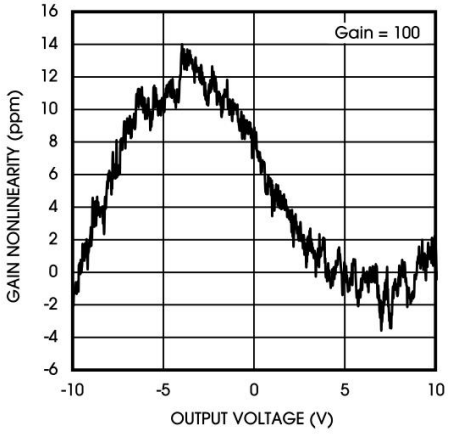


Figure 30. Gain Nonlinearity (G = 100)

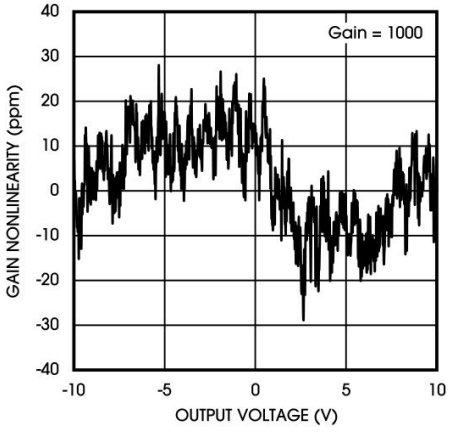


Figure 31. Gain Nonlinearity (G = 1000)

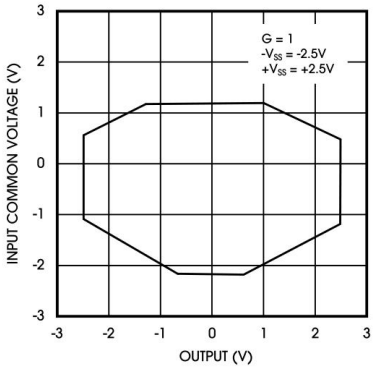


Figure 32. Input Common-Mode Range vs. Output Voltage, G = 1 (5V)

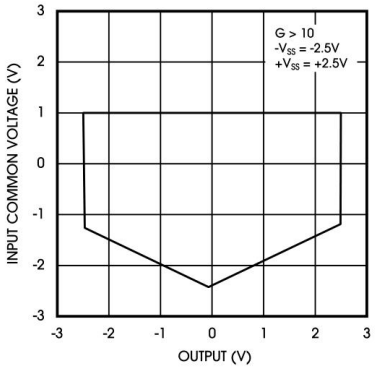


Figure 33. Input Common-Mode Range vs. Output Voltage, G > 10 (5V)

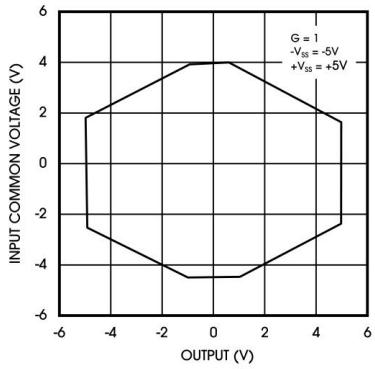


Figure 34. Input Common-Mode Range vs. Output Voltage, G = 1 (10V)

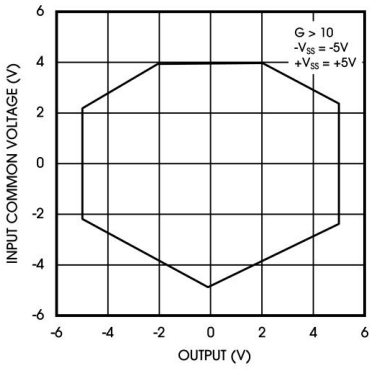


Figure 35. Input Common-Mode Range vs. Output Voltage, G > 10 (10V)

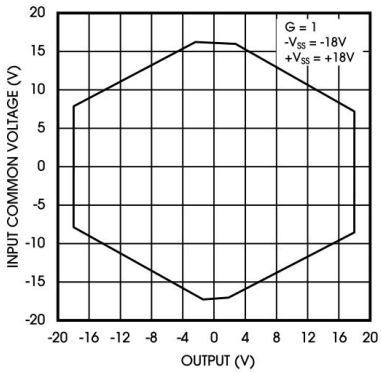


Figure 36. Input Common-Mode Range vs. Output Voltage, G = 1 (36V)

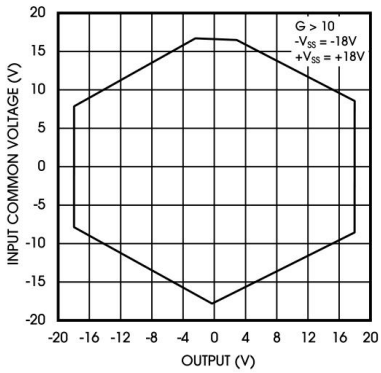


Figure 37. Input Common-Mode Range vs. Output Voltage, G > 10 (36V)

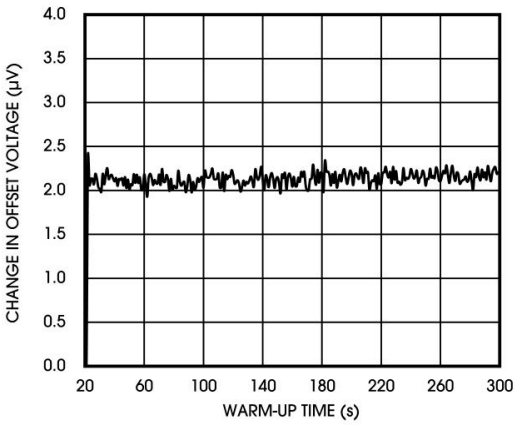


Figure 38. Warm-Up Time

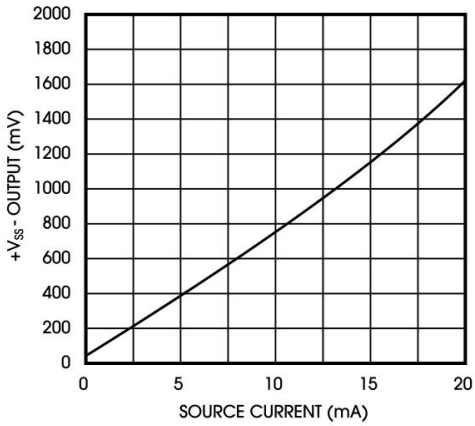


Figure 39. V_{OH} vs. Source Current

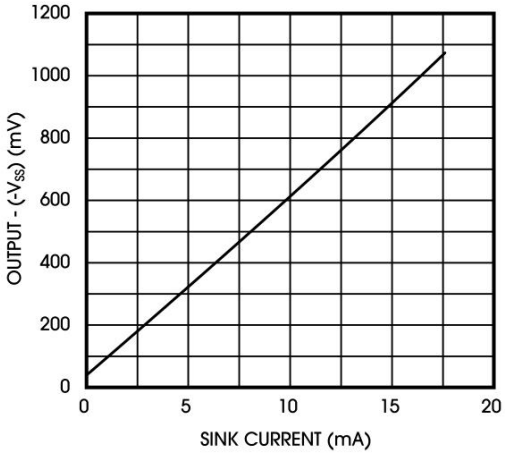


Figure 40. V_{OL} vs. Sink current

DETAILED DESCRIPTION

Summarize

The INA129 is an improved monolithic instrument amplifier based on the classical three-op amplifier approach. Absolute value fine-tuning allows the user to accurately set the gain with just one resistor. The monolithic structure and fine-tuning allow for close matching and tracking of circuit elements, thus ensuring the inherent high performance of the circuit.

The internal gain resistors R1 and R2 are adjusted to an absolute value of 24.7kΩ, allowing the gain to be precisely programmed using a single external resistor. Then the gain equation is:

$$G = \frac{49.4k\Omega}{R_G} + 1$$

$$R_G = \frac{49.4k\Omega}{G - 1}$$

As a single-ended output for reference REF pins, REF pins can be connected to ground or low resistance sources.

Functional module block diagram

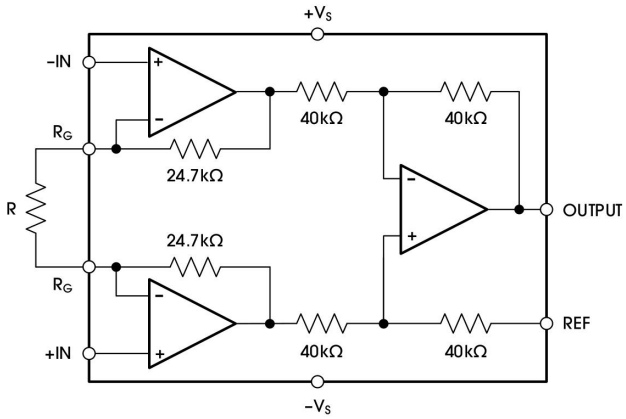


Figure 41. Functional Block Diagram

Characteristic description

Precision V-I converter

The INA129 together with another operational amplifier and two resistors form a precision current source (Figure 42). The operational amplifier buffered the reference terminals to maintain good CMR. The output voltage VX of the INA129 appears at both ends of R1, converting it into current. This current, minus only the input bias current of the op amp, then flows out to the load.

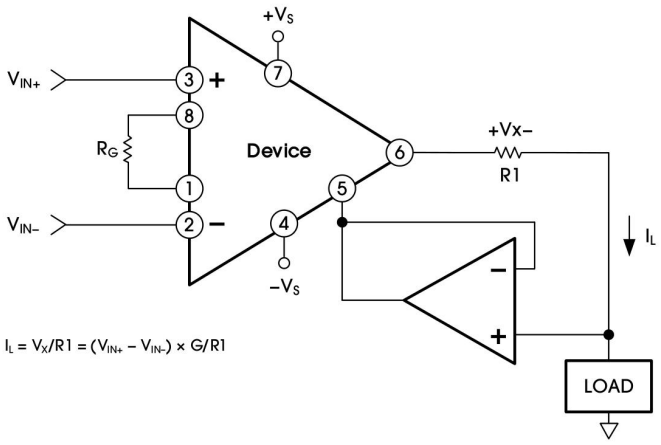


Figure 42. Precision Voltage-to-Current Converter

Design Requirements

The INA129 gain is programmed by the RG resistor, or more precisely, set by whatever impedance appears between pins 1 and 8. The INA129 is designed to provide precise gain using resistors ranging from 0.1% to 1%. Table 9 shows the required RG values for the various gains. Note that for G = 1, the RG pin is not connected (RG = ∞). For any gain, RG can be calculated using the following formula:

$$R_G = \frac{49.4k\Omega}{G - 1}$$

In order to minimize gain errors and avoid high parasitic resistance in series with RG; To minimize gain drift, RG should have a low TC - less than 10ppm/°C for best performance.

Table 9. Required Values of Gain Resistors

1% STD TABLE VALUE OF R_G (Ω)	CALCULATED GAIN	0.1% STD TABLE VALUE OF R_G (Ω)	CALCULATED GAIN
49.9k	1.990	49.3k	2.002
12.4k	4.984	12.4k	4.984
5.49k	9.998	5.49k	9.998
2.61k	19.93	2.61k	19.93
1.00k	50.40	1.01k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1,003.0

Input and output offset voltages

The low error of INA129 is attributed to two sources, input and output errors. When referring to input, the output error is divided by G. In practice, input errors dominate at high gain, while output errors dominate at low gain. The total VOS for a given gain is calculated as follows:

$$\text{Total Error RTI} = \text{Input Error} + (\text{Output Error} / G)$$
$$\text{Total Error RTO} = (\text{Input Error} \times G) + \text{Output Error}$$

Reference terminal

The reference terminal potential defines the zero output voltage and is especially useful when the load does not share precise ground with the rest of the system. It provides a direct way to inject precise offsets into the output. For optimal CMR, parasitic resistance should be kept to a minimum.

Input protection

For input voltages that exceed the supply, a protection resistor should be placed in series at each input to limit the current to 10mA. These can be the same resistors as those used in RFI filters. High resistance values affect the noise and AC CMRR performance of the system. A low leakage diode (e.g. BAV199) can be placed at the input to reduce the required protection resistance.

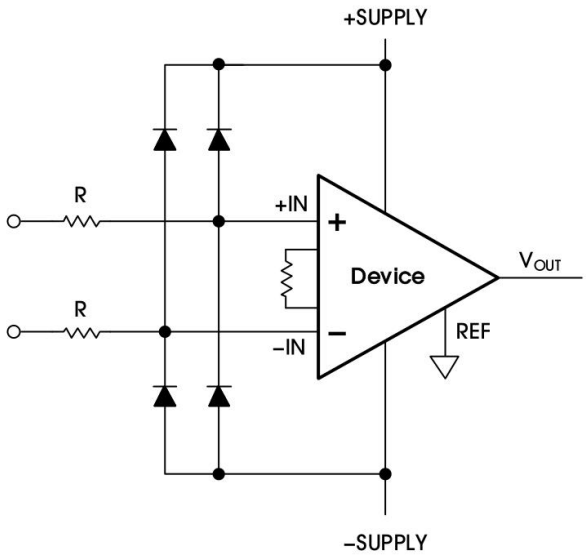


Figure 43. Diode Protection for Voltages Beyond Supply

Radio-frequency interference

All instrumentation amplifiers rectify small out-of-band signals. Interference may appear as a small DC voltage shift. High-frequency signals can be filtered using a low-pass R-C network placed at the input of the instrumentation amplifier. Figure 44 shows this configuration. The filter restricts the input signal according to the following relation:

$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_C}$$

Among them:

- $C_D \geq 10C_C$.

CD affects the difference signal. CC affects the common mode signal. Any mismatch in R × CC reduces the INA129 CMRR. To avoid unintentionally degrading CMRR bandwidth performance, make sure that CC is at least an order of magnitude smaller than CD. The impact of mismatched CC decreases as the CD-CC ratio increases.

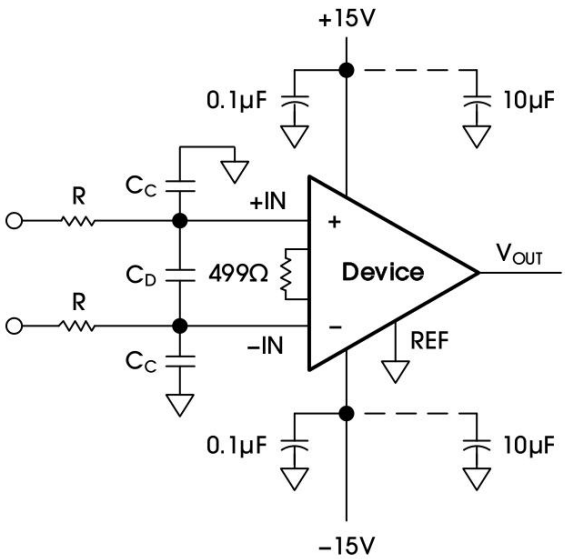


Figure 44. Circuit to Attenuate RF Interference

Common-mode rejection

The INA129 instrumentation amplifier provides high CMR, which is a measure of the change in output voltage when two inputs change by an equal amount. These specifications are usually given for the full range of input voltage variations and specified source imbalances.

For optimal CMR, the reference terminal should be connected to a low impedance point, and the capacitance and resistance differences between the two inputs should be kept to a minimum. In many applications, shielded cables are used to minimize noise; In order to obtain the best CMR in the frequency range, the shielding should be driven correctly. Figures 45 and 46 show active data protection, which is configured to improve AC common mode suppression by "boottripping" the capacitance of the input cable shield, thereby minimizing capacitance mismatch between inputs.

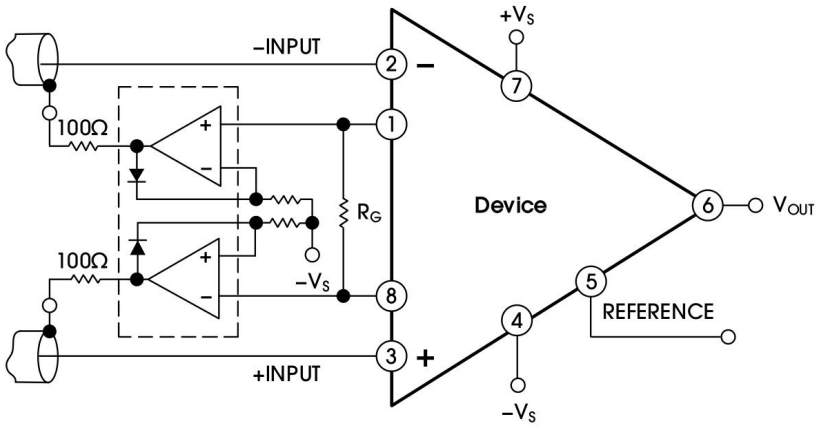


Figure 45. Differential Shield Driver

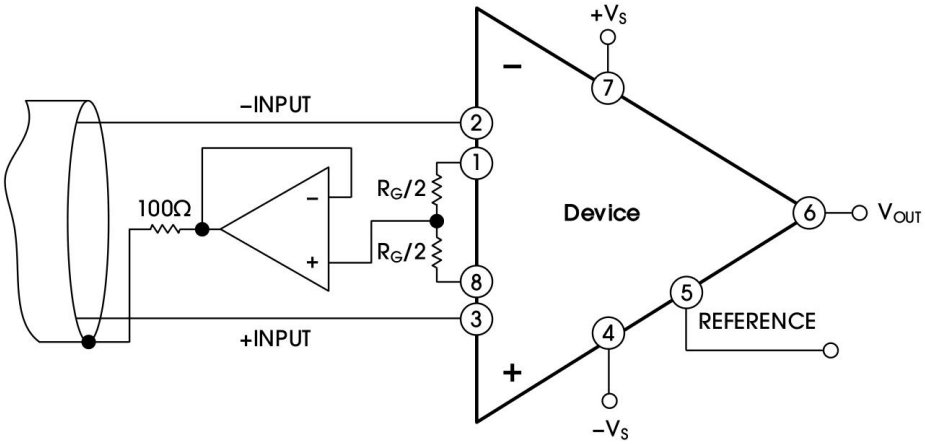


Figure 46. Common-Mode Shield Driver

Common mode input range

The linear input voltage range of the INA129 input circuit is approximately 2V lower than the positive charge and 0.1V higher than the negative supply. Differential input voltage increases output voltage; However, the linear input range is limited by the output voltage swing of the input stage of the amplifier. Therefore, the linear common-mode input range is related to the output voltage of the entire amplifier. This behavior also depends on the supply voltage. Input overload can produce a seemingly normal output voltage. For example, if the input overload condition drives two input amplifiers to their positive output swing limit, the differential voltage amplifier measured by the output is close to zero. The output stage outputs close to 0V, even if both inputs are overloaded. See Figure 32 through Figure 37.

Ground circuit for input bias current

The input bias current is the current necessary to bias the amplifier's input transistors. These currents must have a direct return path. Therefore, when amplifying "floating" input sources (such as transformers or AC coupled sources), there must be a DC path between each input and ground, as shown in Figure 47, Figure 48, and Figure 49.

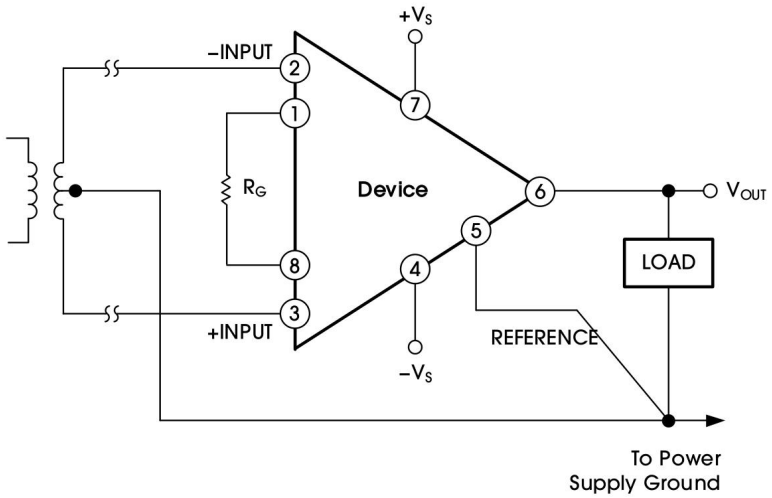


Figure 47. Ground Returns for Bias Currents with Transformer-Coupled Inputs

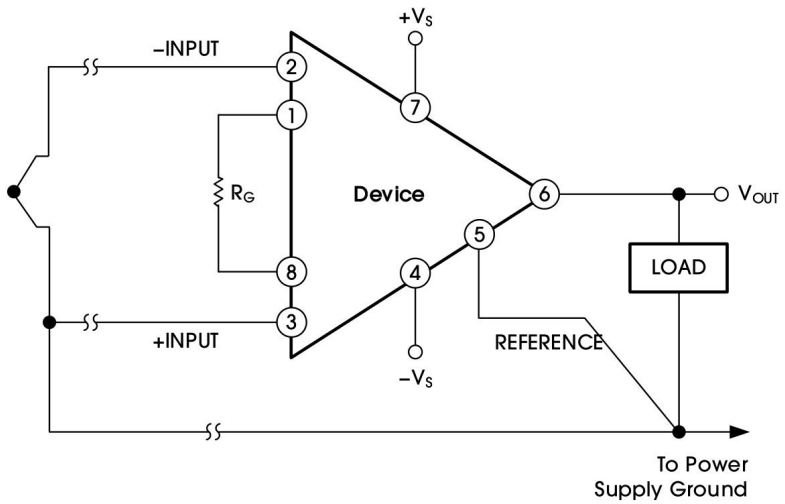


Figure 48. Ground Returns for Bias Currents with Thermocouple Inputs

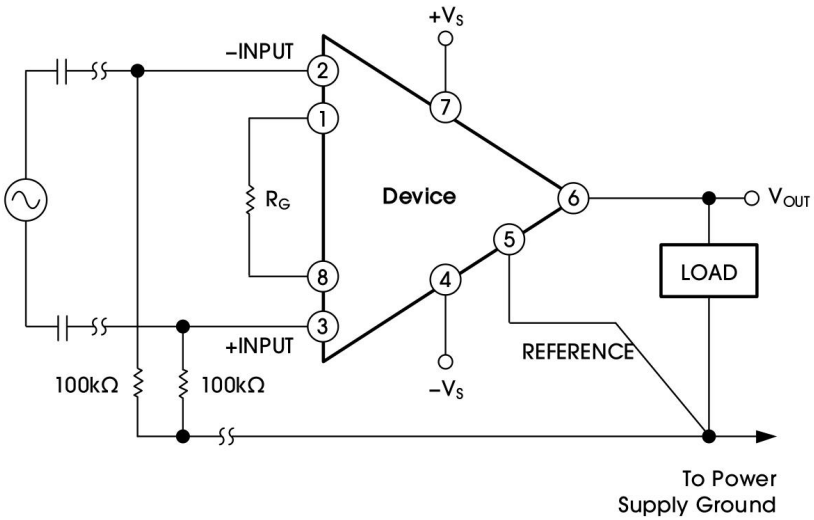


Figure 49. Ground Returns for Bias Currents with AC-Coupled Inputs

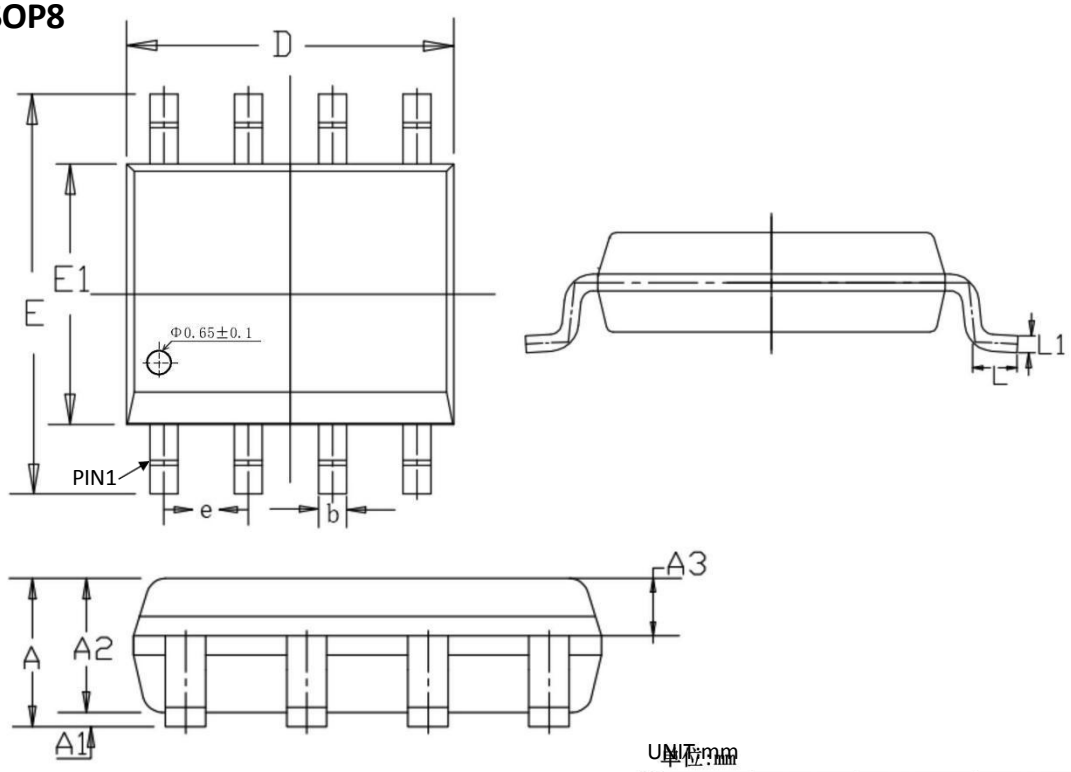
ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
INA129UA/2K5	INA129	SOP8	4.90 * 3.90	-40 to +85	MSL3	T&R	2500

9. DIMENSIONAL DRAWINGS

SOP8



UNIT:mm
单位:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1(站高)	0.100	0.150	0.200
A2(厚度)	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	-	0.510
e(脚间距)	1.240	1.270	1.300
D(长度)	4.800	4.900	5.000
E(跨度)	5.800	6.000	6.200
E1(宽度)	3.800	3.900	4.000
L(脚长)	0.450	0.600	0.750
L1	—	0.25BSC	—