Precision High Speed Fully Differential Amplifier

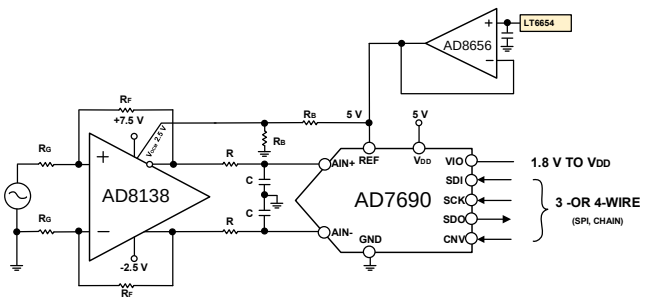
Features

- Broad Power Supply Range: 3 V to 15 V
- Low Power: 4.6 mA
- High Bandwidth: 145 MHz
- High Slew Rate: 447 V/µs
- Low Input Offset Voltage:
  50 µV max (B grade)
  110 µV max from -40 °C to +125 °C (B grade)
- Low Input Offset Current: max 70 nA
- Low Noise: 2.9 $nV/\sqrt{Hz}$, f = 100 kHz
- Wide Input Common-mode Range:
  $(-V_S)$ – 0.4 V to $(+V_S)$ – 1 V
- Wide Output Common Mode Control:
  $(-V_S)$ + 1 V to $(+V_S)$ – 1 V
- Rail-to-rail Output
- Low Harmonic Distortion:
  -133 dBc HD2 and -140 dBc HD3 at 1 kHz
- Fast Settling Time
  18-bit: 100 ns
  16-bit: 50 ns

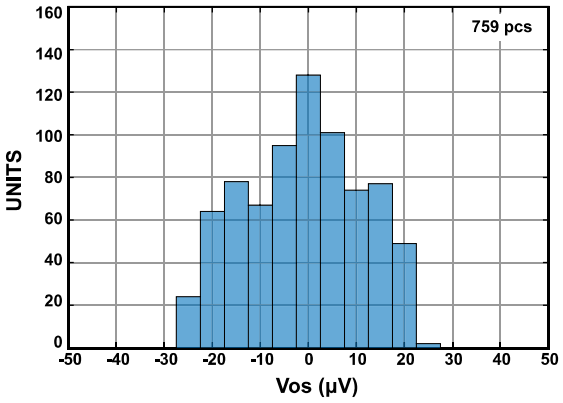
Applications

- Low Power Differential ADC Drivers
- Single-ended to Differential Converters
- Differential Buffers
- Medical Imaging
- Process Control
- Portable Electronics

Typical Application



Typical Characteristics



Pin Configurations and Function

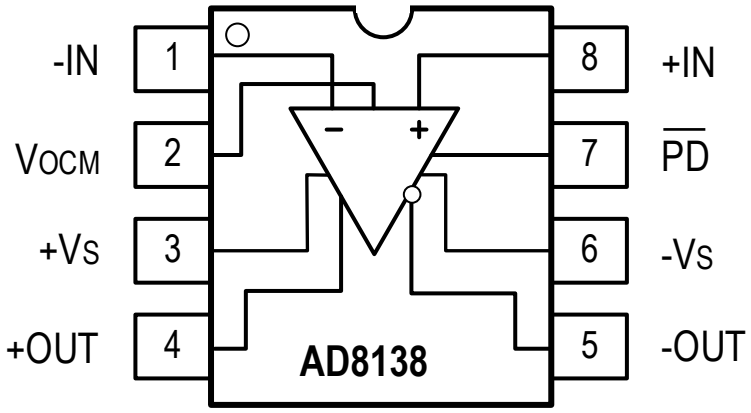


Figure 1. AD8138 Pin Configuration (8-lead SOIC and MSOP)

Mnemonic	Pin No.	I/O[1]	Description
-IN	1	AI	Negative Input Summing Node.
V_{OCM}	2	AI	Output Common-Mode Voltage.
$+V_S$	3	P	Positive Supply Voltage.
+OUT	4	AO	Positive Output for Load Connection.
-OUT	5	AO	Negative Output for Load Connection.
$-V_S$	6	P	Negative Supply Voltage.
$\overline{PD}$	7	AI	Power Down Control. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal Operation. Normal operation is the default.
+IN	8	AI	Positive Input Summing Node.

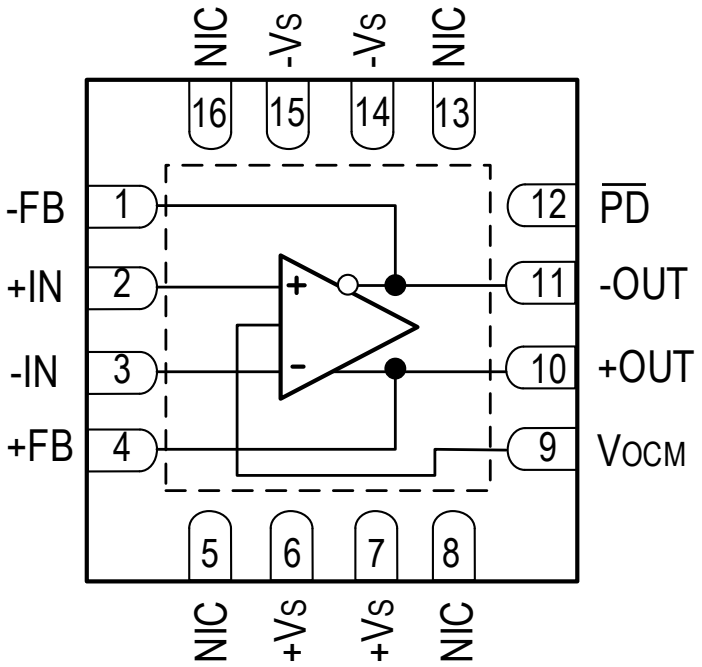


Figure 2. AD8138 Pin Configuration (16-lead QFN)

Mnemonic	Pin No.	I/O[1]	Description
-FB	1	AO	Negative Output for Feedback Component Connection.
+IN	2	AI	Positive Input Summing Node.
-IN	3	AI	Negative Input Summing Node.
+FB	4	AO	Positive Output for Feedback Component Connection.
NIC	5, 8, 13, 16	--	No Internal Connection.
+VS	6,7	P	Positive Supply Voltage.
V_{OCM}	9	AI	Output Common-Mode Voltage.
+OUT	10	AO	Positive Output for Load Connection.
-OUT	11	AO	Negative Output for Load Connection.
$\overline{PD}$	12	AI	Power Down Control. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal Operation. Normal operation is the default.
$-V_S$	14,15	P	Negative Supply Voltage.
Exposed pad (EPAD)			Exposed Pad. Solder it to a heat-spreading power or ground plane. This pad is electrically isolated from the die, but must be connected to a power or ground plane and not floated.

Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	15 V
Input Voltage	$\pm V_S$
Operating Temperature Range	-40 °C to 125 °C
Storage Temperature Range	-65 °C to 150 °C
Junction Temperature Range	-65 °C to 150 °C
Max Reflow Temperature	260 °C
Lead Temperature, Soldering (10 sec)	300 °C
ESD Rating (ESD)	
Human Body Model (HBM)	2 kV
Charge Device Model (CDM)	1.5 kV

Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-lead SOIC	158	43	°C/W
8-lead MSOP	190	44	°C/W
16-lead QFN	51	27	°C/W

Specifications

SUPPLY VOLTAGE (V_S = ±5 V)

The ● denotes the specification which apply over the full operating temperature range, otherwise specifications are at $+V_S$ = 5 V, $-V_S$ = -5 V, V_{OCM} = midsupply, G = 1, $R_F = R_G$ = 499 Ω, $R_{L, dm}$ =1 kΩ and T_A = 25 °C, unless otherwise noted.

Positive Input ($+D_{IN}$) or Negative Input ($-D_{IN}$) to Differential Output Voltage ($V_{OUT, dm}$) Performance.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
INPUT CHARACTERISTICS							
Input Offset Voltage	V_{OS}	B Grade			20	50	µV
			●			110	µV
		A Grade			50	100	µV
			●			500	µV
Input Offset Voltage Drift			●		0.5		µV/°C
Input Bias Current					2	5.5	µA
			●			25	µA
Input Offset Current					30	70	nA
			●			300	nA
Input Common-Mode Voltage (V_{CM}) Range				$(-V_S)$ - 0.4		$(+V_S)$ - 1	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±1 V	●	94			dB
Open-Loop Gain		Output Voltage (V_{OUT}) = ±4 V					dB
DYNAMIC PERFORMANCE							
-3 dB Small Signal Bandwidth		$V_{OUT, dm}$ = 20 mV_{P-P}, G = 1			145		MHz
Bandwidth for 0.1 dB Flatness		$V_{OUT, dm}$ = 20 mV_{P-P}, G = 1			19		MHz
Slew Rate		$V_{OUT, dm}$ = 8 V step			447		V/µs
Settling Time	t_S	16-bit			50		ns
		18-bit			100		ns
Output Overdrive Recovery		G = 2, $V_{OUT, dm}$ = 10 V_{P-P}, triangular waveform			30		ns
OUTPUT CHARACTERISTICS							
Output Voltage Swing [1]		Load resistance (R_L) = 100 Ω for each single-ended output		$(-V_S)$ + 0.9		$(+V_S)$ - 1	V
			●	$(-V_S)$ + 1.2		$(+V_S)$ - 1.4	V
		R_L = 1 kΩ		$(-V_S)$ + 0.2		$(+V_S)$ - 0.3	V
			●	$(-V_S)$ + 0.25		$(+V_S)$ - 0.4	V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Short-Circuit Current	I_{SC}	Sourcing			82		mA
			•		45		mA
		Sinking			89		mA
			•		55		mA
NOISE PERFORMANCE							
Input Voltage Noise Differential	e_n	f = 100 kHz			2.9		nV/√Hz
V_{OCM} PERFORMANCE							
Input Voltage Noise Gain		$\Delta V_{OUT, cm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V		0.99		1.01	V/V
V_{OCM} CHARACTERISTICS							
Input Common-Mode Voltage Range	IVR			$(-V_S) + 1$		$(+V_S) - 1$	V
Input Offset Voltage	V_{OSI}	$V_{OS, cm} = V_{OUT, cm} / 2$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 0 V	•		1	5	mV
Input Bias Current			•		0.1	5	µA
CMRR		$\Delta V_{OS, dm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V	•	86	96		dB

General Performance

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
$\overline{PD}$ Pin							
Input Voltage		Logic threshold	•	0.3	0.95	2	V
$\overline{PD}$ Pin Bias Current							
Enable		$\overline{PD}$ = 5 V			1.7	5	µA
Disable		$\overline{PD}$ = 0 V		-2	-0.7		µA
POWER SUPPLY							
Operating Range				3		15	V
Quiescent Current							
Enabled					4.6	4.9	mA
			•			7.3	mA
Disabled					45	60	µA
			•			80	µA
Positive Power Supply Rejection Ratio (PSRR)		$\Delta V_{OS, dm}/\Delta V_S$, ΔV_S = 1 V_{P-P}		86	103		dB
SPECIFIED TEMPERATURE RANGE							
				-40		125	°C

Typical Performance Characteristics

Unless otherwise stated, T_A = 25 °C, V_S = ±5 V, R_L = 2 kΩ.

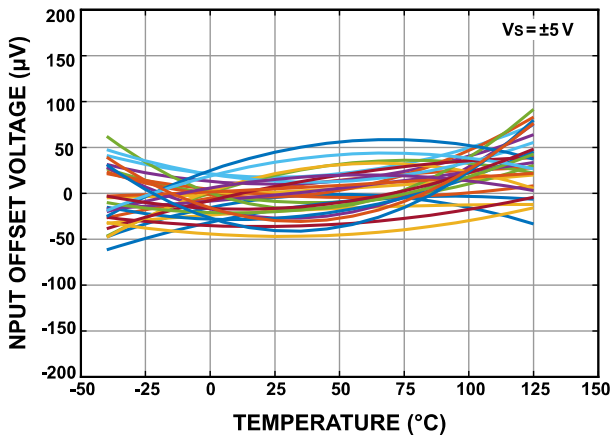


Figure 3. Input Offset Voltage vs. Temperature

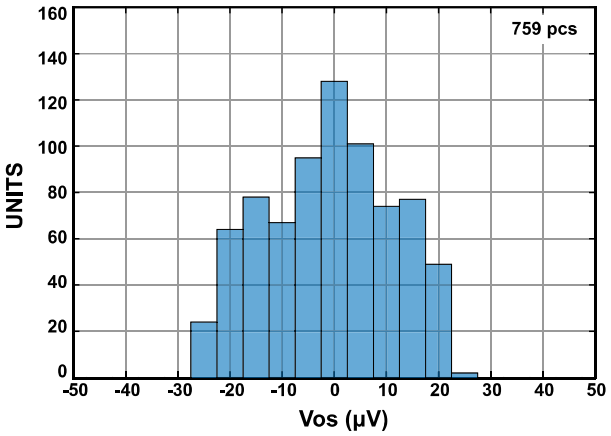


Figure 4. Input Offset Voltage Distribution

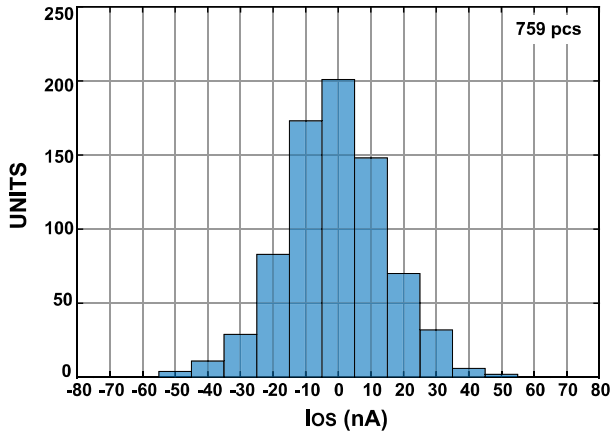


Figure 5. Input Offset Voltage Distribution

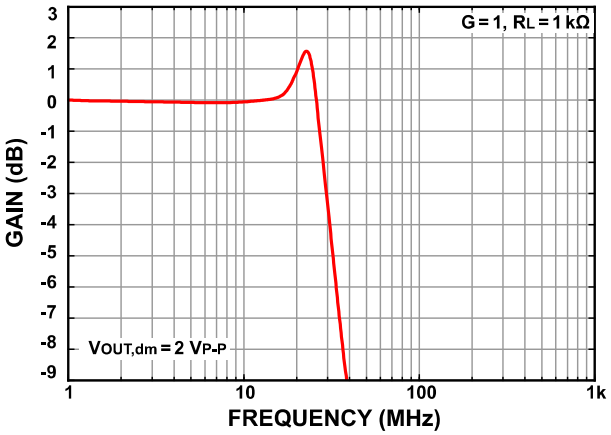


Figure 6. Large Signal Frequency Response

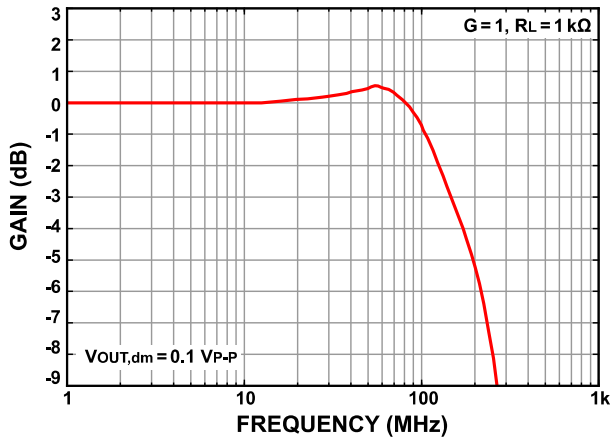


Figure 7. Small Signal Transient Response

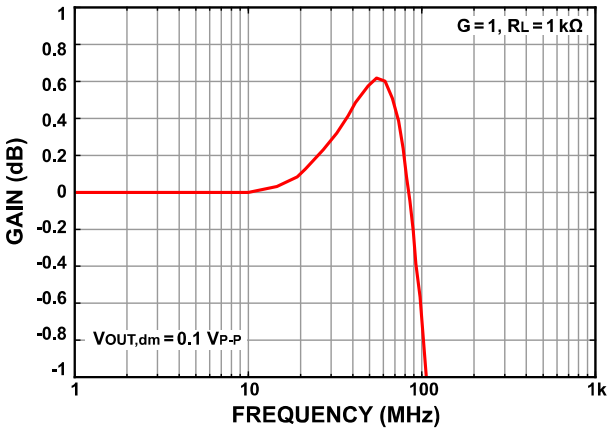


Figure 8. 0.1 dB Flatness Small Signal Frequency Response

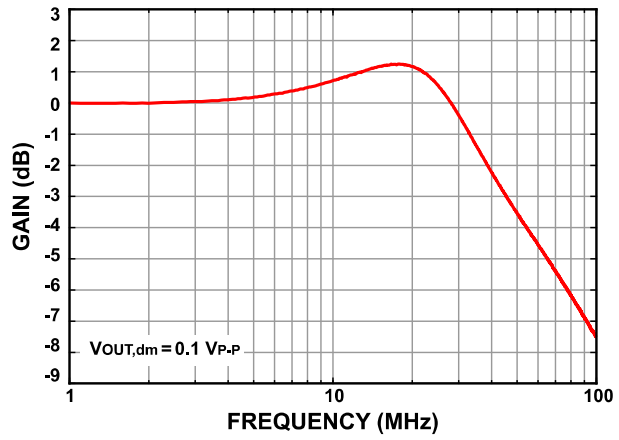


Figure 9. V_{OCM} Small Signal Frequency Response

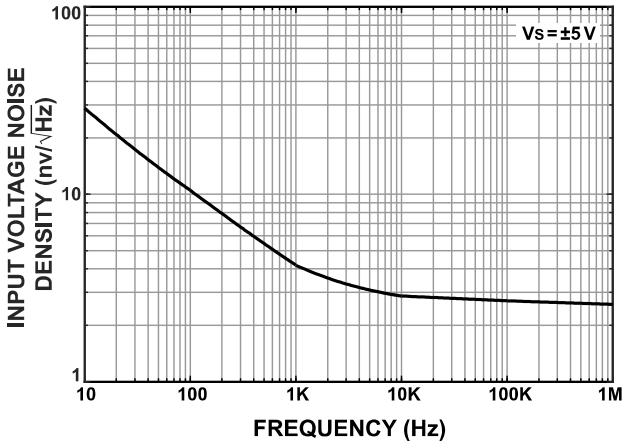


Figure 10. Voltage Noise Density

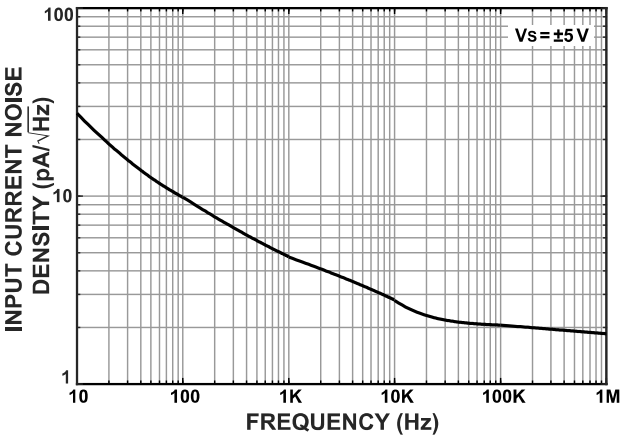


Figure 11. Current Noise Density

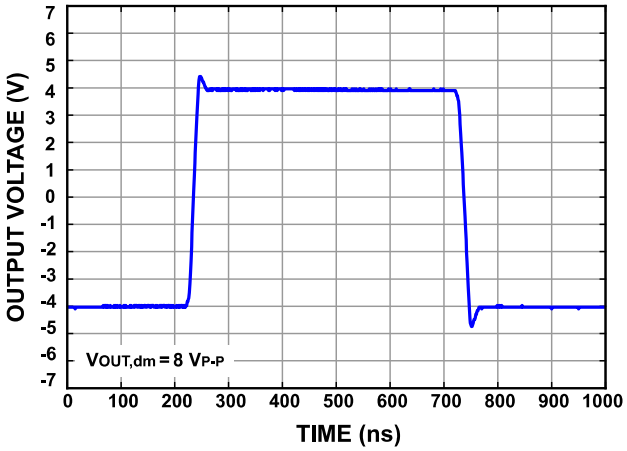


Figure 12. Large Signal Transient Response

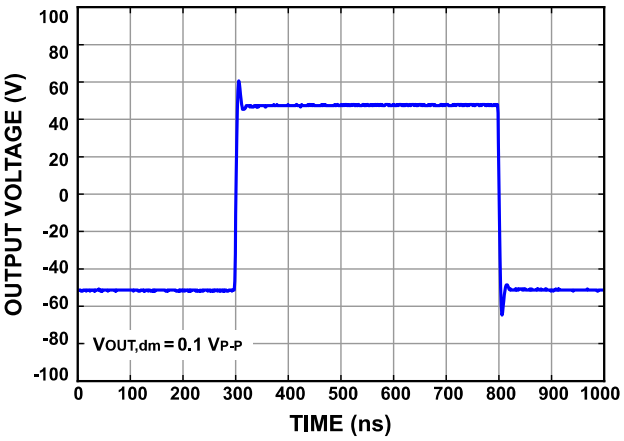


Figure 13. Small Signal Transient Response

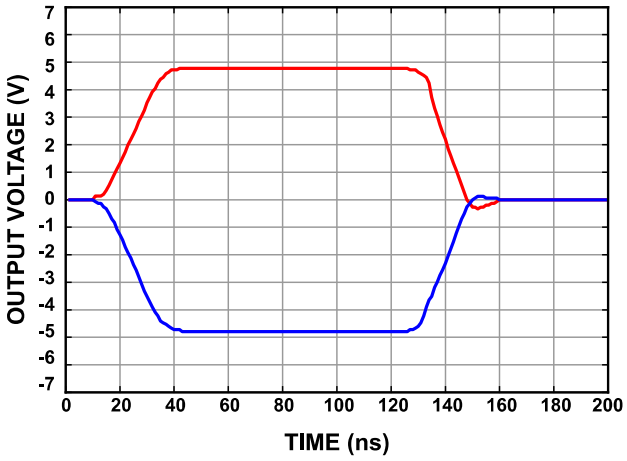


Figure 14. Overdrive Vs = 5 V Input = 5 V_{P-P} G = 2

Terminology and Application Assumptions

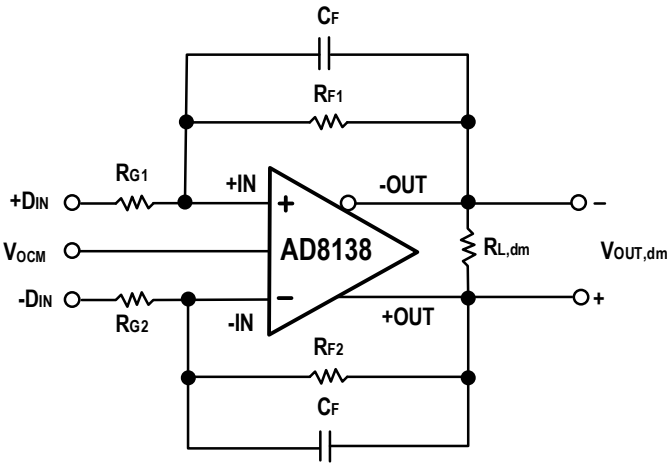


Figure 15. Circuit Definitions

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently output differential-mode voltage) is defined as

$$V_{OUT,dm} = (V_{+OUT} - V_{-OUT}) \qquad \text{(E1)}$$

where V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and -OUT terminals with respect to a common reference.

Common-mode voltage refers to the average of two node voltages. The output common-mode voltage is defined as

$$V_{OUT,cm} = \frac{(V_{+OUT} + V_{-OUT})}{2} = V_{OCM} \qquad \text{(E2)}$$

By setting

$$\beta_1 = \frac{R_{G1}}{R_{F1} + R_{G1}}$$

$$\beta_2 = \frac{R_{G2}}{R_{F2} + R_{G2}}$$

The voltages at outputs under ideal assumptions:

$$V_{+OUT} = \frac{(+D_{IN})(1-\beta_1) - (-D_{IN})(1-\beta_2) + 2V_{OCM}\beta_1}{\beta_1+\beta_2} \qquad \text{(E3)}$$

$$V_{-OUT} = \frac{-[(+D_{IN})(1-\beta_1) - (-D_{IN})(1-\beta_2)] + 2V_{OCM}\beta_2}{\beta_1+\beta_2} \qquad \text{(E4)}$$

$$V_{OUT,dm} = \frac{2[(+D_{IN})(1-\beta_1) - (-D_{IN})(1-\beta_2)] + 2V_{OCM}(\beta_1-\beta_2)}{\beta_1+\beta_2} \qquad \text{(E5)}$$

For a balanced system where $R_{G1} = R_{G2} = R_G$ and $R_{F1} = R_{F2} = R_F$, the equations simplify to

$$\beta_1 = \beta_2 = \frac{R_G}{R_F + R_G}$$

Balance is a measure of how well differential signals are matched in amplitude and exactly 180° apart in phase. Balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the midpoint of the divider with the magnitude of the differential signal (see Figure 16). By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage:

$$Output\ Balance\ Error = \left|\frac{V_{OUT,cm}}{V_{OUT,dm}}\right|$$

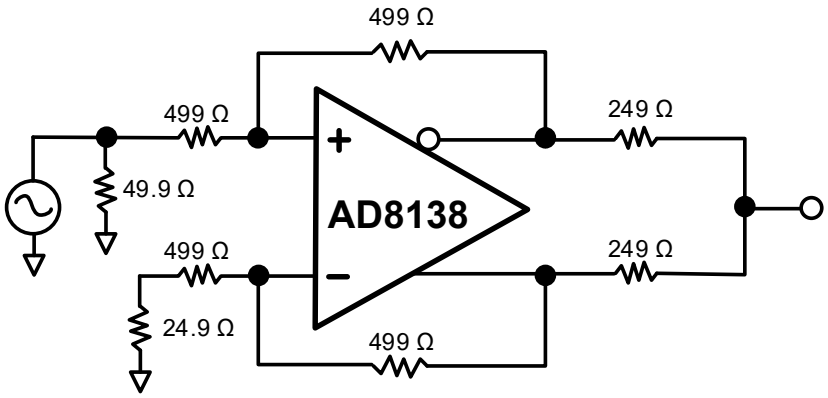


Figure 16. Test Circuit for Output Balance

Numerous common terms that are unique to this type of device exist.

- Fully differential amplifier (FDA). This term is restricted to devices offering what appears similar to a differential inverting op amp design element that requires an input resistor (not a high-impedance input) and includes a second internal control loop that sets the output average voltage ($V_{OUT,CM}$) to a set point.
- This second common-mode control loop interacts with the differential loop in certain configurations.
- The desired output signal at the two output pins is a differential signal that swings symmetrically around a common-mode voltage, which is the average voltage for the two outputs as defined above as $V_{OUT,CM}$.
- Single-ended to differential. The output must always be used differentially in an FDA; however, the source signal can be either a single-ended or a differential source with a variety of implementation details for either source. For an FDA operating in single-ended to differential, only one of the two input signals is applied to one of the input resistors.
- The common-mode control has limited bandwidth from the input V_{OCM} pin to the common-mode output voltage. The internal loop bandwidth beyond the input V_{OCM} buffer is a much wider bandwidth than the reported V_{OCM} bandwidth but is not directly discernable. A very wide bandwidth in the internal V_{OCM} loop is required to perform an effective and low-distortion single-ended to differential conversion.

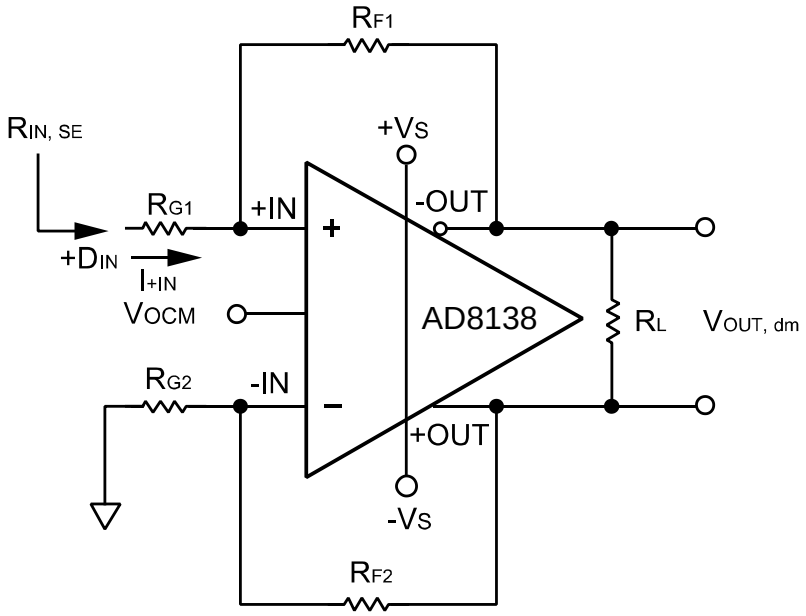


Figure 17. AD8138 with Unbalanced (Single -Ended) Input

The input impedance becomes

$$R_{IN,SE} = \frac{+D_{IN}}{I_{+IN}} = \frac{+D_{IN}}{(+D_{IN} - V_{-OUT})/(R_{G1} + R_{F1})} = R_{G1}\frac{\beta_1 + \beta_2}{\beta_1(1 + \beta_2)}$$

For a balanced system where $R_{G1} = R_{G2} = R_G$ and $R_{F1} = R_{F2} = R_F$, the equations simplify to

$$R_{IN,SE} = \frac{R_G}{1 - \frac{R_F}{2(R_G + R_F)}} \qquad \text{(E6)}$$

The input impedance of the circuit is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistors R_{G1} and R_{G2}.

Input Common-mode Voltage Range

The input common-mode range at the summing nodes of the AD8138 is specified as ($-V_S$) – 0.4 V to ($+V_S$) – 1 V. By extending the input common-mode range down to ($-V_S$) – 0.4 V, the AD8138 is especially well suited to dc-coupled, single-ended-to-differential, and single-supply applications, such as ADC driving.

The AD8138 is optimized for level-shifting, ground-referenced input signals. For a single-ended input, this would imply, for example, that the voltage at $-D_{IN}$ in Figure 15 would be 0 V when the negative power supply voltage of the amplifier (at pin $-V_S$) is also set to 0 V.

Setting the Output Common-mode Voltage

To ensure accurate control of the output common-mode level, the V_{OCM} pin of the AD8138 should not be left open. An external low impedance voltage source, or resistor divider (made up of 10 kΩ resistors as shown in Figure 19), should be used. The output common-mode offset listed in the Specifications section assumes the V_{OCM} input is driven by a low impedance voltage source.

Driving a Capacitive Load

The capacitive load of an ADC or some other next-stage device is commonly required to be driven. However, a purely capacitive load can react with the pin and bond wire inductance of the AD8138 , resulting in high frequency ringing in the pulse response. One way to minimize this effect is to place a small capacitor across each of the feedback resistors. The added capacitance should be small to avoid destabilizing the amplifier. An alternative technique is to place a small resistor in series with the outputs of the amplifier, as shown in Figure 18. Even when the small resistor is not required, good practice is to leave a place for them in a board layout (a 0 Ω value initially) for later adjustment in case the response appears unacceptable.

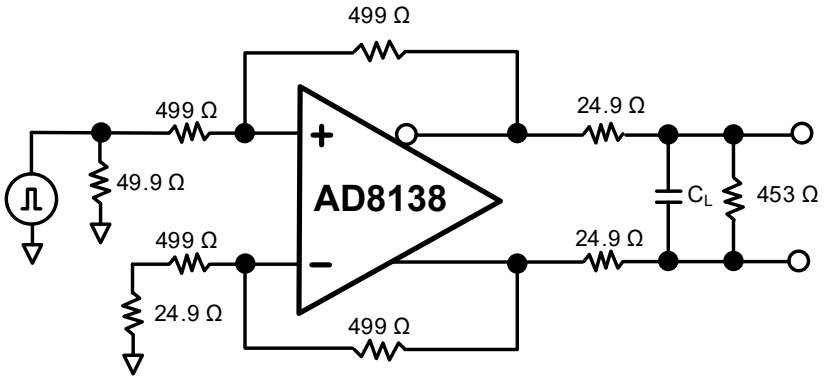


Figure 18. Test Circuit for Cap Load Drive

Operating the Power Shutdown Feature

The wideband FDA requires external resistors for correct signal-path operation. When configured for the desired input impedance and gain setting with these external resistors, the amplifier can be controlled via the $\overline{PD}$ pin with a voltage threshold of

$$\frac{[(+V_S) + (-V_S)]}{2} + 0.7\ V$$

It can be turned off by asserting $\overline{PD}$ lower than the threshold. Disabling the amplifier shuts off the quiescent current and stops correct amplifier operation. The signal path is still present for the source signal through the external resistors, which provides poor signal isolation from the input to output in power-down mode.

An internal pullup resistor is provided on the $\overline{PD}$ pin so that AD8138 's default state is power on. For applications simply requiring the device to be powered on when the supplies are present, tie the $\overline{PD}$ pin to the positive supply voltage.

Interfacing to High-Performance Precision ADCs

The AD8138 provides a simple interface to a wide variety of precision SAR and sigma-delta (Σ-Δ) ADCs. To deliver the exceptional distortion at the output pins, considerably wider bandwidth than what is typically required in the signal path to the ADC inputs is provided by the AD8138 . This wide amplifier bandwidth provides the low broadband, closed-loop output impedance to supply the sampling glitches and to recover quickly for the best SFDR.

A particularly challenging task is to drive the high-frequency modulator sample rates for a precision Σ-Δ converter where the modulator frequency can be far higher than the final output data rate.

For SAR ADC drivers, noise, distortion, bandwidth, slew rate, and output drive capability are critical specifications. Since SAR ADCs are typically used in precision applications, the AD8138's precision performance, including offset voltage and its drift, is crucial for system performance. As demonstrated in Figure 22, the AD7690 (an 18 -bit, 400 kSPS SAR ADC) combined with the AD8138 fully differential amplifier and the LT5400 -4 delivers exceptional DC and AC performance across a wide temperature range of -40 °C to 125 °C.

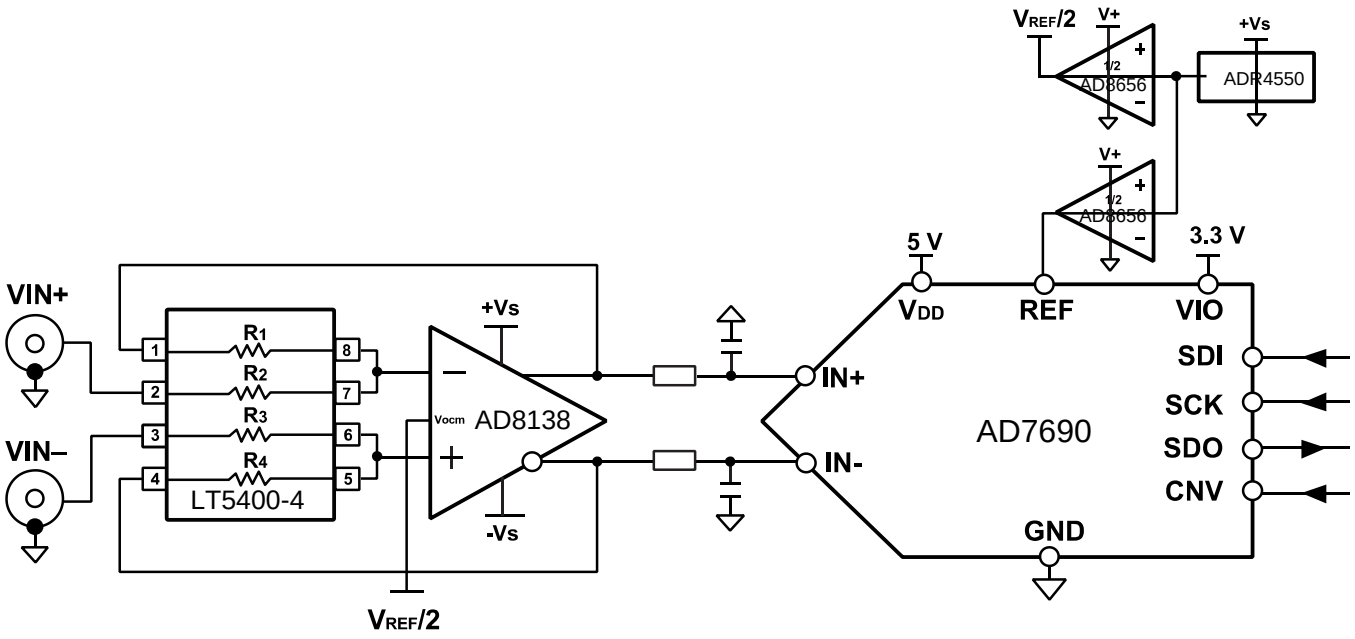


Figure 22. Using AD8138 with 18-bit SAR ADC AD7690

The AD8138 has also been verified to drive the AC4022, a 20 -bit, 350 kSPS SAR ADC.

Layout Guidelines

Similar to all high-speed devices, best system performance is achieved with close attention to board layout. General high-speed signal path layout suggestions include:

- Continuous ground planes are preferred for signal routing with matched impedance traces for longer runs; however, both ground and power planes must be opened up around the capacitive sensitive input and output device pins. When the signal goes to a resistor, parasitic capacitance becomes more of a band-limiting issue and less of a stability issue.
- Good high-frequency decoupling capacitors (0.1 µF) are required to a ground plane at the device power pins. Additional higher-value capacitors (2.2 µF) are also required but can be placed further from the device power pins and shared among devices. For best high-frequency decoupling, consider X2Y supply decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- Differential signal routing over any appreciable distance must use microstrip layout techniques with matched impedance traces.
- The input summing junctions are very sensitive to parasitic capacitance. Any R_G elements must connect into the summing junction with minimal trace length to the device pin side of the resistor. The other side of the R_G elements can have more trace length if needed to the source or to GND.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85 °C for 30 minutes is sufficient for most circumstances.

Layout Example

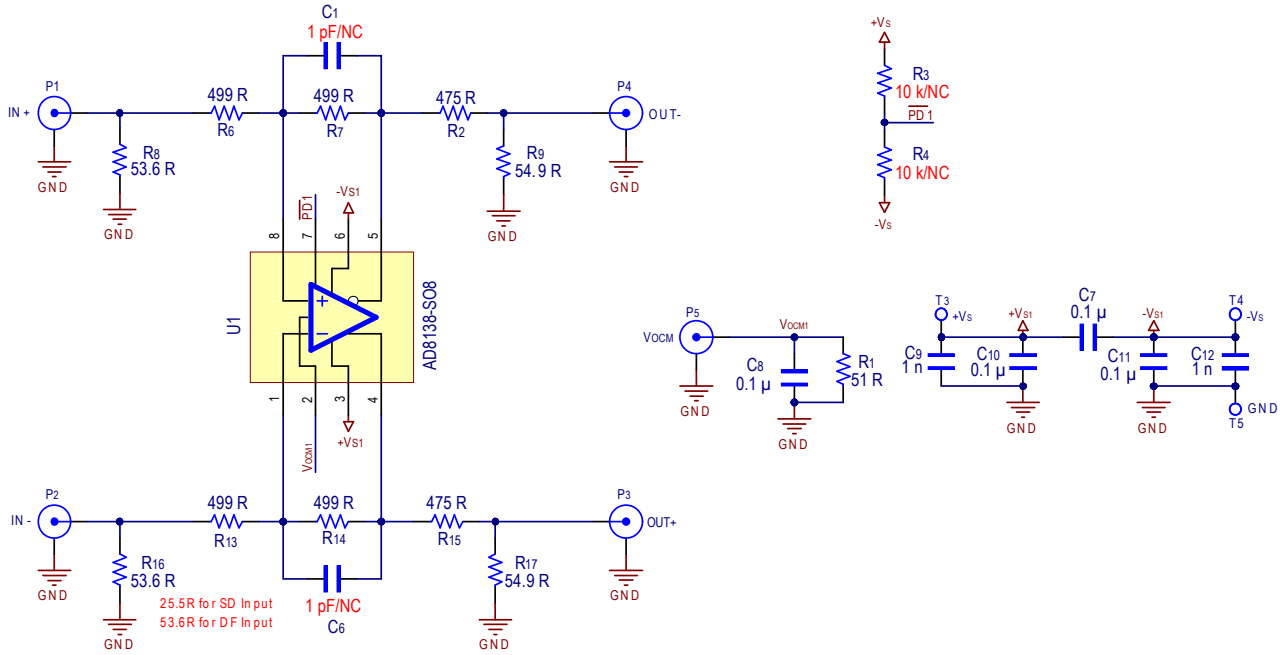


Figure 23. AD8138 Evaluation Board Schematic

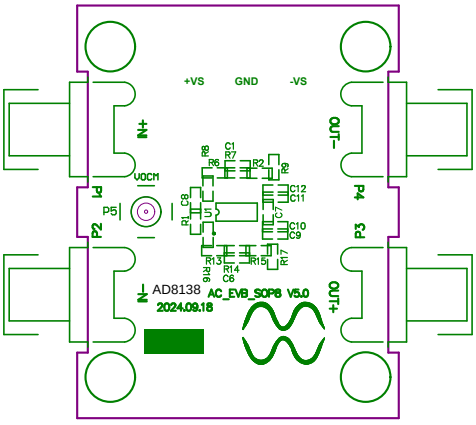


Figure 24. AD8138 Evaluation Board Top Silkscreen

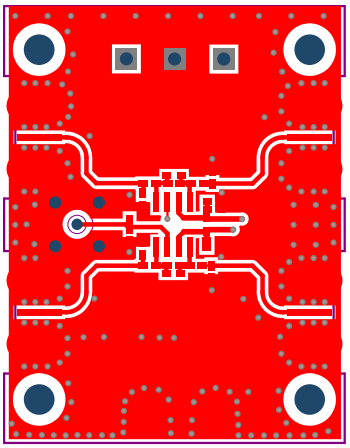


Figure 25. AD8138 Evaluation Board Layout (Top Layer)

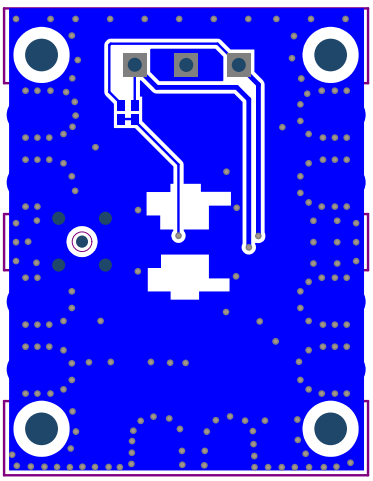


Figure 26. AD8138 Evaluation Board Layout (Bottom Layer)

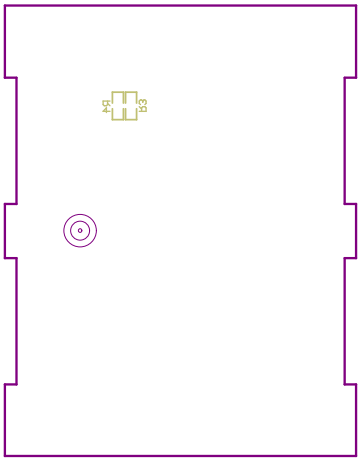


Figure 27. AD8138 Evaluation Board Bottom Silkscreen

Outline Information

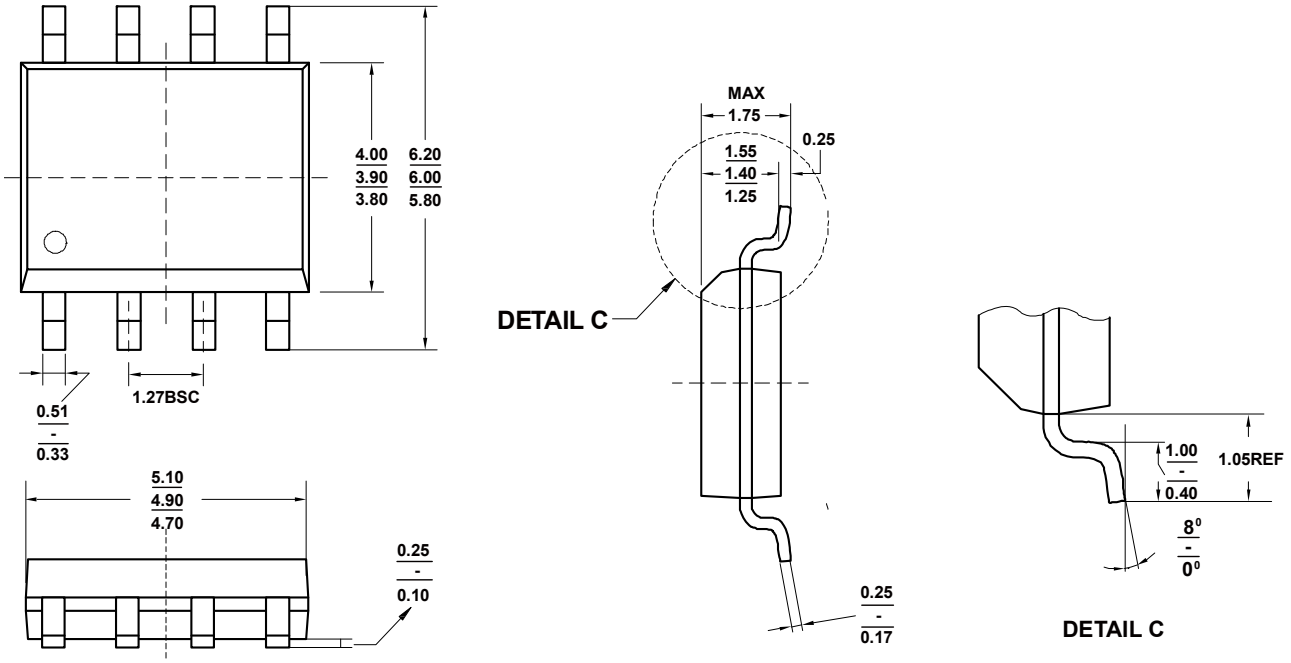


Figure 28. 8-Lead SOIC Package Dimensions shown in millimeters

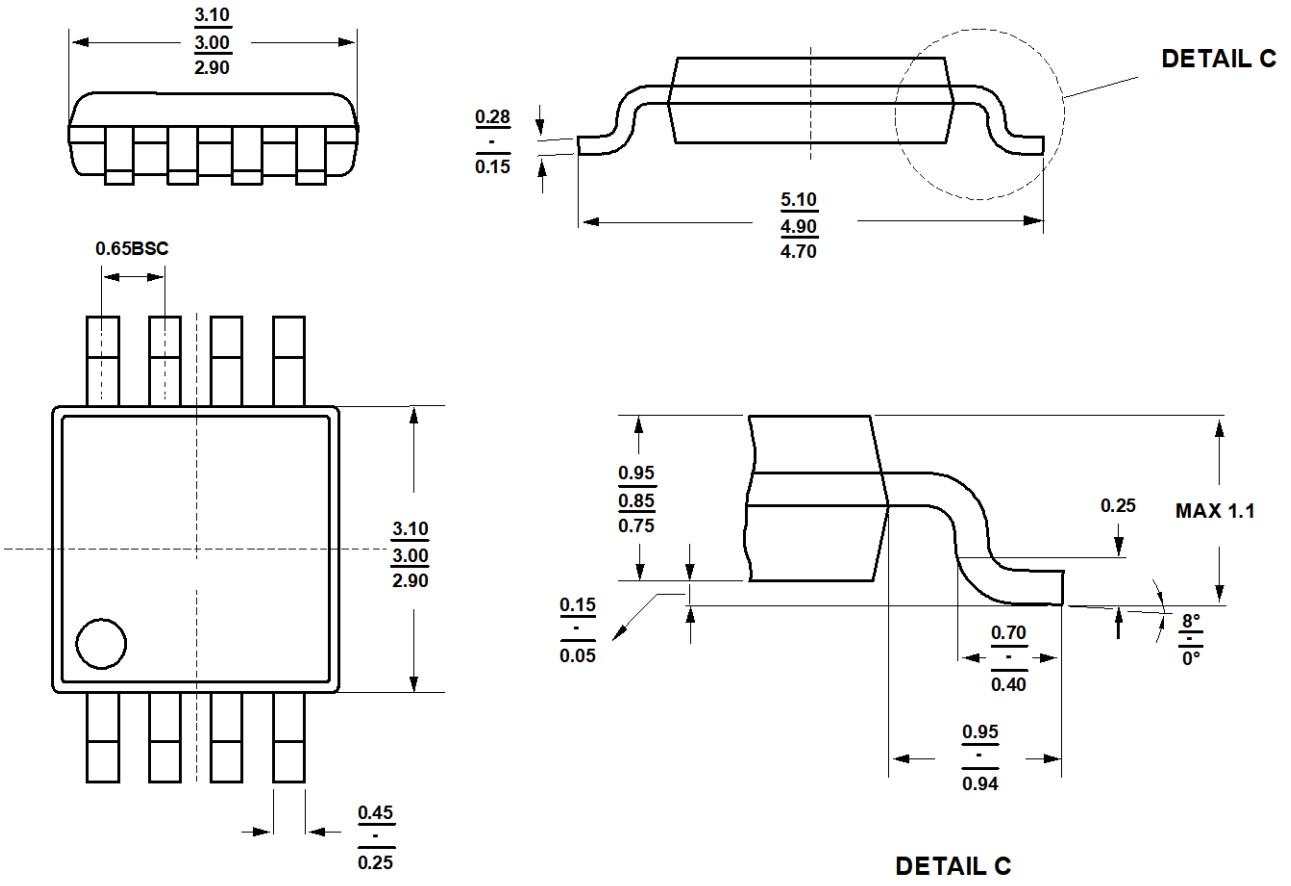


Figure 29. 8-Lead MSOP Package Dimensions shown in millimeters

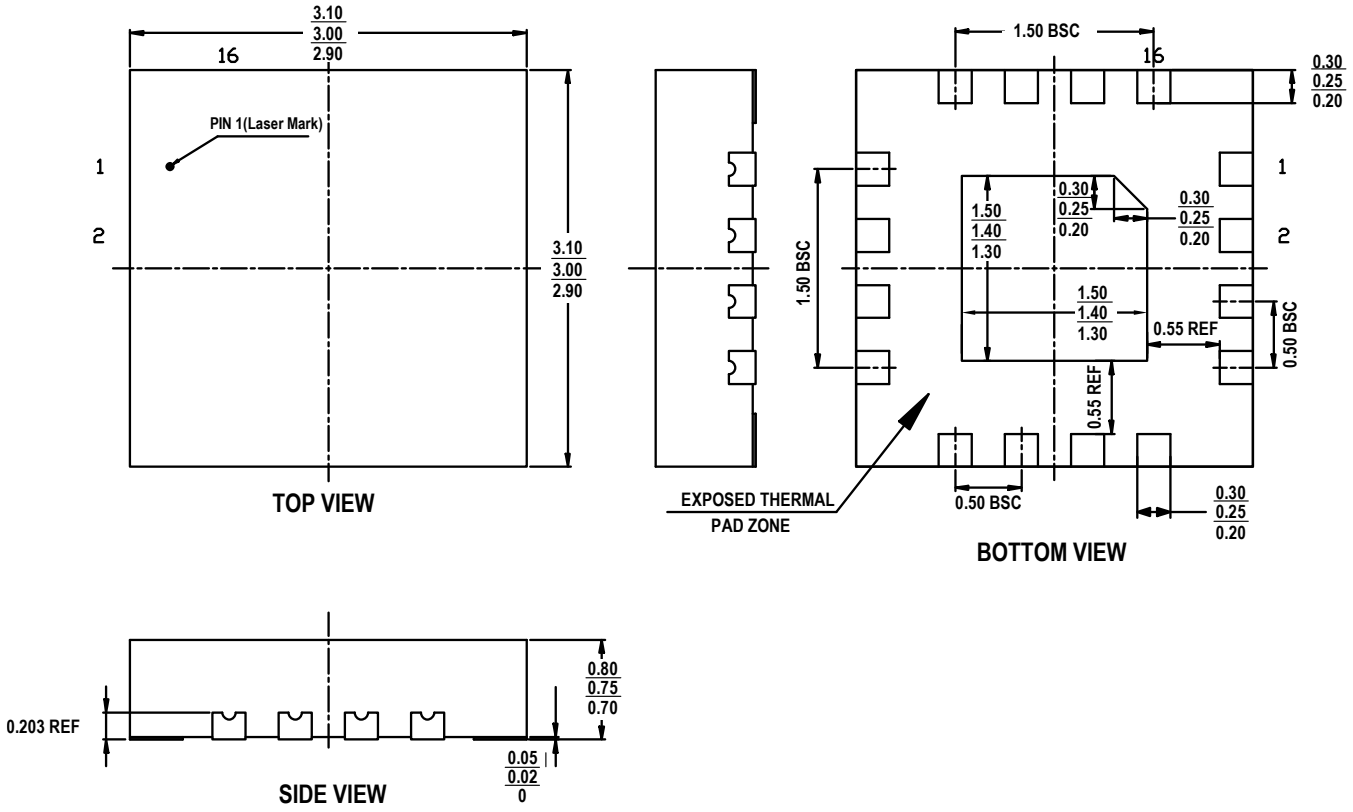


Figure 30. 16-Lead QFN Package Dimensions shown in millimeters

Ordering Guide

Model	Orderable Device	Status[1]	Package	Vos (max) (μV)	Temperature Range (°C)	External Package
AD8138	AD8138ARZ	ACTIVE	SOIC-8	50	-40 to +125	Tube
	AD8138ARZ-R7	ACTIVE				13” Reel
	AD8138AR	ACTIVE		100		Tube
	AD8138AS	ACTIVE				13” Reel
	AD8138BRZ	ACTIVE	MSOP-8	50		Tube
	AD8138BRZ-R7	ACTIVE				13” Reel
	AD8138BR	ACTIVE		100		Tube
	AD8138BS	ACTIVE				13” Reel
	AD8138CR	ACTIVE	QFN-16	50		13” Reel
	AD8138CS	ACTIVE		100		