12V, 100mA, Ultralow Noise, Ultrahigh PSRR LDO

DESCRIPTION

The 1033 is an ultralow noise and ultrahigh PSRR LDO. Using an advanced structure, it achieves excellent line and load transient response with only a 4.7μF ceramic output capacitor.

The 1033 is capable of sourcing 100mA at a typical 250mV dropout voltage. And it can be easily paralleled to further increase output current and reduce noise.

The device is suitable for powering noise sensitive applications, such as RF circuit, high precision ADC/DAC and high precision sensor.

DEVICE INFORMATION

Part No.	Package	Packing
1033TR	DFN-10-3×3×0.75-0.5	Tape & Reel

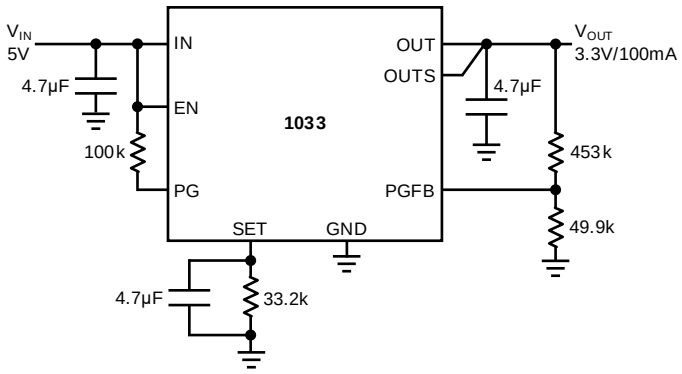
FEATURES

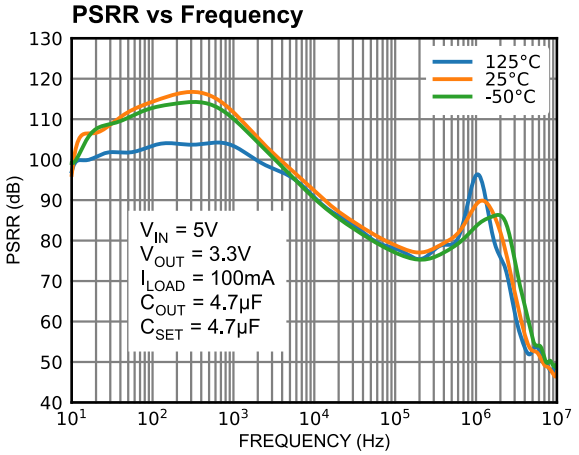
- Ultralow RMS Noise: 0.9μV_{RMS} (10Hz to 100kHz)
- Ultrahigh PSRR: 78dB@100kHz, 88dB@1MHz
- Wide Input Voltage Range: 2V to 12V
- Wide Output Voltage Range: 0V to 9V
- Output Current: 100mA
- Low Dropout Voltage: 250mV
- Programmable PG Threshold

APPLICATIONS

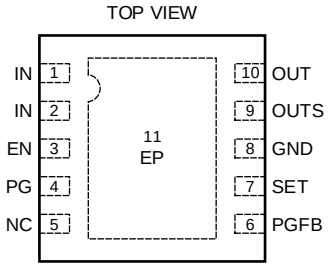
- RF Circuit: LNA, PLL, Mixer
- High Precision ADC/DAC
- High Precision Sensor
- High Precision Signal Process Circuit
- Medical Instrument
- Post-Regulator for SMPS

TYPICAL APPLICATION





PIN CONFIGURATION



PIN FUNCTIONS

Pin No.	Pin Name	I/O	Function Description
1, 2	IN	I	Power Supply. Supply voltage ranges from 2V to 12V. A bypass capacitor at the IN pin is required.
3	EN	I	Enable. Regulator enable control or undervoltage lockout threshold input. The typical threshold voltage is 1.27V.
4	PG	O	Power Good Indication. This is an open-collector pin. Float the PG pin if not used.
5	NC	-	No Connection.
6	PGFB	I	Power Good Feedback. Connect PGFB to the center point of the external resistor divider. The typical PGFB threshold voltage is 300mV.
7	SET	I	Output Voltage Set Pin.
8	GND	G	GND.
9	OUTS	I	Output Voltage Sensing Feedback. Connect OUTS to output side of the output capacitor.
10	OUT	O	Regulator Output. Bypass with a minimum 4.7μF ceramic capacitor to GND.
11	EP	-	Exposed Pad. No internal electrical connection. Solder the EP to GND pin and connect to a large copper plane to reduce thermal resistance.
I = Input, O = Output, G = Ground			

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
IN Voltage	V_{IN}	-0.3 ~ 13.2	V
EN Voltage	V_{EN}	-0.3 ~ 13.2	V
PG Voltage	V_{PG}	-0.3 ~ 13.2	V
PGFB Voltage	V_{PGFB}	-0.3 ~ 13.2	V
SET Voltage	V_{SET}	-0.3 ~ 10	V
OUT Voltage	V_{OUT}	-0.3 ~ 10	V
OUTS Voltage	V_{OUTS}	-0.3 ~ 10	V
Lead Temperature (Soldering 5 Sec)	T_{LEAD}	260	ºC
Operating Junction Temperature Range	T_J	-40 ~ 125	ºC
Storage Temperature Range	T_{STG}	-65 ~ 150	ºC
Junction-to-Ambient Thermal Resistance	θ_{JA}	34	ºC/W
ESD Protection (HBM)	V_{ESD_HBM}	±2000	V
ESD Protection (CDM)	V_{ESD_CDM}	±1000	V

ELECTRICAL CHARACTERISTICS

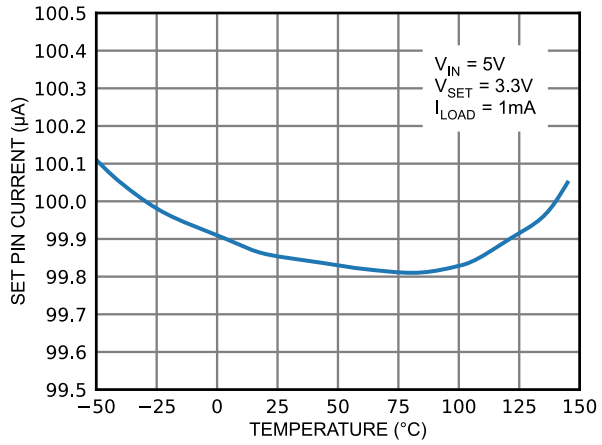
The • denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. C_{SET} = 4.7µF, C_{OUT} = 4.7µF, unless otherwise noted.

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Minimum IN Pin Voltage	V_{IN_MIN}	I_{LOAD} = 10mA, V_{IN} UVLO Rising	•		1.75	2	V
SET Pin Current	I_{SET}	V_{IN} = 2V, V_{OUT} = 1.4V, I_{LOAD} = 1mA		99	100	101	µA
		2V ≤ V_{IN} ≤ 12V, 0V ≤ V_{OUT} ≤ 9V, 1mA ≤ I_{LOAD} ≤ 100mA	•	98	100	102	µA
SET Pin Current During Fast Start-Up	I_{SET_FS}	V_{PGFB} = 289mV, V_{IN} = 2.8V, V_{SET} = 1.4V			2.1		mA
Output Offset Voltage (V_{OUT} - V_{SET})	V_{OS}	V_{IN} = 2V, V_{OUT} = 1.4V, I_{LOAD} = 1mA		-0.4		0.4	mV
		2V ≤ V_{IN} ≤ 12V, 0V ≤ V_{OUT} ≤ 9V, 1mA ≤ I_{LOAD} ≤ 100mA	•	-1		1	mV
Line Regulation	ΔI_{SET}	V_{IN} = 2V to 12V, V_{OUT} = 1.4V, I_{LOAD} = 1mA			0.5		nA/V
	ΔV_{OS}	V_{IN} = 2V to 12V, V_{OUT} = 1.4V, I_{LOAD} = 1mA	•		1	±3	µV/V
Load Regulation	ΔI_{SET}	I_{LOAD} = 1mA to 100mA, V_{IN} = 2V, V_{OUT} = 1.4V			9		nA
	ΔV_{OS}	I_{LOAD} = 1mA to 100mA, V_{IN} = 2V, V_{OUT} = 1.4V	•		0.06	0.3	mV
Dropout Voltage	V_{DROP}	V_{IN} = 3.3V, V_{SET} = 3.3V, I_{LOAD} = 100mA	•		250	320	mV
Quiescent Current in Shutdown	I_{Q_SD}	V_{IN} = 6V, V_{EN} = 0V			0.5	1	µA
			•			5	µA
Ripple Rejection	PSRR	f_{RIPPLE} = 1kHz, V_{RIPPLE} = 100mV_{PP}, I_{LOAD} = 100mA			112		dB
		f_{RIPPLE} = 100kHz, V_{RIPPLE} = 100mV_{PP}, I_{LOAD} = 100mA			78		dB
		f_{RIPPLE} = 1MHz, V_{RIPPLE} = 100mV_{PP}, I_{LOAD} = 100mA			88		dB
Output RMS Noise	V_{NOISE}	BW = 10Hz to 100kHz, V_{OUT} = 3.3V, I_{LOAD} = 100mA			0.9		μV_{RMS}
EN Threshold	V_{EN_TH}	V_{IN} = 10V	•	1.18	1.25	1.32	V
EN Threshold Hysteresis	V_{EN_HYS}	V_{IN} = 10V			200		mV
EN Pin Current	I_{EN}	V_{IN} = 10V, V_{EN} = 1.4V	•		0.04	1	µA
Current Limit	I_{LIMIT}	V_{IN} = 9V, V_{OUT} = 0V	•	120	150	180	mA
PGFB Threshold	V_{PGFB_TH}	PGFB Rising	•	292	301	310	mV
PGFB Threshold Hysteresis	V_{PGFB_HYS}				7		mV
PGFB Pin Current	I_{PGFB}	V_{IN} = 2V, V_{PGFB} = 300mV	•	-100	-34	100	nA
PG Output Low Voltage	V_{PG_LOW}	I_{PG} = 100µA	•		50	100	mV
Thermal Shutdown	T_{SD}	T_J Rising			164		°C
Thermal Shutdown Hysteresis	T_{SD_HYS}				7		°C

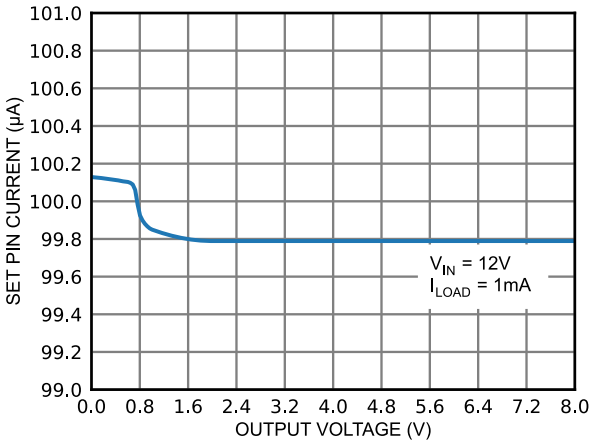
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

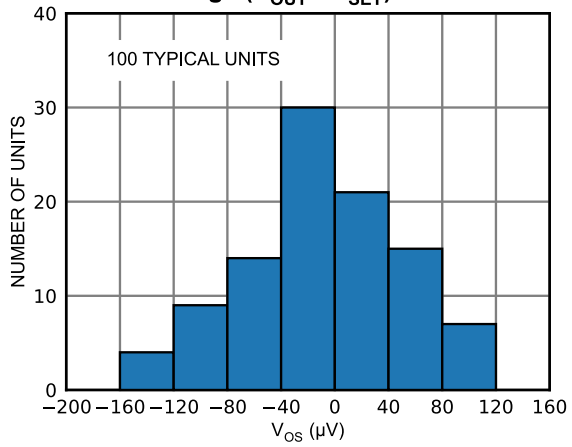
SET Pin Current



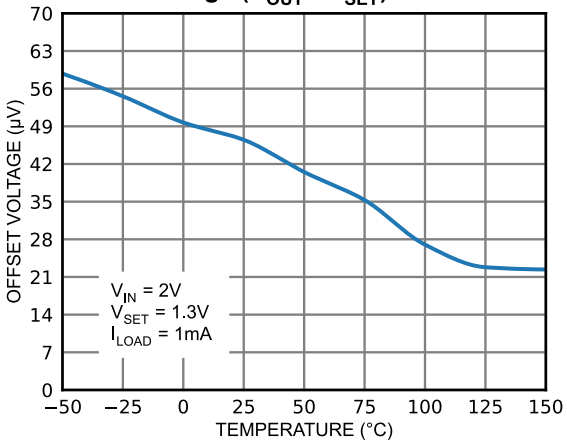
SET Pin Current



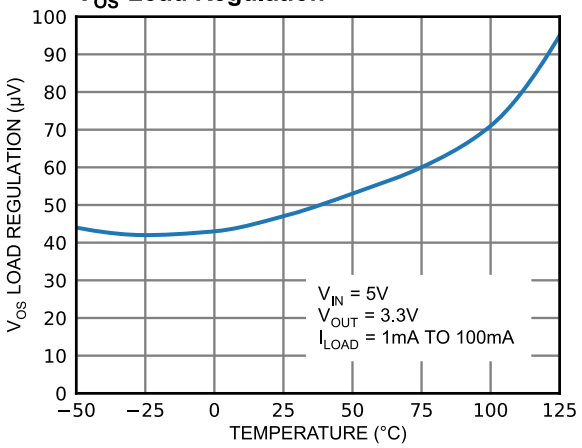
Offset Voltage (V_{OUT} - V_{SET})



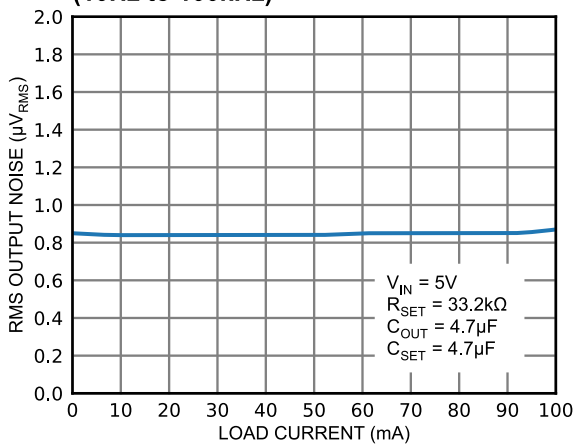
Offset Voltage (V_{OUT} - V_{SET})



V_{OS} Load Regulation



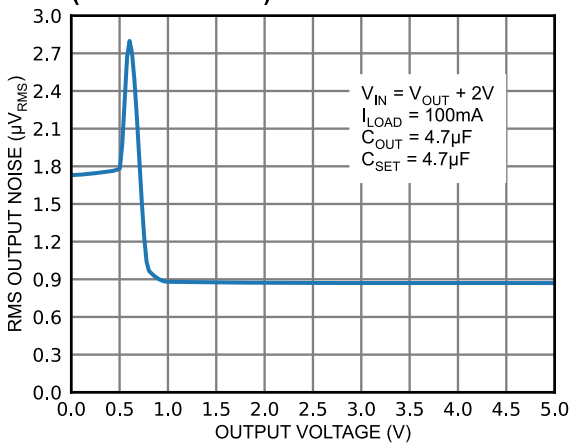
Integrated RMS Output Noise (10Hz to 100kHz)



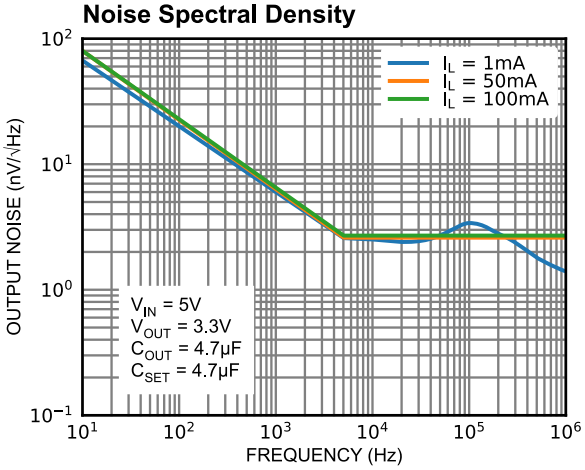
TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

T_A = 25°C, unless otherwise noted.

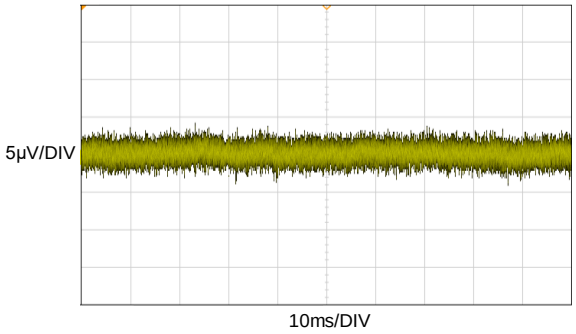
Integrated RMS Output Noise (10Hz to 100kHz)



Noise Spectral Density

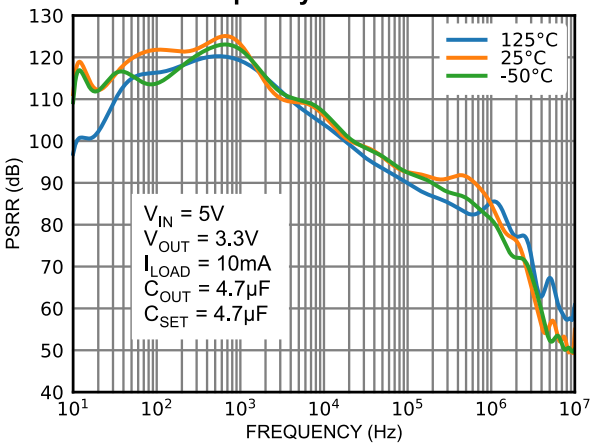


Output Noise: 10Hz to 100kHz

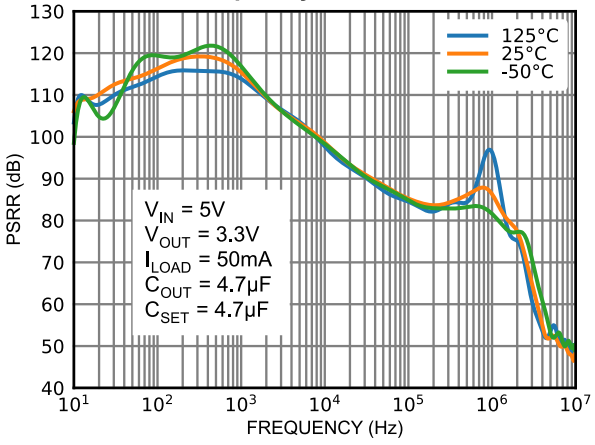


V_{IN} = 5V
R_{SET} = 33.2kΩ
C_{OUT} = 4.7μF
C_{SET} = 4.7μF
I_{LOAD} = 100mA

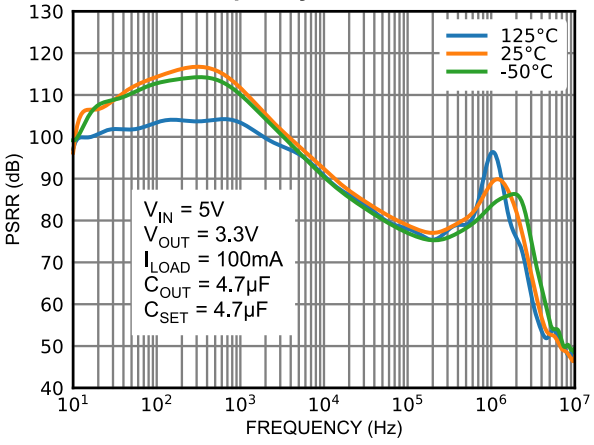
PSRR vs Frequency



PSRR vs Frequency



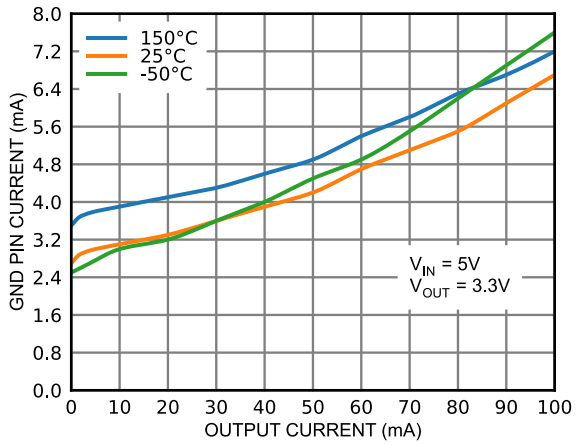
PSRR vs Frequency



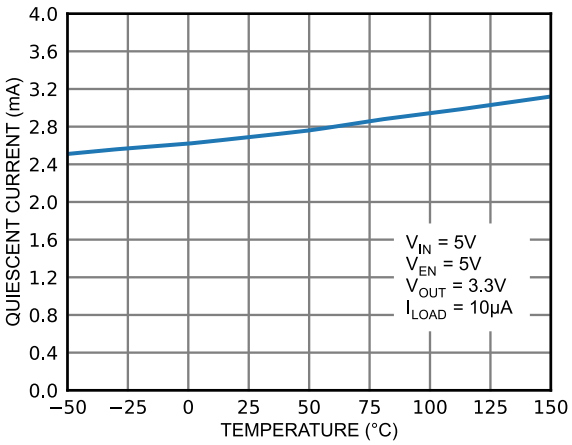
TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

T_A = 25°C, unless otherwise noted.

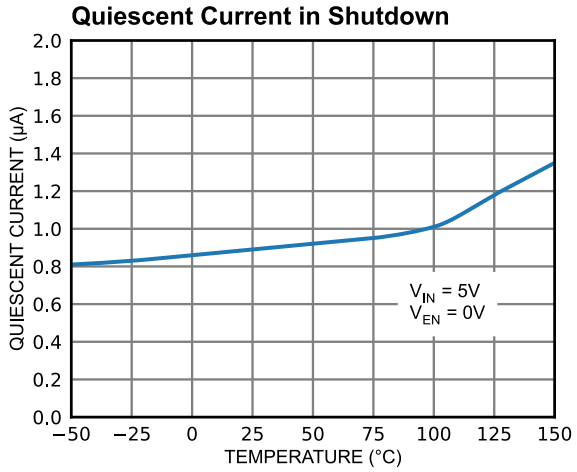
GND Pin Current



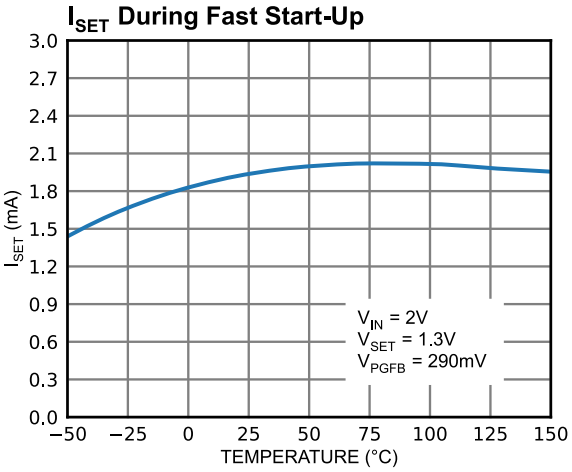
Quiescent Current



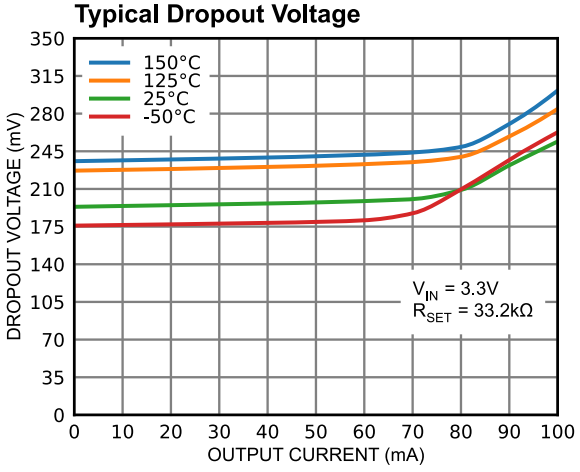
Quiescent Current in Shutdown



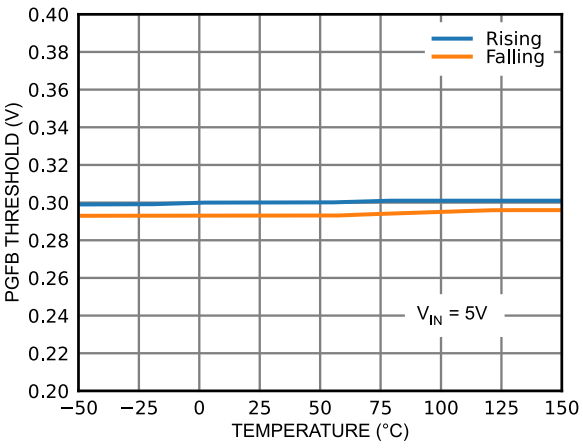
I_{SET} During Fast Start-Up



Typical Dropout Voltage



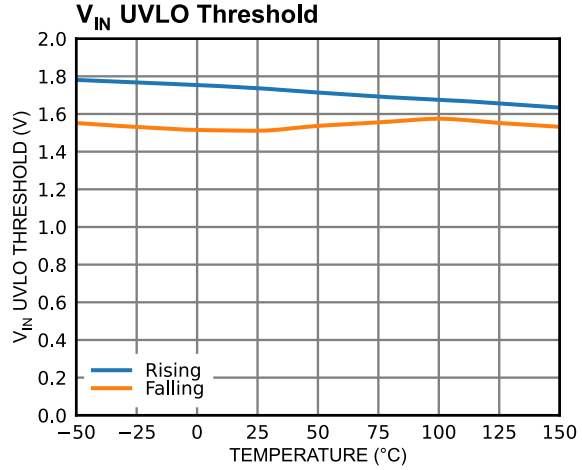
PGFB Threshold



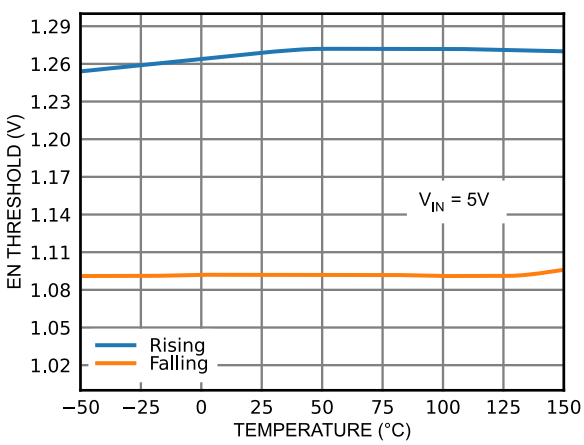
TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

T_A = 25°C, unless otherwise noted.

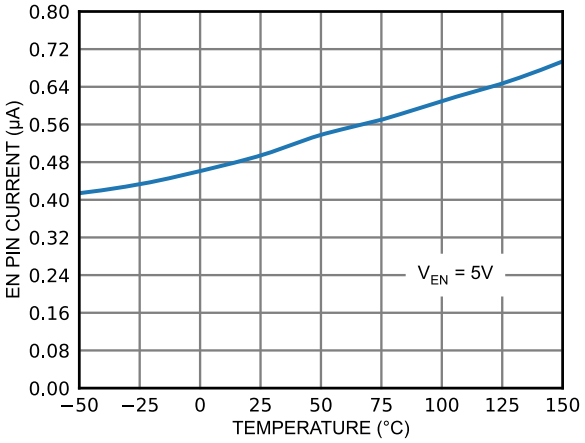
V_{IN} UVLO Threshold



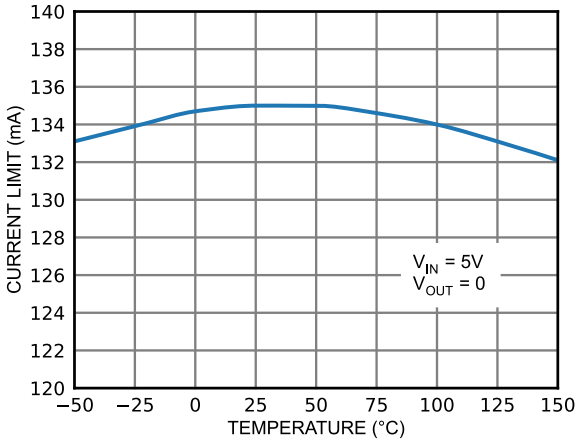
EN Threshold



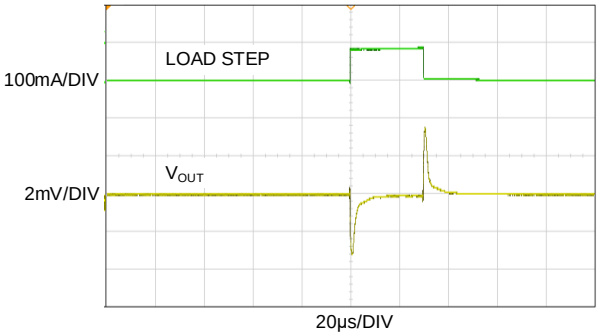
EN Pin Current



Current Limit

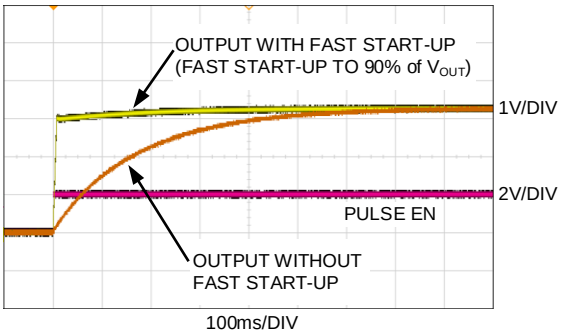


Load Transient Response



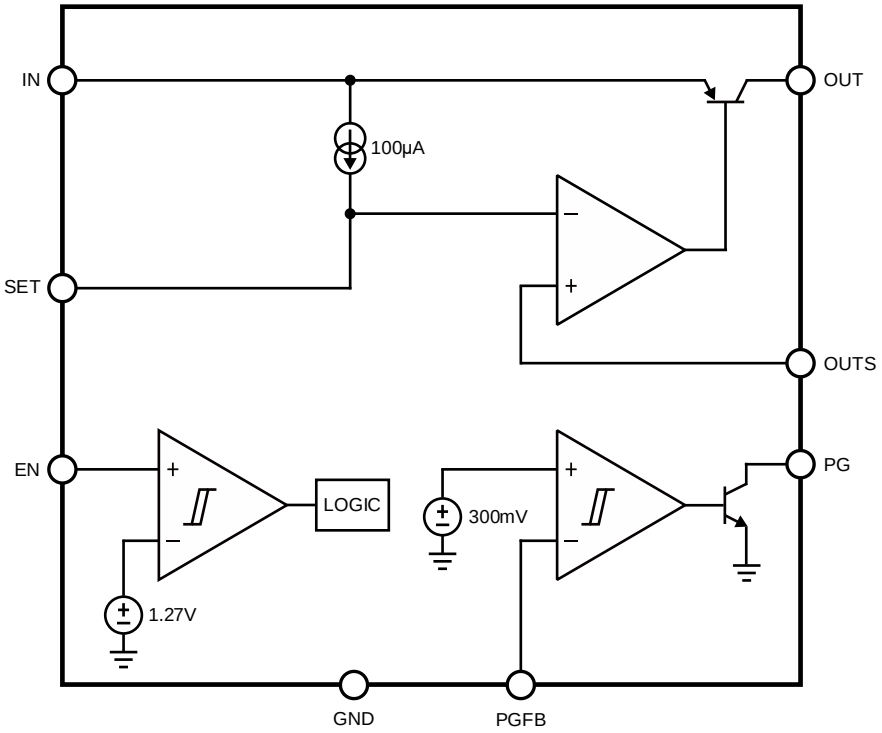
V_{IN} = 5V
R_{SET} = 33.2kΩ
C_{OUT} = 4.7µF
C_{SET} = 4.7µF
LOAD STEP = 10mA TO 100mA

Start-Up Time



V_{IN} = 5V
R_{SET} = 33.2kΩ
C_{OUT} = 4.7µF
C_{SET} = 4.7µF
R_{LOAD} = 33Ω

BLOCK DIAGRAM



OPERATION

The 1033 is an ultralow noise and ultrahigh PSRR LDO for powering noise sensitive applications. It consists of a precision 100μA current reference, an error amplifier and a PNP pass device. With a resistor connected from SET to ground, the current reference flows of the SET pin and generates a reference voltage for the error amplifier. The error amplifier amplifies the difference of the reference voltage and feedback voltage from the output. When the load current increases it causes a reduction in the feedback voltage relative to the reference voltage, the base of the PNP devices will then be puller lower, allowing more current to be delivered and increasing the output voltage.

The 1033 incorporates all the necessary protections including input UVLO, short-circuit and thermal shutdown.

Output Enable/ Undervoltage Lockout (UVLO)

The EN pin is used to put the regulator into a shut-down state. The output voltage is enabled when the EN pin voltage exceeds 1.27V, and disabled when the EN pin voltage is less than 1.09V. If independent enable control of the output is not needed, then tie the EN to the IN pin. Do not float the EN pin. If a resistor divider between IN, EN and GND is used, the EN pin can set an input UVLO threshold to control the output voltage dependently.

Dropout Voltage

Dropout voltage (V_{DROP}) is defined as the $V_{IN} – V_{OUT}$ voltage when $V_{IN} = V_{OUT(NOMINAL)}$. If the input falls below the nominal output regulation, then the output follows the input. The typical dropout voltage of 1033 is 250mV.

Current Limit

The 1033 includes a current limit circuit that limits the maximum output current to 135mA (typical). When the output load exceeds 135mA, the output voltage is reduced to maintain a constant current limit.

Thermal Shutdown

When the 1033 junction temperature exceeds 164°C (typical), the internal thermal shutdown circuit disables the LDO. Thermal shutdown hysteresis assures the LDO resets (turns on) when the temperature falls to 157°C (typical). The internal thermal protection is designed to protect against the device under overload conditions. For reliable operation, limit the junction temperature to a maximum of 125°C.

Power-Good Function

The 1033 includes a power good circuit that monitors the voltage at the power good feedback pin (PGFB) to indicate output voltage regulation. The power good pin (PG) will be pulled high by the external PG resistor if PGFB exceeds 300mV(typical), and will be internally pulled to ground when PGFB falls below 293mV (typical). Connecting a resistor divider between OUT, PGFB and GND sets a programmable power good threshold. If the power good function is not needed, float the PG pin.

Soft-Start and Fast Start-Up

Using a bypass capacitor at the SET pin improves the noise and PSRR performance of the 1033. Also, this bypass capacitor provides the soft-start capability for the output. The ramp-up time of the V_{OUT} (from 0 to 90%, fast start-up disabled) can be expressed as:

$$t_{SS} \approx 2.3 \cdot R_{SET} \cdot C_{SET}$$

For the applications that ultralow noise is expected, the customer may use a larger SET pin bypass capacitor. Normally, this large bypass capacitor will significantly increase the start-up time. The 1033 features the fast start-up capability by increasing the SET pin current to about 2mA to speed up the start-up. This feature is automatically enabled during the start-up when PGFB voltage is below 300mV. When fast start-up is not used, connect PGFB to a voltage higher than 300mV (such as IN pin).

APPLICATION INFORMATION

Adjustable Output

The 1033 has an adjustable output voltage from 0 to 9V given a 2V to 12V input, by using a resistor R_{SET} that connects the SET pin to GND. Use the below equation to calculate the resistor value needed for the desirable output voltage:

$$V_{OUT} = I_{SET} \cdot R_{SET}$$

The SET pin resistor should be a precision resistor to assure that reference voltage is enough accurate． Some factors in PCB may lead to a leakage current in SET pin, so high quality insulation is necessary. Since the SET pin is a high impedance node, a minimum 10nF SET capacitor is suggested to avoid unwanted coupling.

Table 1 lists the resistor value required to achieve a few of the most common rails using commercially available, 1% -tolerance resistors.

Table 1. Recommended SET Resistor Values

V_{OUT} (V)	R_{SET} (kΩ)
1.8	18.2
3.3	33.2
5.0	49.9

Output Sensing

The OUTS pin is the noninverting input to the error amplifier. It's very important to tie the OUTS pin directly to the output capacitor and the GND side of C_{SET} to the GND side of the C_{OUT}, which decreases effects of PCB inductances. Place the GND side of C_{IN} and the GND side of the C_{OUT} as close to each other as possible.

Stability and Capacitance Recommendation

The 1033 is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the output and input pin. For output capacitance, a minimum 4.7μF capacitor with below 50mΩ of ESR and below 2nH ESL is recommended. A large output capacitance can only slightly improve the performance because it decreases the bandwidth of regulator.

Place a high-quality ceramic capacitor with low leakage in SET pin, and thus reduce the impact of current error in SET pin. A typical 4.7μF capacitance bypass capacitor is recommended.

A minimum 4.7μF input ceramic capacitor with low ESR is recommended for the IN pin. Note that using a small ceramic input capacitance might cause the regulator to be instable. Use a larger capacitance ceramic input capacitor if a distantly located supply powers the input pin. The long wire inductance and the input capacitor, form a resonant LC circuit which might lead to the regulator's instability. In addition to using a larger input capacitor, using a series resistor (range from 100mΩ to 500mΩ) between the supply and the input pin of regulator can also stabilize the regulator.

If the IN pin of 1033 is supplied by a switching converter's output in some applications, the ac current at the switching frequency flows through the input capacitor of 1033. Because the input capacitor is close to 1033, the current generates a magnetic field that couples to the 1033 output, which degrades the PSRR performance. The method to reduce the unwanted situation is that removes the input capacitor and places the switching converter's output capacitor far from 1033.

The switching converter's output may introduce very high frequency (larger than 100MHz) ripples to the IN pin of the 1033, which directly affect the output due to a low PSRR performance at very high frequency. A short PCB trace between the switcher's output and the 1033's input, which acts as inductance to a LC-filter, can be used to suppress these very high frequency ripples.

Power Dissipation

The power dissipation in the regulator (P_D) can be calculated as below:

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{LOAD} + V_{IN} \cdot I_{GND}$$

The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction to ambient thermal resistance of the package (θ_{JA}). Using the following equation to calculate the maximum junction temperature:

$$T_J = T_A + P_D \cdot \theta_{JA}$$

The junction to ambient thermal resistance is highly dependent on the PCB layout. Careful attention to PCB thermal design is required if high maximum power dissipation exists in the application.

PCB Layout Guide

PCB layout is very important to achieve good regulation, ripple rejection and thermal performance. Place input capacitor and output capacitor close to each other, and tie the GND side of C_{SET} directly to the GND side of C_{OUT}. For further details, please refer to Figure 1 for the example layout.

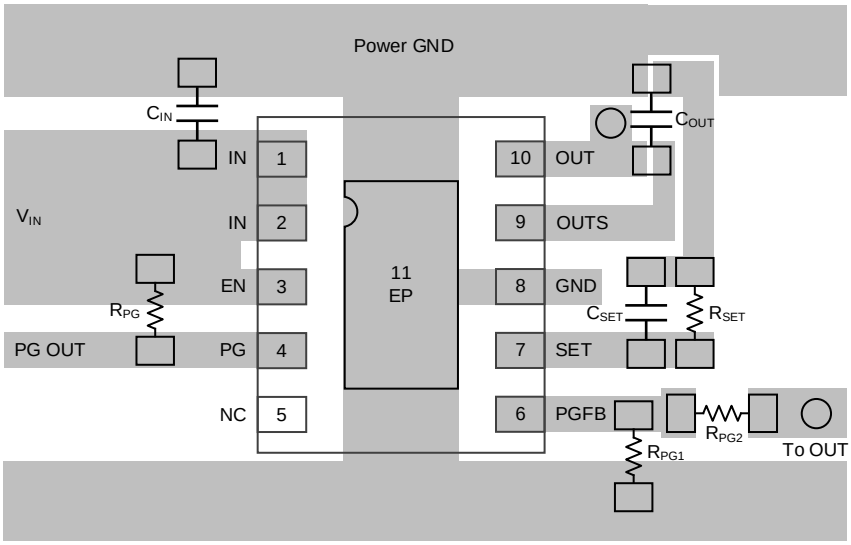


Figure 1. 1033 Example Layout

TYPICAL APPLICATION CIRCUITS

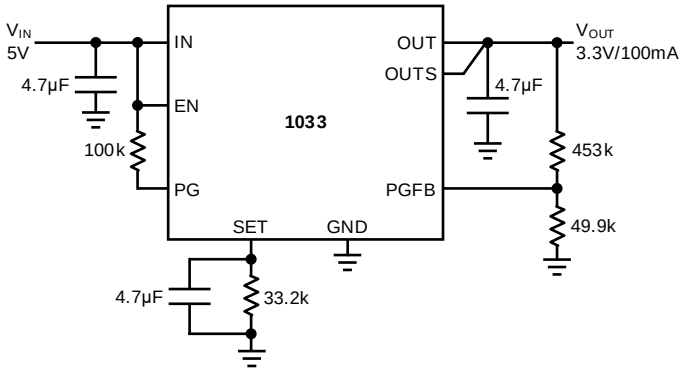
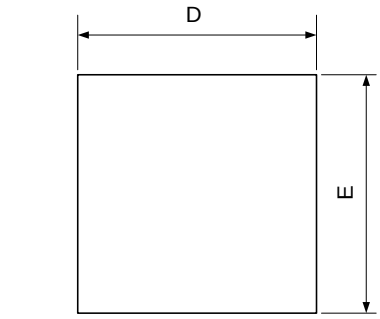


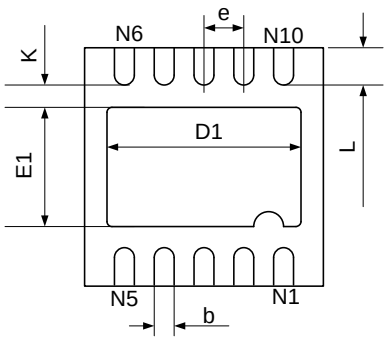
Figure 2. Typical Application Circuit

PACKAGE OUTLINE

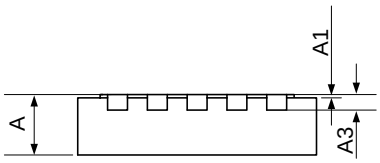
DFN-10-3x3x0.75-0.5 **UNIT: mm**



Top View



Bottom View



Side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.700	—	0.800
A1	0	—	0.050
A3	0.203 REF		
D	2.900	3.000	3.100
E	2.900	3.000	3.100
D1	2.300	—	2.500
E1	1.600	—	1.800
b	0.200	—	0.300
e	0.500 TYP		
K	0.200	—	—
L	0.300	0.400	0.500

Important notice:

1. **The instructions are subject to change without notice!**
2. **Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current. Please read the instructions carefully before using our products, including the circuit operation precautions.**
3. **Our products are consumer electronic products or the other civil electronic products.**
4. **When using our products, please do not exceed the maximum rating of the products, otherwise the reliability of the whole machine will be affected. There is a certain possibility of failure or malfunction of any semiconductor product under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design, sample and whole machine manufacturing, so as to avoid potential failure risk that may cause personal injury or property loss.**
5. **It is strongly recommended to identify the trademark when buying our products. Please contact us if there is any question.**
6. **Product promotion is endless, our company will wholeheartedly provide customers with better products!**

Part No.:	1033

Rev.	1.1	Date	2024-03-12

Description:

1. Update maximum output voltage from 8V to 9V.
2. Some minor changes to ELECTRICAL CHARACTERISTICS table.

Rev.	1.0	Date	2022-06-18

Description:

1. First release.