General Description

The AGM60P20EY combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$

This device is ideal for load switch and battery protection applications.

Features

- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance
- 100% Avalanche tested
- 100% DVDS tested

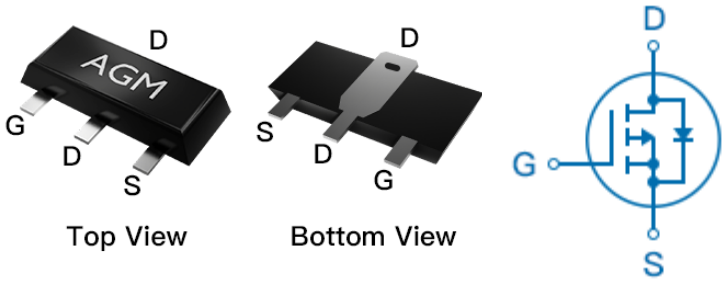
Application

- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

Product Summary

BVDSS	RDSON	ID
-60V	54mΩ	-8A

SOT89-3 Pin Configuration



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM60P20EY	AGM60P20EY	SOT89-3	330mm	12mm	3000

Table 1. Absolute Maximum Ratings (TC=25℃)

Symbol	Parameter	Value	Unit
VDS	Drain-Source Voltage (VGS=0V)	-60	V
VGS	Gate-Source Voltage (VDS=0V)	±20	V
ID	Drain Current-Continuous(TC=25℃) **(Note 1)**	-8.0	A
	Drain Current-Continuous(TC=100℃)	-5.3	A
IDM (pluse)	Drain Current-Pulsed **(Note 2)**	-32	A
PD	Maximum Power Dissipation(TC=25℃)	8.5	w
EAS	Avalanche energy **(Note 3)**	31	mJ
TJ,TSTG	Operating Junction and Storage Temperature Range	-55 To 150	℃

Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
RθJA	Thermal Resistance Junction-ambient (Steady State)[1]	---	62.5	℃/W
RθJC	Thermal Resistance Junction-Case[1]	---	14.7	℃/W

Table 3. Electrical Characteristics (TJ=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	VGS=0V ID=-250μA	-60	--	--	V
IDSS	Zero Gate Voltage Drain Current	VDS=-60V,VGS=0V	--	--	-1	μA
IGSS	Gate-Body Leakage Current	VGS=±20V,VDS=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	VDS=VGS,ID=-250μA	-1.2	--	-2.2	V
gFS	Forward Transconductance	VDS=5V,ID=-4A	--	7.0	--	S
RDS(on)	Drain-Source On-State Resistance	VGS=-10V, ID=-5A	--	54	80	mΩ
		VGS=-4.5V, ID=-4A	--	69	115	mΩ
Dynamic Characteristics						
Ciss	Input Capacitance	VDS=30V,VGS=0V, F=1MHZ	--	525	--	pF
Coss	Output Capacitance		--	80	--	pF
Crss	Reverse Transfer Capacitance		--	3.9	--	pF
Rg	Gate resistance	f=1.0MHz	--	3.5	--	Ω
Switching Times						
td(on)	Turn-on Delay Time	VGS=-10V,VDS=-30V, ID=-3.5A,RGEN=3Ω	--	10	--	nS
tr	Turn-on Rise Time		--	6.0	--	nS
td(off)	Turn-Off Delay Time		--	40	--	nS
tf	Turn-Off Fall Time		--	13	--	nS
Qg	Total Gate Charge	VGS=-10V, VDS=-30V, ID=-3.5A	--	10.5	--	nC
Qgs	Gate-Source Charge		--	2.8	--	nC
Qgd	Gate-Drain Charge		--	1.5	--	nC
Source-Drain Diode Characteristics						
ISD	Source-Drain Current(Body Diode)		--	--	-8.0	A
VSD	Forward on Voltage	VGS=0V,IS=-5A	--	--	-1.2	V
trr	Reverse Recovery Time	Isd=-5A , dI/dt=100A/μs , TJ=25℃	--	50	--	ns
Qrr	Reverse Recovery Charge		--	105	--	nc

Notes 1.The maximum current rating is package limited.

Notes 2.Repetitive Rating: Pulse width limited by maximum junction temperature.

Notes 3.EAS condition: TJ=25℃,VDD=-30V,Vgs=-10V,ID=-25A, L=0.1mH,RG=25ohm

Characteristics Curve：

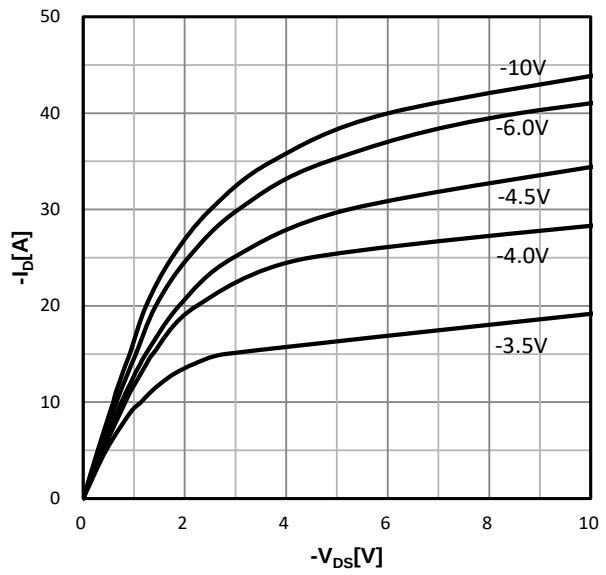
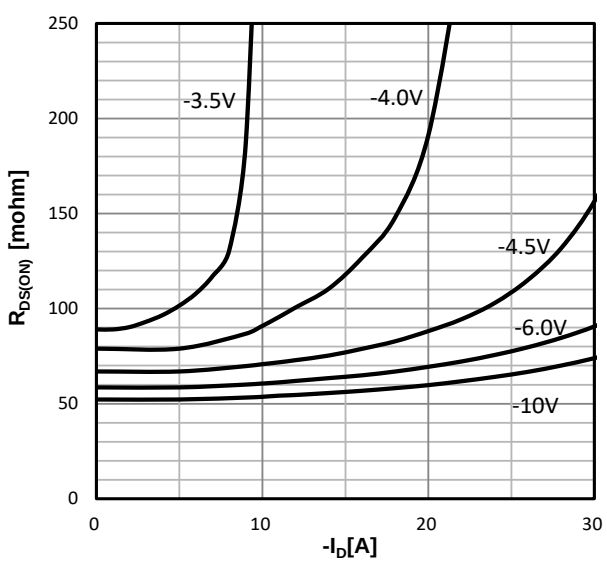
Figure 1: Typ. output characteristics	Figure 2: Typ. drain-source on resistance
	
$I_D=f(V_{DS})$, T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}=f(I_D)$, T_j=25 °C; parameter: V_{GS}

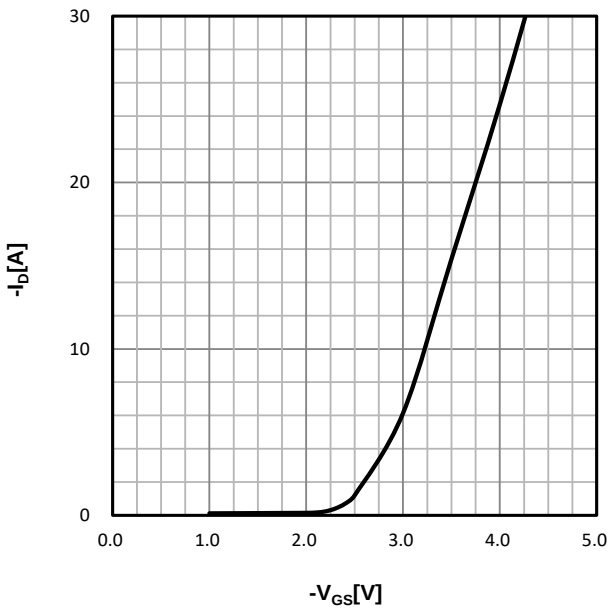
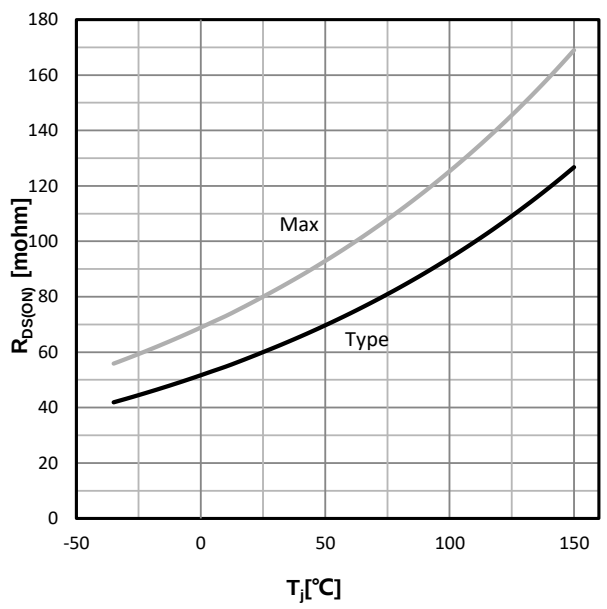
Figure 3: Typ. transfer characteristics	Figure 4: drain-source on resistance
	
$I_D=f(V_{GS})$, $\|V_{DS}\|>2\|I_D\|R_{DS}(on)max$;	$R_{DS(on)}=f(T_j)$, I_D=-3.5A, V_{GS}=-10V;

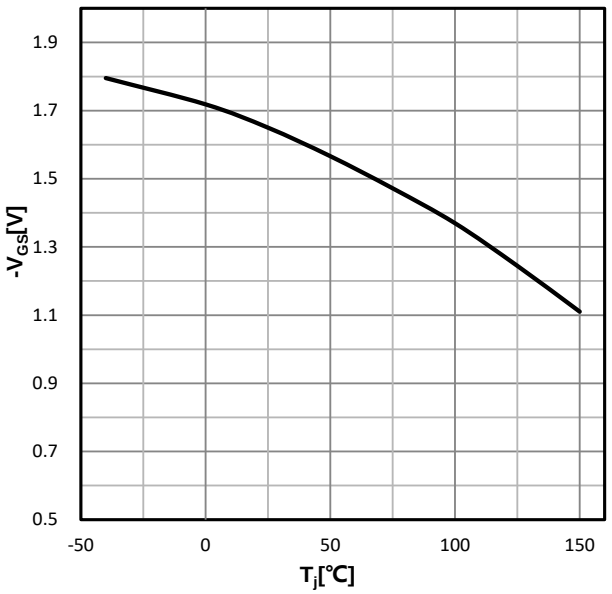
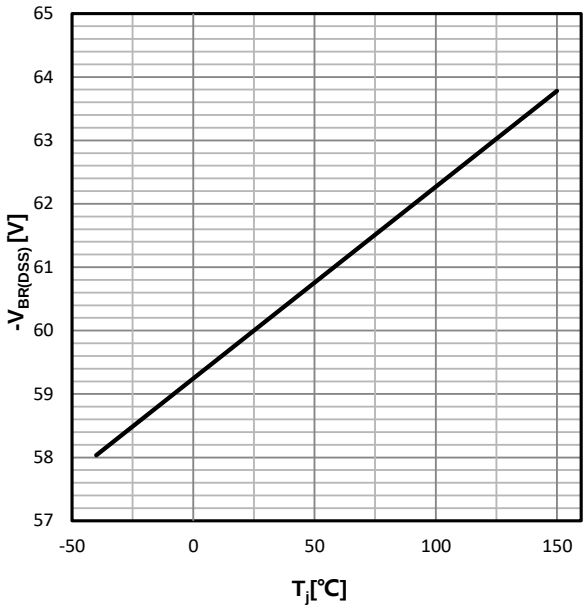
Figure 5: Typ. gate threshold voltage	Figure 6: Drain-source breakdown voltage
	
V_{GS}=f(T_j), V_{GS}=$V_{DS,}$ I_D=-250μA;	$V_{BR(DSS)}$=f(T_j); I_D=-250μA;

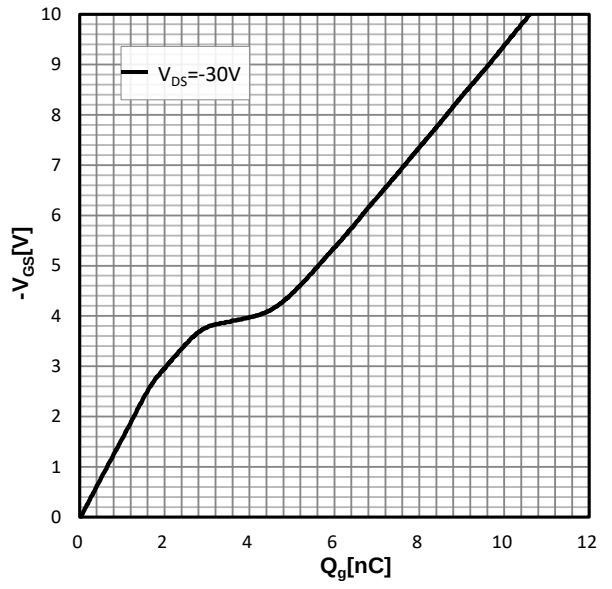
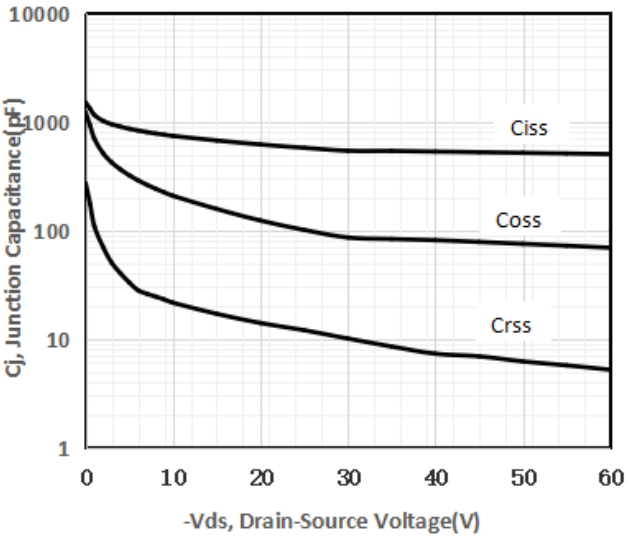
Figure 7: Typ. gate charge	Figure 8: Typ. Capacitances
	
V_{GS}=f(Q_g), I_D=-3.5A, T_j=25 °C; parameter: V_{DS}	C=f(V_{DS}); V_{GS}=0V; f=1.0 MHz;

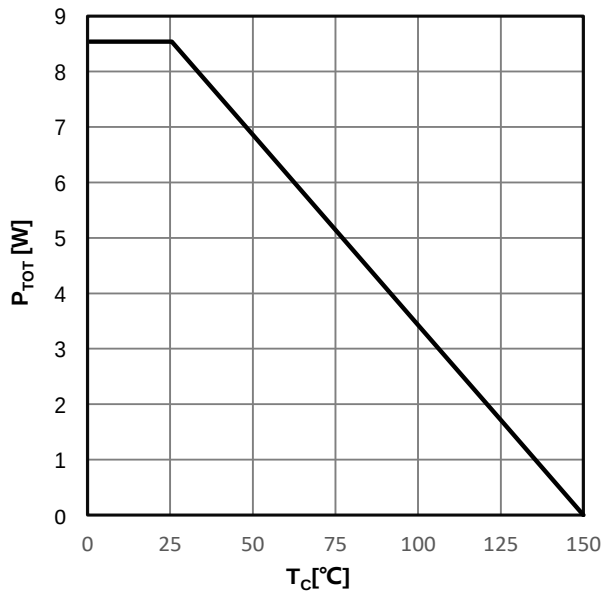
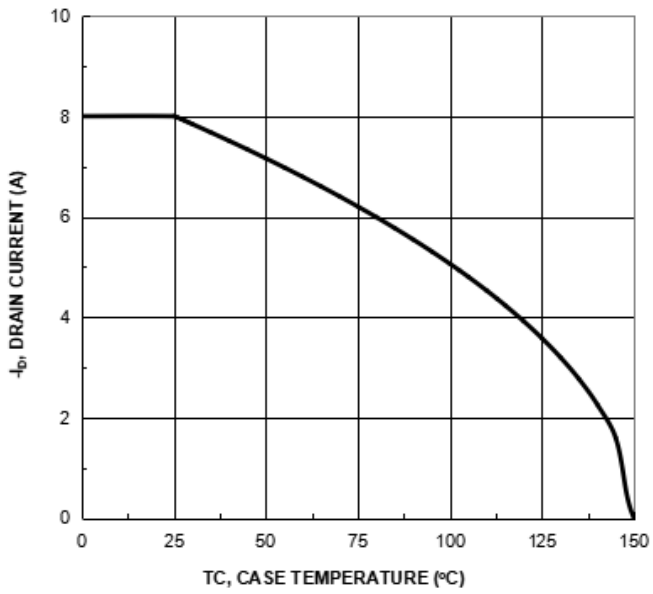
Figure 9: Power dissipation	Figure 10:Drain current
	
$P_{tot}=f(T_C)$;	$I_D=f(T_C)$;

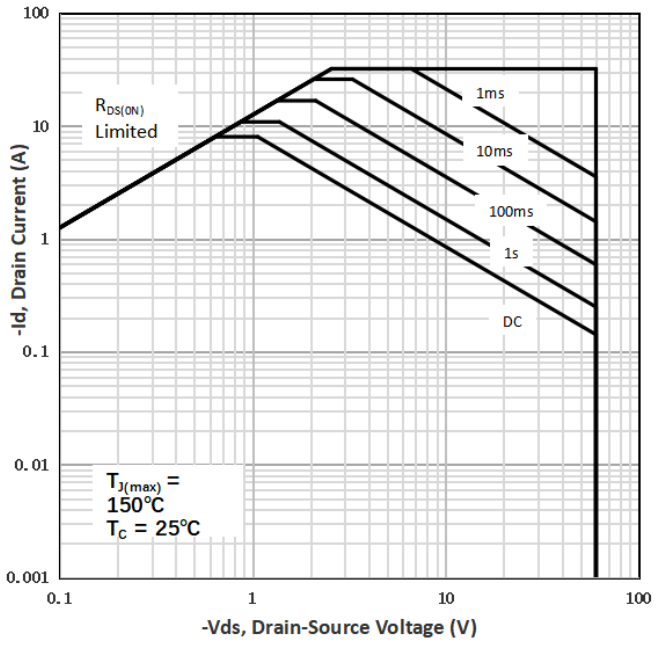
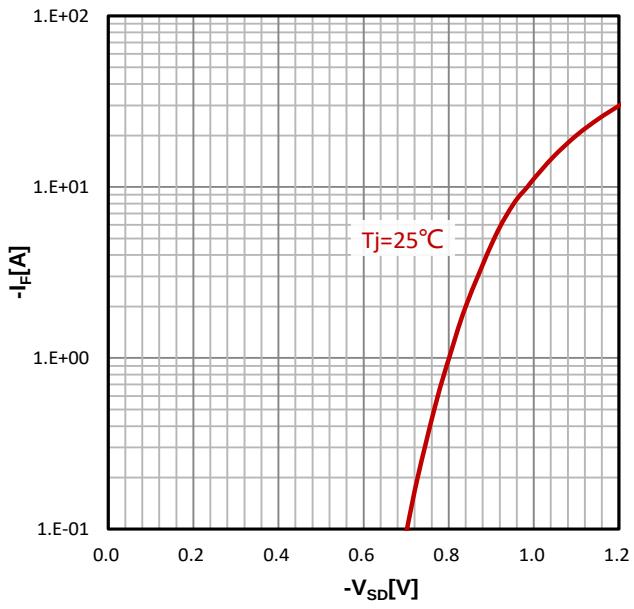
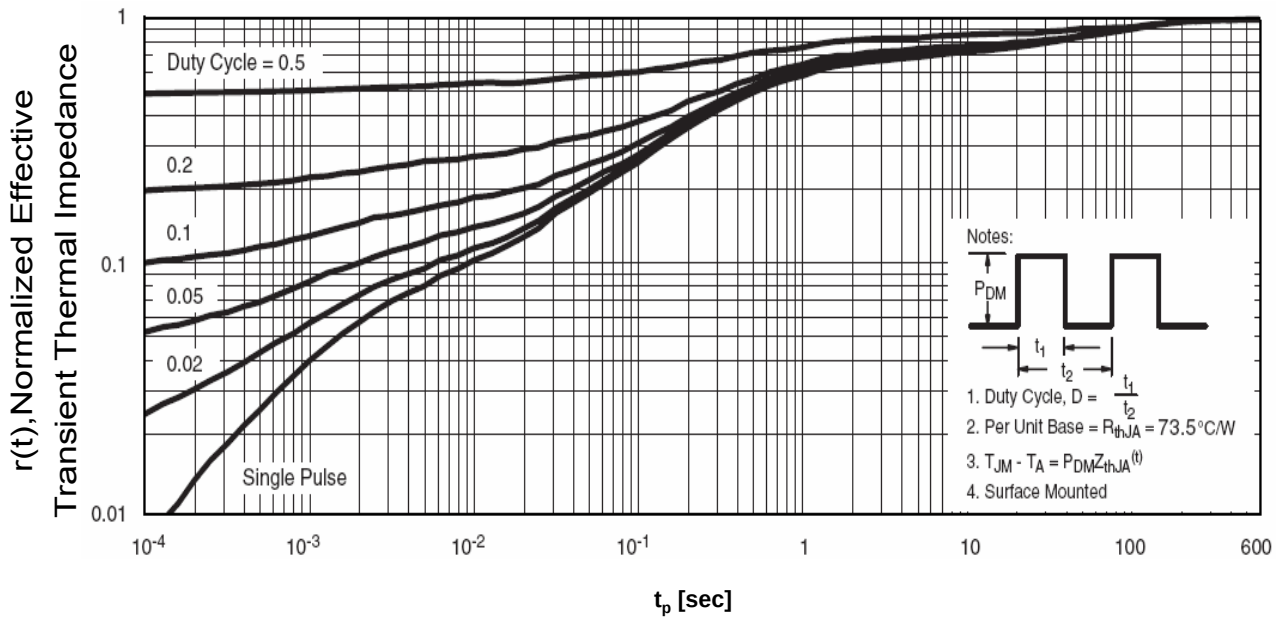
Figure 11: Safe operating area	Figure 12: Typ. forward characteristics
	
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: tp	$I_F=f(V_{SD})$;

Figure 13: Max. Transient Thermal Impedance



$Z_{thJA}=f(t_p)$; parameter: D

Test Circuit & Waveform:

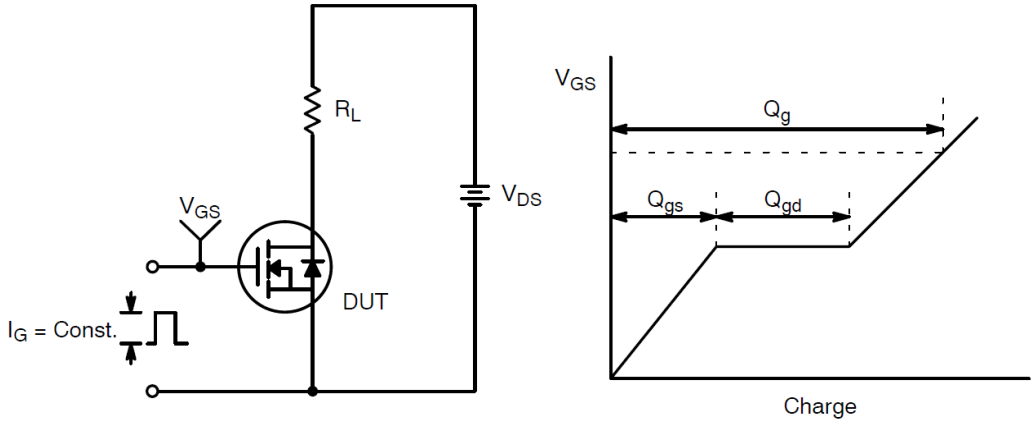


Figure 14: Gate Charge Test Circuit & Waveform

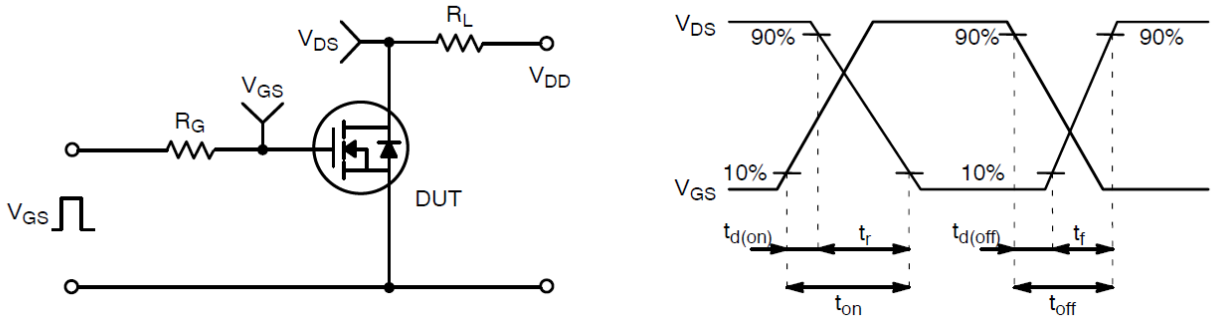


Figure 15: Resistive Switching Test Circuit & Waveforms

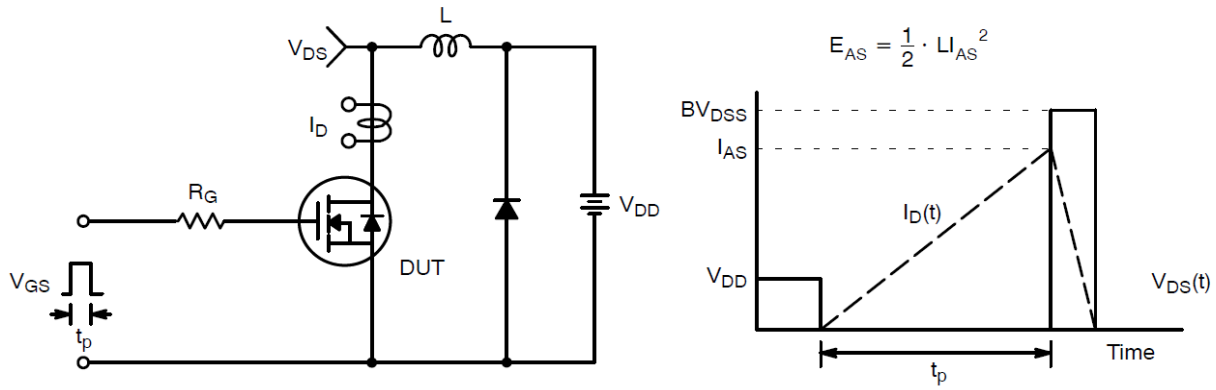
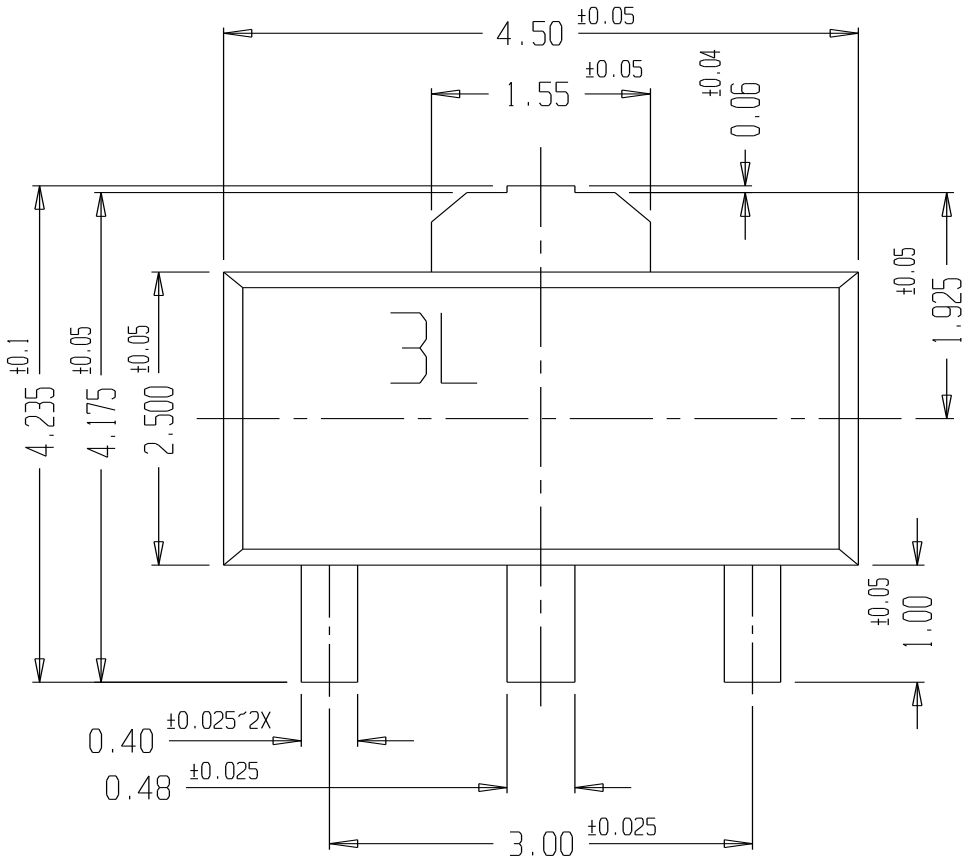


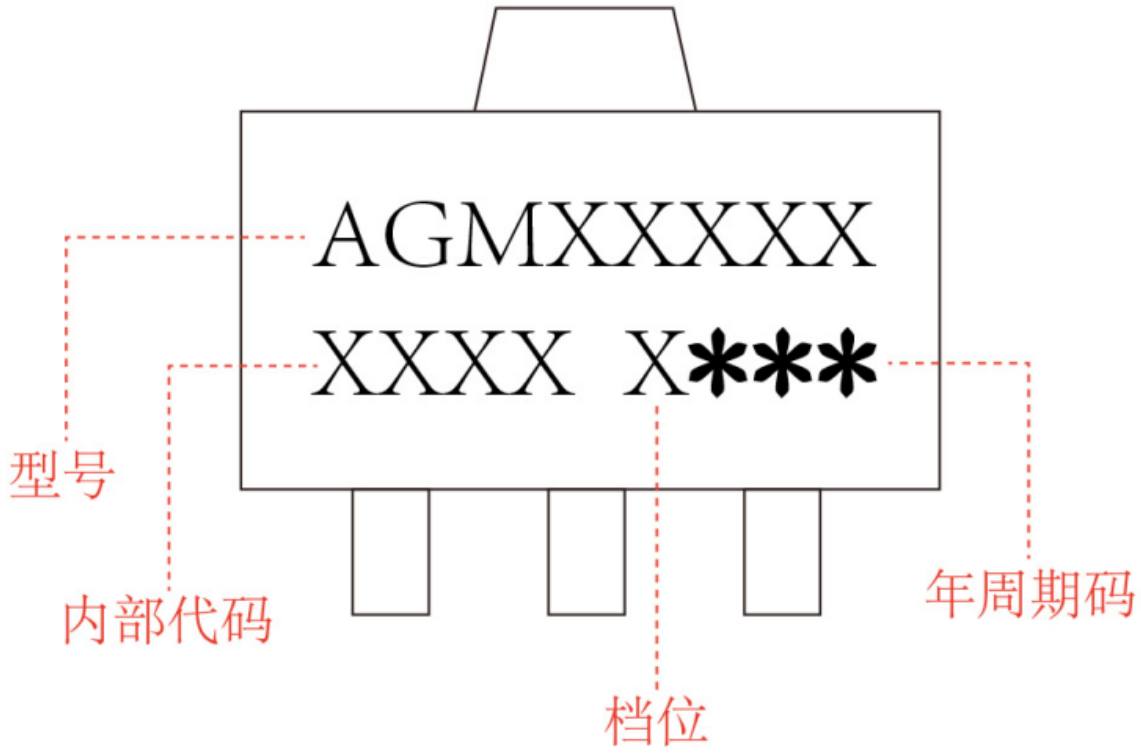
Figure 16: Unclamped Inductive Switching Test Circuit & Waveforms

●**Dimensions (**SOT89**-3)**



SOT89-3

Marking Instructions:



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