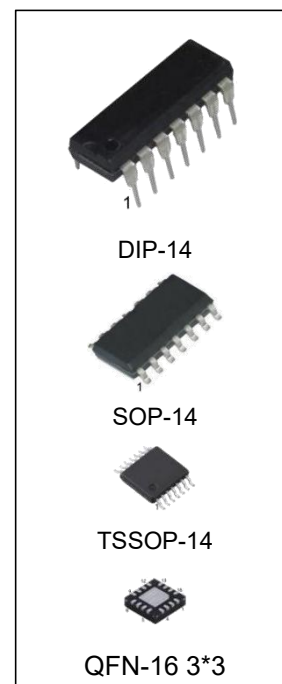


Features

- Wide supply voltage range from 3V to 15V
- Fully static operation
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from -40°C to +105°C
- Packaging information: DIP-14/SOP-14/TSSOP-14/QFN-16



Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
CD4068BE/ CD4068BN	DIP-14	CD4068B	TUBE	1000pcs/Box
CD4068BM/TR	SOP-14	CD4068B	REEL	2500pcs/Reel
CD4068BMT/TR	TSSOP-14	CD4068B	REEL	2500pcs/Reel
CD4068BLQ/TR	QFN-16 3*3	4068B	REEL	5000pcs/Reel

General Description

The CD4068B is an 8-input And Gate/Nand Gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity to output impedance variations.

It operates over a recommended VDD power supply range of 3V to 15V referenced to VSS (usually ground). Unused inputs must be connected to VDD, VSS, or another input.

Block Diagram

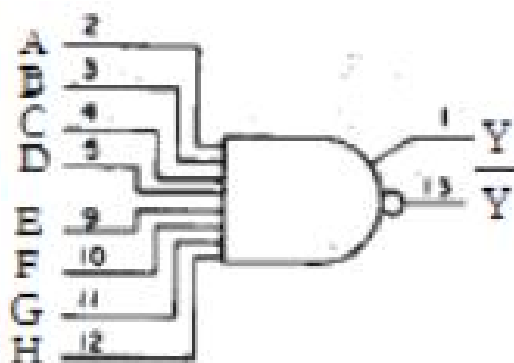


Figure 1. Functional diagram

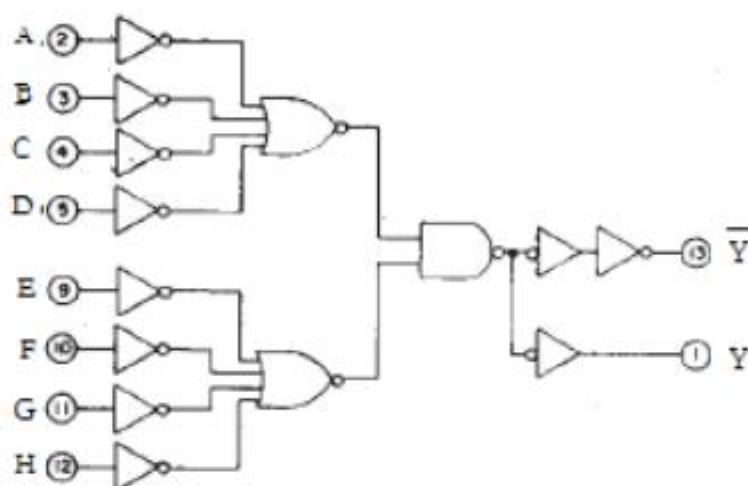
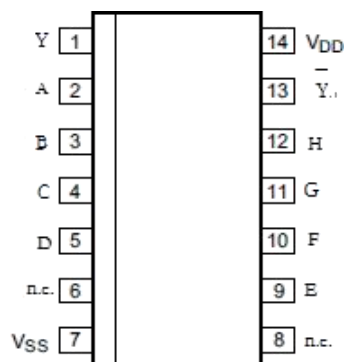


Figure 2. Logic diagram

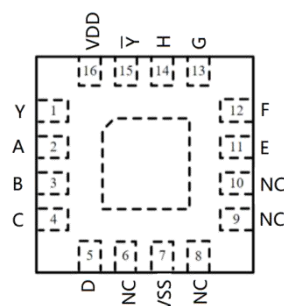
Function Table

Input								Output	
A	B	C	D	E	F	G	H	Y	$\bar{Y}$
H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	H
X	L	X	X	X	X	X	X	L	H
X	X	L	X	X	X	X	X	L	H
X	X	X	L	X	X	X	X	L	H
X	X	X	X	L	X	X	X	L	H
X	X	X	X	X	L	X	X	L	H
X	X	X	X	X	X	L	X	L	H
X	X	X	X	X	X	X	L	L	H

Pin Configurations



DIP-14,SOP-14,TSSOP-14



QFN-16 3*3

Pin No.		Pin Name	Description
DIP/SOP/TSSOP	DFN-16		
1	1	Y	data output
2	2	A	data input
3	3	B	data output
4	4	C	data output
5	5	D	data input
6	6	n.c.	not connected
7	7	VSS	ground (0V)
8	10	n.c.	not connected
9	11	E	data input
10	12	F	data output
11	13	G	data output
12	14	H	data input
13	15	$\bar{Y}$	complement output
14	16	VDD	supply voltage
-	8	NC	not connected
-	9	NC	not connected

Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	VDD	-	-0.5	+18	V
DC input current	I _{IK}	any one input	-	±10	mA
input voltage	V _I	all inputs	-0.5	V _{DD} +0.5	V
storage temperature	T _{stg}	-	-65	+150	°C
total power dissipation	P _{tot}	-	-	500	mW
device dissipation	P	per output transistor	-	100	mW
Soldering temperature	TL	10s	260		°C

Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V _{DD}	-	3	-	15	V
ambient temperature	T _{amb}	in free air	-40	-	+85	°C

Note:

- (1) For DIP14 packages: above 70°C the value of P_{tot} derates linearly with 12mW/K.
- (2) For SOP14 packages: above 70°C the value of P_{tot} derates linearly with 8mW/K.
- (3) For (T)SSOP14 packages: above 60°C the value of P_{tot} derates linearly with 5.5mW/K.

Electrical Characteristics

DC Characteristics 1

(T_{amb}=25°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)			T _{amb} =25°C			Unit
		V _O	V _{IN}	V _{DD}	Min.	Typ.	Max.	
supply current	I _{DD}	-	0, 5	5	-	0.01	5	uA
		-	0, 10	10	-	0.01	10	uA
		-	0, 15	15	-	0.01	15	uA
LOW-level output current	I _{OL}	0.4	0, 5	5	0.51	1	-	mA
		0.5	0, 10	10	1.3	2.6	-	mA
		1.5	0, 15	15	3.4	6.8	-	mA
HIGH-level output current	I _{OH}	4.6	0, 5	5	-0.51	-1	-	mA
		2.5	0, 5	5	-1.6	-3.2	-	mA
		9.5	0, 10	10	-1.3	-2.6	-	mA
		13.5	0, 15	15	-3.4	-6.8	-	mA
LOW-level output voltage	V _{OL}	-	0, 5	5	-	0	0.05	V
		-	0, 10	10	-	0	0.05	V
		-	0, 15	15	-	0	0.05	V
HIGH-level output voltage	V _{OH}	-	0, 5	5	4.95	5	-	V
		-	0, 10	10	9.95	10	-	V
		-	0, 15	15	14.95	15	-	V
LOW-level input voltage	V _{IL}	0.5, 4.5	-	5	-	-	1.5	V
		1, 9	-	10	-	-	3	V
		1.5, 13.5	-	15	-	-	4	V
HIGH-level input voltage	V _{IH}	0.5, 4.5	-	5	3.5	-	-	V
		1, 9	-	10	7	-	-	V
		1.5, 13.5	-	15	11	-	-	V
input leakage current	I _I	-	0, 15	15	-	±10 ⁻⁵	±0.1	uA

DC Characteristics 2

($T_{amb}=-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)			$T_{amb}=-40^{\circ}\text{C}$		$T_{amb}=+85^{\circ}\text{C}$		$T_{amb}=+105^{\circ}\text{C}$		Unit
		VO	VIN	VDD	Min.	Max.	Min.	Max.	Min.	Max.	
supply current	I_{DD}	-	0, 5	5	-	0.25	-	7.5	-	7.5	uA
		-	0, 10	10	-	0.5	-	15	-	15	uA
		-	0, 15	15	-	1	-	30	-	30	uA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.61	-	0.42	-	0.36	-	mA
		0.5	0, 10	10	1.5	-	1.1	-	0.9	-	mA
		1.5	0, 15	15	4	-	2.8	-	2.4	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-0.61	-	-0.42	-	-0.36	-	mA
		2.5	0, 5	5	-1.8	-	-1.3	-	-1.15	-	mA
		9.5	0, 10	10	-1.5	-	-1.1	-	-0.9	-	mA
		13.5	0, 15	15	-4	-	-2.8	-	-2.4	-	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	0.05	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	-	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	-	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	14.95	-	V
LOW-level input voltage	V_{IL}	0.5, 4.5	-	5	-	1.5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	-	3	V
		1.5, 13.5	-	15	-	4	-	4	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	11	-	V
input leakage current	I_I	-	0, 15	15	-	± 0.1	-	± 1	-	± 1	uA

AC Characteristics

($T_{amb}=25^{\circ}\text{C}$, $V_{SS}=0\text{V}$, $t_r, t_f=20\text{ns}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay time	t_{PHL}, t_{PLH}	see Figure 4	$V_{DD}=5\text{V}$	-	150	300	ns
			$V_{DD}=10\text{V}$	-	75	150	ns
			$V_{DD}=15\text{V}$	-	55	110	ns
transition time	t_{THL}, t_{TLH}	see Figure 4	$V_{DD}=5\text{V}$	-	100	200	ns
			$V_{DD}=10\text{V}$	-	50	100	ns
			$V_{DD}=15\text{V}$	-	40	80	ns
input capacitance	C_I	any input		-	5	7.5	pF

AC Testing Circuit

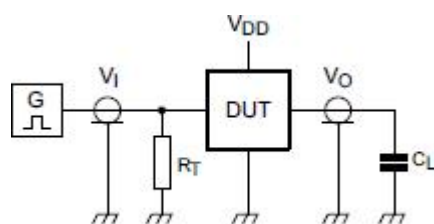


Figure 3. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

AC Testing Waveforms

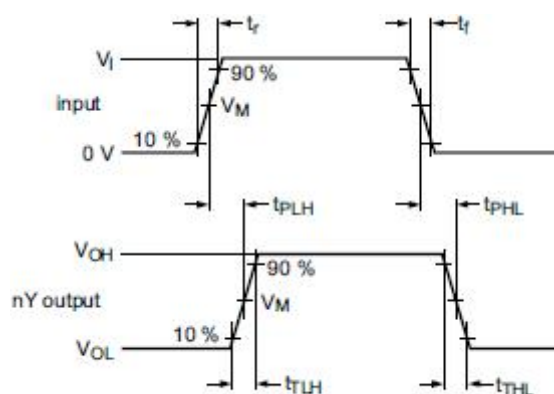


Figure 4. Input to output propagation delay and output transition times

Measurement Points

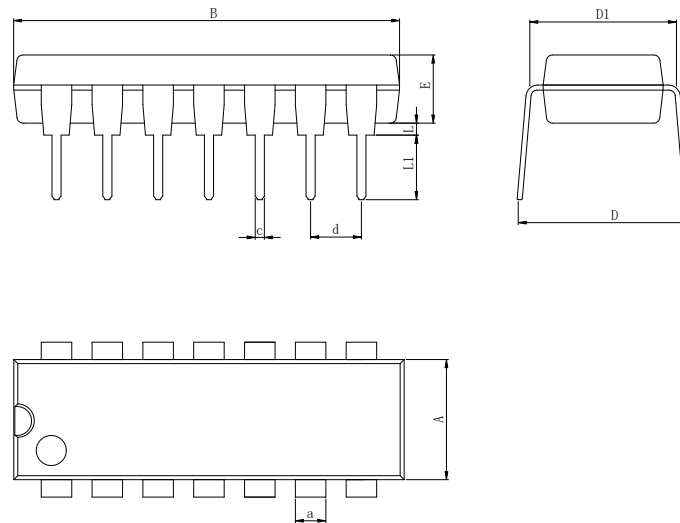
Supply voltage	Input	Output
VDD	VM	VM
5V to 15V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

Test Data

Supply voltage	Input		Load
VDD	VI	tr , tf	CL
5V to 15V	VSS or VDD	$\leq 20\text{ns}$	50pF

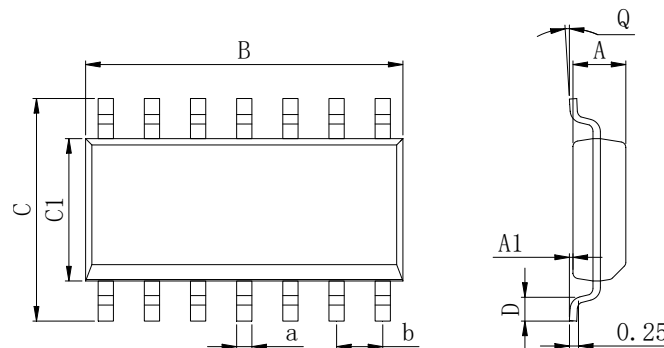
Physical Dimensions

DIP-14



Dimensions In Millimeters(DIP-14)										
Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.50	

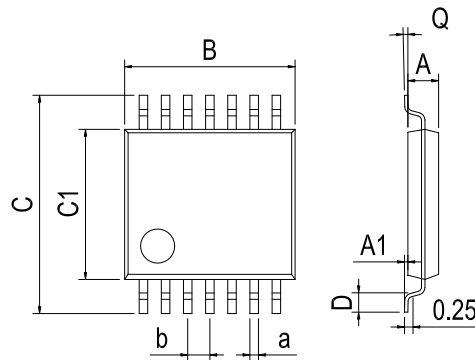
SOP-14



Dimensions In Millimeters(SOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	

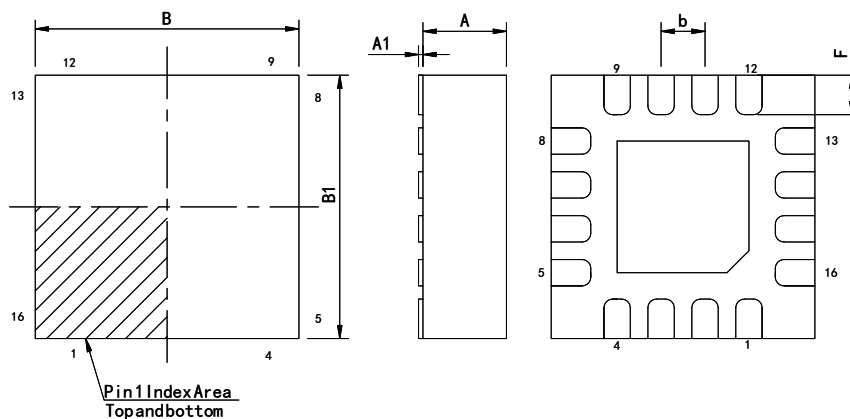
Physical Dimensions

TSSOP-14



Dimensions In Millimeters(TSSOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

QFN-16 3*3



Dimensions In Millimeters(QFN-16 3*3)								
Symbol:	A	A1	B	B1	E	F	a	b
Min:	0.85	0	2.90	2.90	0.15	0.25	0.18	0.50TYP
Max:	0.95	0.05	3.10	3.10	0.25	0.45	0.30	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2012-3	New	1-10
V1.1	2018-11	Updated DIP-14 dimension、Add annotation for Maximum Ratings	3、 7
V1.2	2021-9	Update encapsulation type、 Update DIP Package New Model	1
V1.3	2024-11	Add the QFN-16 package device、 Update Lead Temperature	1、 3
V1.4	2025-5	Update the maximum supply current	4

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