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Product Specification

XBLW XCP82C55

CMOS Programmable Peripheral Interface

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Description

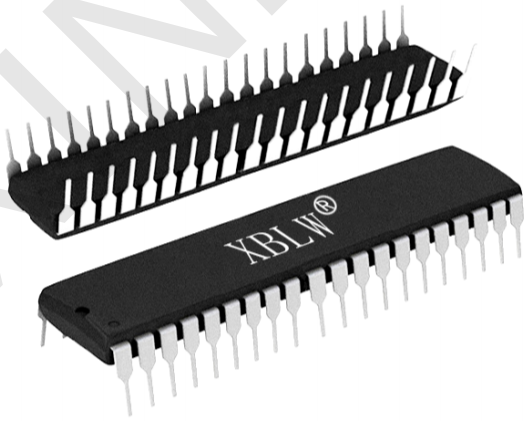
XCP82C55 is a general purpose programmable I/O expansion circuit. The circuit provides 3 sets (PA, PB, PC) programmable universal I/O pins, each port can be programmed as input or output bits. The circuit is controlled through an 8-bit parallel data bus, and there are three operating modes.

Features

- Low power consumption
- Three sets of 8 bits (24 in total) programmable I/O pins
- Single bit setting and reset function
- Communication interface: 8-bit parallel port
- Working voltage: 5V
- Package form: DIP-40

Applications

- Industrial control system
- Communication equipment
- Computer system
- Printer, keyboard

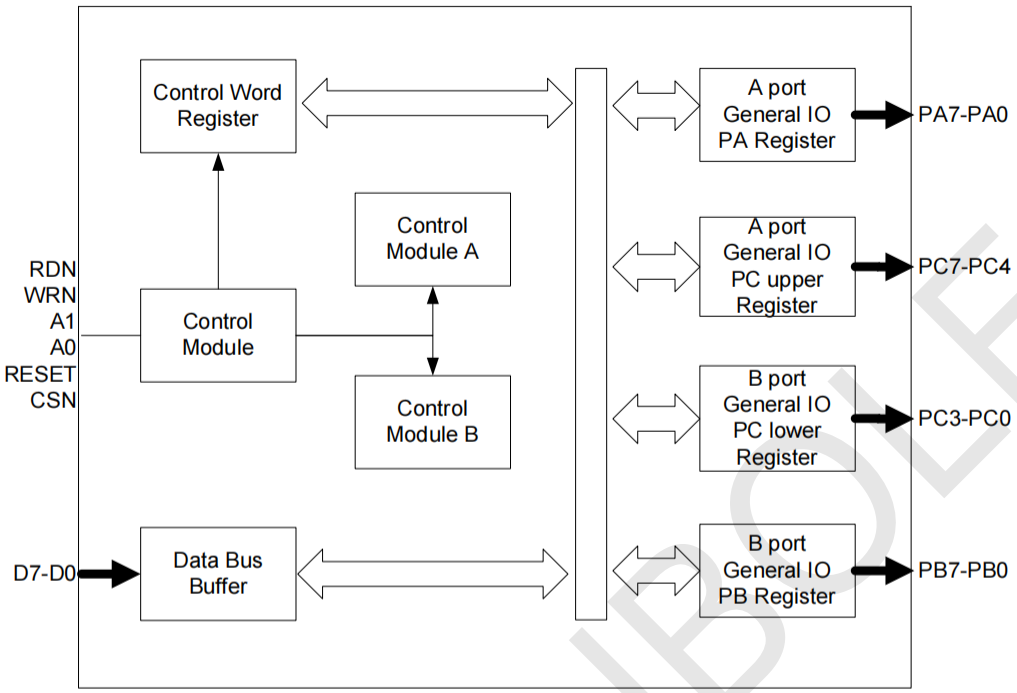


DIP-40

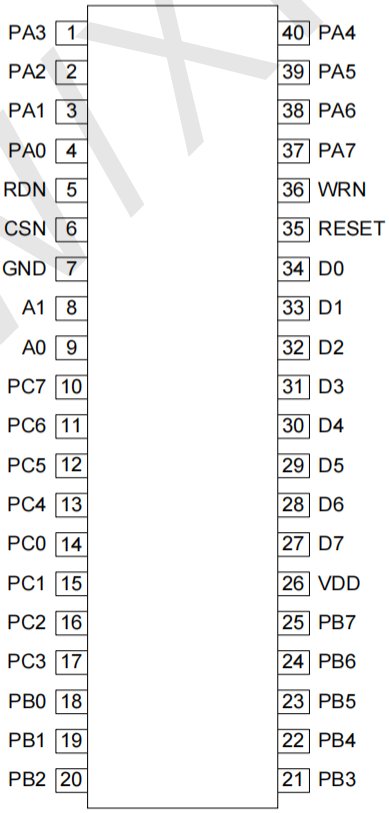
Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW XCP82C55AZ	DIP-40	XCP82C55AZ	Tube	264Pcs/Box

Functional block diagram



Pin arrangement diagram



Description of pin

Pin No.	Symbol	I/O	Description
1-4，37-40	PA0-7	I/O	Port A, universal I/O port. The data direction and pattern are determined by the control word
18-25	PB0-7	I/O	Port B, general purpose I/O port. The data direction and pattern are determined by the control word
14-17	PC0-3	I/O	Port C (lower four bits), I/O port combined with port B, and control port
10-13	PC4-7	I/O	Port C (high four bits), I/O port and control port combined with port A
27-34	D0-7	I/O	Bidirectional data bus
26	V_{DD}	I	Power supply
7	GND	I	grounds
6	C_{SN}	I	Slice selection signal, low level effective
5	R_{DN}	I	Read signal, low level valid
36	W_{RN}	I	Write signal, low level valid
8，9	A1,A0	I	Address signal
35	R_{ESET}	I	Reset signal, high level valid

Electrical characteristic

Limit limit parameter

(Tamb=25 ° C unless otherwise specified)

Parameter	Symbol	Article and piece	Value	Unit
Power supply voltage	V_{DD}	—	-0.3～+5.5	V
Working environment temperature	T_{amb}	—	-40～+85	°C
Temperature of storage	T_{stg}		-65～+150	°C

Electrical characteristics

DC Characteristics

(Tamb=25 ° C, VDD=5V, unless otherwise specified)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Input high level voltage	V_{IH}	V_{DD}=5V RESET Outside ports	2.0	—	—	V
Input low level voltage	V_{IL}	V_{DD}=5V RESET Outside ports			0.8	V
Input high level voltage	V_{IH}	V_{DD}=5V RESET Port of port	2.0	—	—	V
Input low level voltage	V_{IL}	V_{DD}=5V RESET Port of port	—	—	0.8	V
Output high level voltage 1	V_{OH1}	V_{DD}=5V，I_O=-2.5mA, V_{IN}=0V，4.5V	3.0	—	—	V

Output high level voltage2	V_{OH2}	V_{DD}=5V，IO=-100uA，V_{IN}=0V，4.5V	VDD-0.4	—	—	V
Low output voltage	V_{OL}	V_{DD}=5V，I_O=2.5mA，VIN=0V，4.5V	—	—	0.4	V
Input leakage current	I_{IH}	V_{DD}=5.5V，V_{IN}=5.5V	-1.0	—	—	uA
Input leakage current	I_{IL}	V_{DD}=5.5V，V_{IN}=0V	—	—	1.0	uA
Output leakage current	I_{OZH}	V_{DD}=5.5V，V_{IN}=5.5V	-10	—	—	uA
Output leakage current	I_{OZL}	V_{DD}=5.5V，V_{IN}=0V	—	—	10	uA
Static current	I_{DDSB}	V_{DD} 5V，I_O=0mA，V_{IN}=GND or V_{DD}	—	—	20	uA
Frequency of operation	F_T	V_{DD}=4.5V and 5.5V V_{IN}=GND or V_{DD}，f=1MHz	5	—	—	MHz

AC Characteristics

(Tamb=25 ° C, VDD=5V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial communication frequency	f_{SCL}				1	MHz
Bus idle time	t_{BUF}	—	—	0.5	—	us
Start flag hold time	$t_{HD,STA}$	—	—	0.26	—	us
The establishment time of the restart state	$t_{SU,STA}$	—	—	0.26	—	us
Stop flag establishment time	$t_{SU,STO}$	—	—	0.26	—	us
Data retention time	$t_{HD,DAT}$	—	—	0	—	us
Data creation time	$t_{SU,DAT}$	—	—	50	—	ns
SCL low level time	t_{LOW}	—	—	0.5	—	us
SCL high level time	t_{HIGH}	—	—	0.26	—	us
The rise time of SDA and SCL	t_R	—	—	20+0.1C_b	120	ns
SDA, SCL decline time	t_F			20+0.1C_b	120	ns

Port of control

Control port name	Description of function
C_{SN}	Slice selection signal, low level effective
R_{DN}	Bus read signal, low level valid
W_{RN}	Bus write signal, low level valid
A1，A0	Address signal
R_{ESET}	Reset signal, high level valid

A1	A0	RDN	WRN	CSN	Operation
0	0	1	0	0	Data bus to PA output data buffer
0	1	1	0	0	Data bus to PB output data buffer
1	0	1	0	0	Data bus to PC output data buffer
1	1	1	0	0	Data bus to control word register
0	0	0	1	0	PA data to data bus
0	1	0	1	0	PB data to data bus
1	0	0	1	0	PC data to data bus
1	1	0	1	0	Control word registers to the data bus
X	X	1	1	0	PA, PB, and PC were all high configurations
X	X	X	X	1	PA, PB, and PC were all high configurations

Mode selection

The XCP82C55 has three operating modes: mode0, mode1, mode2. The master control can write data and control words through the 8bit bus interface (port D), and can also read data from PA, PB, and PC ports from port D.

Mode selection control word	B7	B6	B5	B4	B3	B2	B1	B0
	1	PAM1	PAM0	PAIO	PCIOH	PBM	PBIO	PCIOL
P_{AM1}, P_{AM0}	PA[7:0] and PC[7:4] operating mode control bit reset value: 00 =00, PA[7:0] and PC[7:4] work at mode0 =01, PA[7:0] and PC[7:4] work at mode1 =1x, PA[7:0] and PC[7:4] work at mode2							
P_{AIO}	PA input/output control bit reset value: 1 =0, PA is the output state =1, PA is the input state							
P_{CIOH}	PC[7:4] input/output control bit reset value: 1 =0, PC[7:4] is the output state =1, PC[7:4] is the input state							
P_{BM}	PB[7:0] and PC[3:0] operating mode control bits Reset value: 0 =0, PB[7:0] and PC[3:0] work at mode0 =1, PB[7:0] and PC[3:0] work at mode1							
P_{BIO}	Reset value of PB input/output control bit: 1 =0, PA is the output state =1, PA is the input state							
P_{CIOL}	PC[3:0] input/output control bit reset value: 1 =0, PC[7:4] is the output state =1, PC[7:4] is the input state							

When the input level of RESET port is high and the hardware reset operation of XCP82C55 is performed, all ports (PA, PB, PC) are reset to the input state.

3 working modes can be selected through D[7:0] bus setting mode selection control word:

1. mode0, basic input/output mode
2. mode1, input/output mode with latch
3. mode2, two-way transmission bus

The working mode of PA and PB can be controlled separately. The PC is divided into two parts: high position and low position. The working mode of PC high position (PCH) shares control bits with PA, and the working mode of PC low position (PCL) shares control bits with PB.

All output data registers, including mode1 and mode2 status flags, are reset after the mode switch. The working modes can be combined, such as PA set to mode1 and PB set to mode0. The working modes can be combined, such as PA set to mode1 and PB set to mode0

The PC port of XCP82C55 can be used for single bit set/reset operation. Single bit set/reset function is performed by software:

PC bit operation control word	B7	B6	B5	B4	B3	B2	B1	B0
	0	NC	NC	NC	B2	B1	B0	RN/S
NC	Can be any value, no effect							
B2，B1，B0	Select the port in the PC to perform bit operations =000,Perform bit operations on PC0 =001,Perform bit operations on PC1 =010,Perform bit operations on PC2 =011,Perform bit operations on PC3 =100,Perform bit operations on PC4 =101,Perform bit operations on PC5 =110,Perform bit operations on PC6 =111,Perform bit operations on PC7							
RN/S	Select the bit operation type =0, perform reset operation =1, perform set operation							

Interrupt control function

When XCP82C55 is operating on mode1 or mode2, the handshake signal provided by the circuit can be used as an external interrupt signal for the MCU. These interrupt flags can also be turned on or blocked by using the PC's bit operation mode. This allows the programmer to enable or disable CPU interrupts with a specific IO without affecting other devices in the interrupt structure.

Interrupt flag signal control: set specific PC ports to enable interrupt flag signal; Reset the specific PC port to turn off the interrupt flag signal.

mode0

Each of the three ports under mode0 has simple input and output functions. Just write data or read data from a specific port.

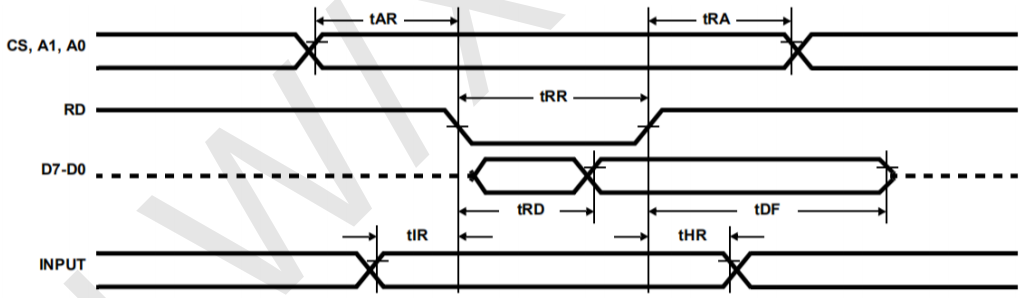
Basic functions of Mode 0:

Two sets of 8-bit ports (PA, PB) and two sets of 4-bit ports (PCH=PC[7:4], PCL=PC[3:0])

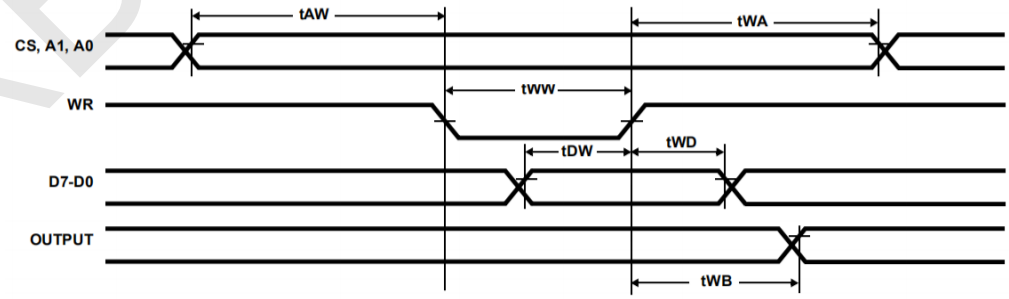
- When PA, PB, and PC are used as input ports, there is no latching function on the ports
- When PA, PB and PC are used as output ports, there is output data latch function on the ports
- PA, PB, PCH, and PCL can be independently set for input or output, with 16 different input/output configurations:

Mode selection control word				Port status			
D4	D3	D1	D0	PA	PCH PC[7:4]	PB	PCL PC[3:0]
0	0	0	0	output	output	output	output
0	0	0	1	output	output	output	input
0	0	1	0	output	output	input	output
0	0	1	1	output	output	input	input
0	1	0	0	output	input	output	output
0	1	0	1	output	input	output	input
0	1	1	0	output	input	input	output
0	1	1	1	output	input	input	input
1	0	0	0	input	output	output	output
1	0	0	1	input	output	output	input
1	0	1	0	input	output	input	output
1	0	1	1	input	output	input	input
1	1	0	0	input	input	output	output
1	1	0	1	input	input	output	input
1	1	1	0	input	input	input	output
1	1	1	1	input	input	input	input

The following figure shows the basic read and write timings in mode 0.



Mode 0 reads the timing



Mode 0 reads the timing

mode1

mode1 provides an IO port with input data latching and handshake signals.

In mode1, PA and PB act as two independent sets of IO, with PCH acting as the handshake signal when PA is working and PCL acting as the handshake signal when PB is working.

mode1 Features:

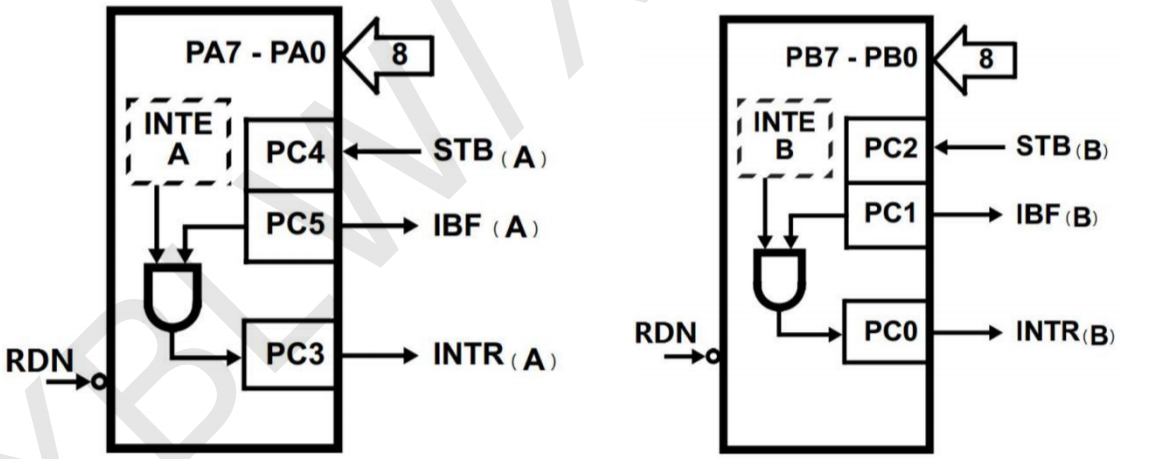
- Two sets of IO ports with handshake signals
- Each group contains 8-bit IO (PA or PB) and 4-bit handshake signal (PCH or PCL)
- 8-bit IO can be configured as input or output. Both input and output are data latching.
- 4-bit handshake signals are used to coordinate the control and status of 8-bit IO and parallel interfaces.

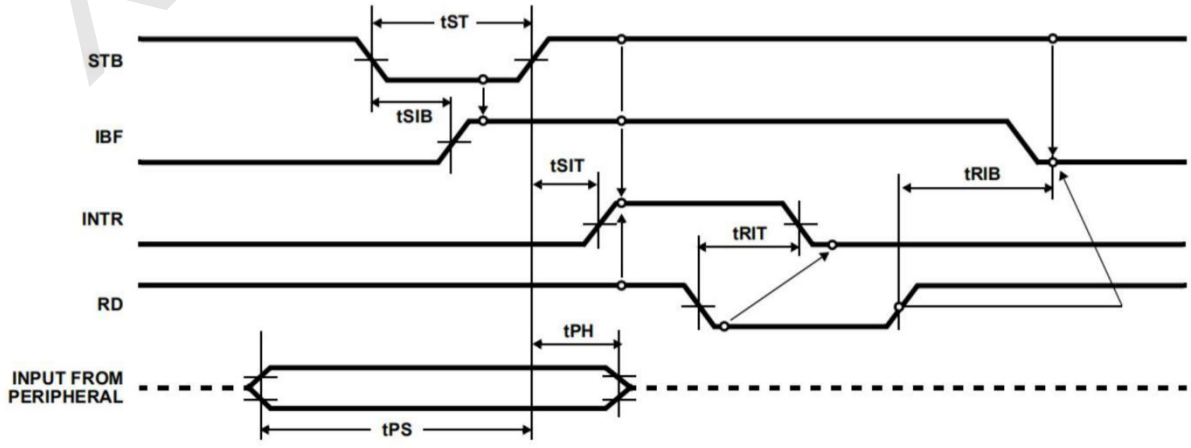
When PA/PB works at mode1 and is set to the input state, the control signal is defined as follows.

Name of signal	Corresponding port	IO	Function
S_{TB}	PC4 (PA) PC2(PB)	Input	Input data latch control signal When STB is L, the data of PA/PB is latched to the internal "input data buffer".
I_{BF}	PC5 (PA） PC1(PB)	Output	Input the data buffer flag bit IBF=H, PA/PB input data buffer has new data that can be read IBF=L, PA/PB input data buffer has not been updated The IBF was positioned at the descending edge of the STB signal and reset at the rising edge of the RDN signal.
I_{NTR}	PC3 (PA) PC0(PB)	Output	The data transmission handshake signal can be used for the interrupt signal of the master control device INTR is positioned at the rising edge of the STB and reset at the falling edge of the RDN signal

The INTR function of PC3 is switched on and off via the bit operation control word of PC4.

The INTR function of PC0 is switched on and off by the bit operation control word of PC2.

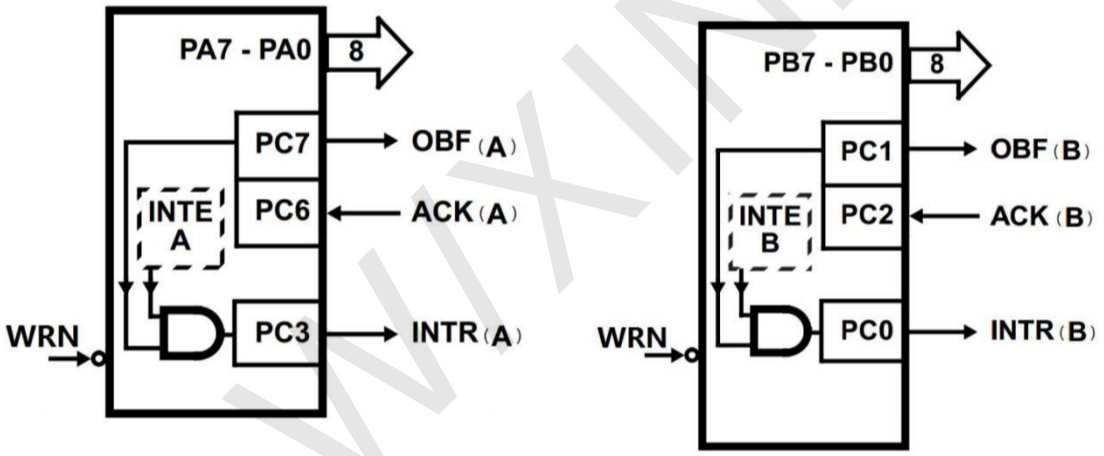


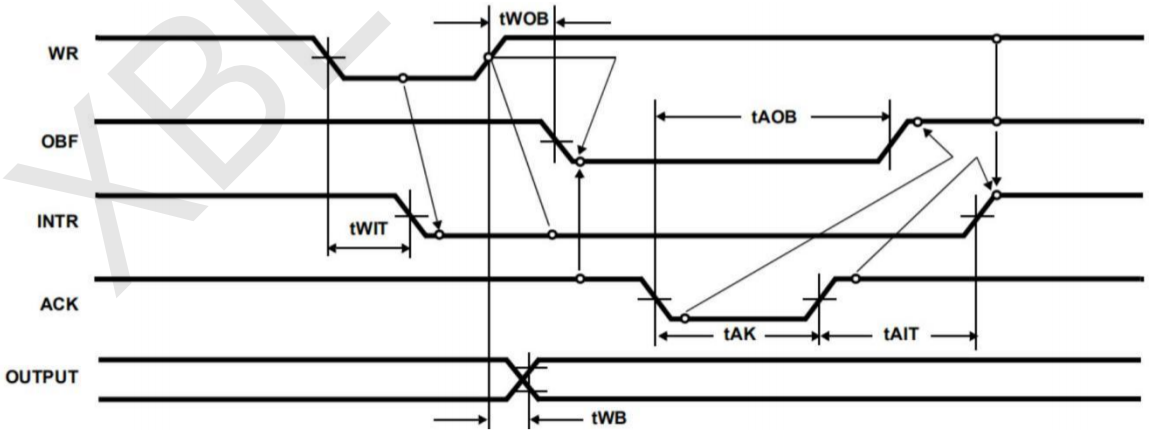


When PA/PB is working at mode1 and set to output state, the control signal is defined as follows.

Name of signal	Corresponding port	IO	Function
O_{BF}	PC7 (PA) PC1(PB)	Output	Output data buffer flag bit OBF=H, the output data buffer is not updated OBF=L, there is new data to output in the output data buffer OBF is reset on the rising edge of the WRN signal and positioned on the falling edge of the ACK signal.
A_{CK}	PC6 (PA) PC2(PB)	Input	The data transfer handshake signal is used to set OBF and INTR ACK= descending edge, set OBF ACK= rising edge, set INTR
I_{NTR}	PC3 (PA) PC0(PB)	Output	The data transmission handshake signal can be used for the interrupt signal of the master control device INTR is set at the rising edge of the ACK signal and reset at the falling edge of the WRN signal.

The INTR function of PC3 is switched on and off via the bit operation control word of PC6.
The INTR function of PC0 is switched on and off by the bit operation control word of PC2.





The following table shows the eight different combinations of output input states and PA, PB, and PC port functions under mode1.

Word of control			PAPB PC port function under MODE 1									
D4	D3	D1	Port A	Port B	PC0	PC1	PC2	PC3	PC4	PC5	PC6	PC7
0	1	0	output	output	INTR B	OBF B	ACK B	INTR A	Input* Output*		ACK A	OBF A
0	1	1	output	input	INTR B	IBF B	STB B	INTR A	Input* Output*		ACK A	OBF A
1	1	0	input	output	INTR B	OBF B	ACK B	INTR A	STB A	IBF A	Input* Output*	
1	1	1	input	input	INTR B	IBF B	STB B	INTR A	STB A	IBF A	Input* Output*	

* When PA is set to mode1 output mode, PC4 and PC5 can work in mode0 input mode, and the port status of PC4 and PC5 can be read normally through the parallel interface.

* When PA is set to mode1 output mode, PC4 and PC5 can work in mode0 output mode, but can only change the port state of PC4 and PC5 through single bit operation mode.

* When PA is set to mode1 input mode, PC6 and PC7 can work in mode0 input mode, and the port status of PC6 and PC7 can be read normally through the parallel interface.

* When PA is set to mode1 input mode, PC6 and PC7 can work in mode0 output mode, but can only change the port state of PC6 and PC7 through single bit operation mode.

4.3.3、mode2

Mode2 provides a set of 8-bit buses with handshake signals that transmit data in both directions. The handshake signal, similar to mode1, also provides a handshake signal that can act as an interrupt flag signal, which can also be turned on or off by software selection.

mode2 Features:

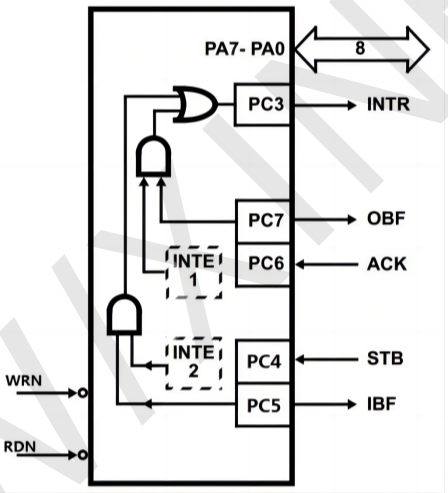
- Only the PA provides mode2 functionality while the PC serves as the handshake signal
- Provides a set of 8-bit bidirectional bus ports (PA) and a set of 5-bit control ports (PC)
- PA has latches for both input and output data
- A 5-bit control port (PC) is used to control the PA's data input/output and provide process-related flag signals

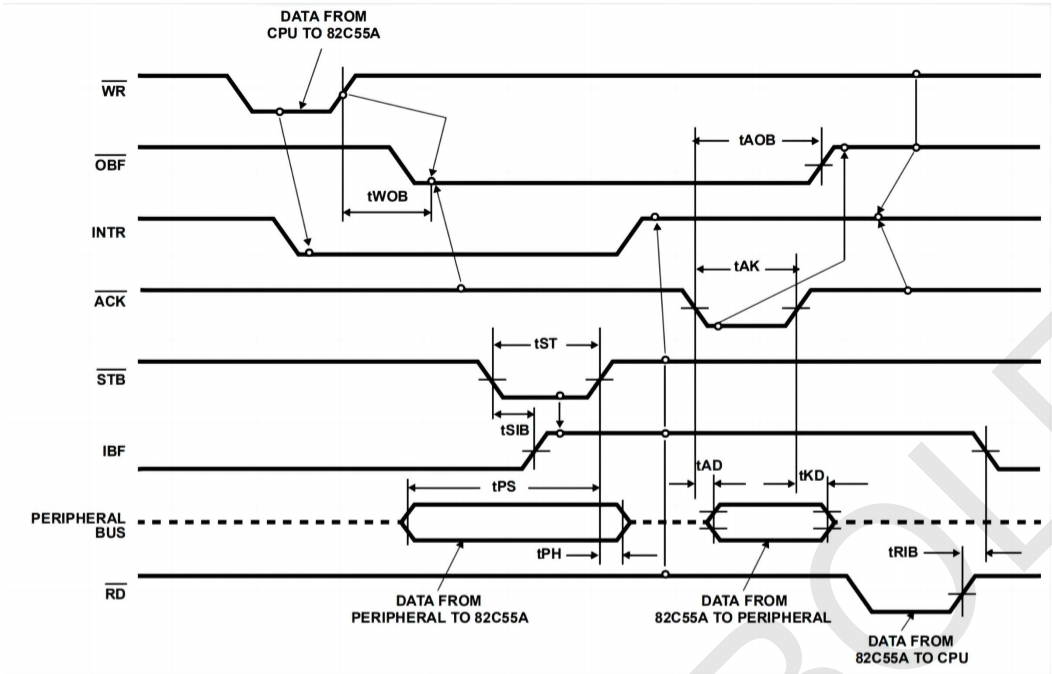
Control signal definition in mode2

Name of signal	Corresponding port	IO	Function
O_{BF}	PC7	The output	Output data buffer flag bit OBF=H, the output data buffer is not updated OBF=L, there is new data to output in the output data buffer OBF is reset on the rising edge of the WRN signal and positioned on the falling edge of the ACK signal.
A_{CK}	PC6	Input in	The data transfer handshake signal is used to set OBF and INTR ACK= falling edge, set OBF ACK= rising edge, set INTR
S_{TB}	PC4	Input in	Input data latch control signal When STB is L, the data of PA/PB is latched to the internal "input data buffer".

I_{BF}	PC5	The output	Input the data buffer flag bit IBF=H, PA/PB input data buffer has new data that can be read IBF=L, PA/PB input data buffer has not been updated The IBF is positioned at the descending edge of the STB signal and at the RDN signal
I_{NTR}	PC3	The output	The data transmission handshake signal can be used for the interrupt signal of the master control device The INTR of the input function is set at the rising edge of the STB, the INTR of the output function is reset at the falling edge of the RDN, and the INTR of the output function is set at the rising edge of the ACK and restored at the falling edge of the WRN.

The INTR function of the PC3 in the input function is switched on and off by the bit operation control word of the PC4.
The INTR function of the PC3 in the output function is switched on and off by the bit operation control word of the PC6.

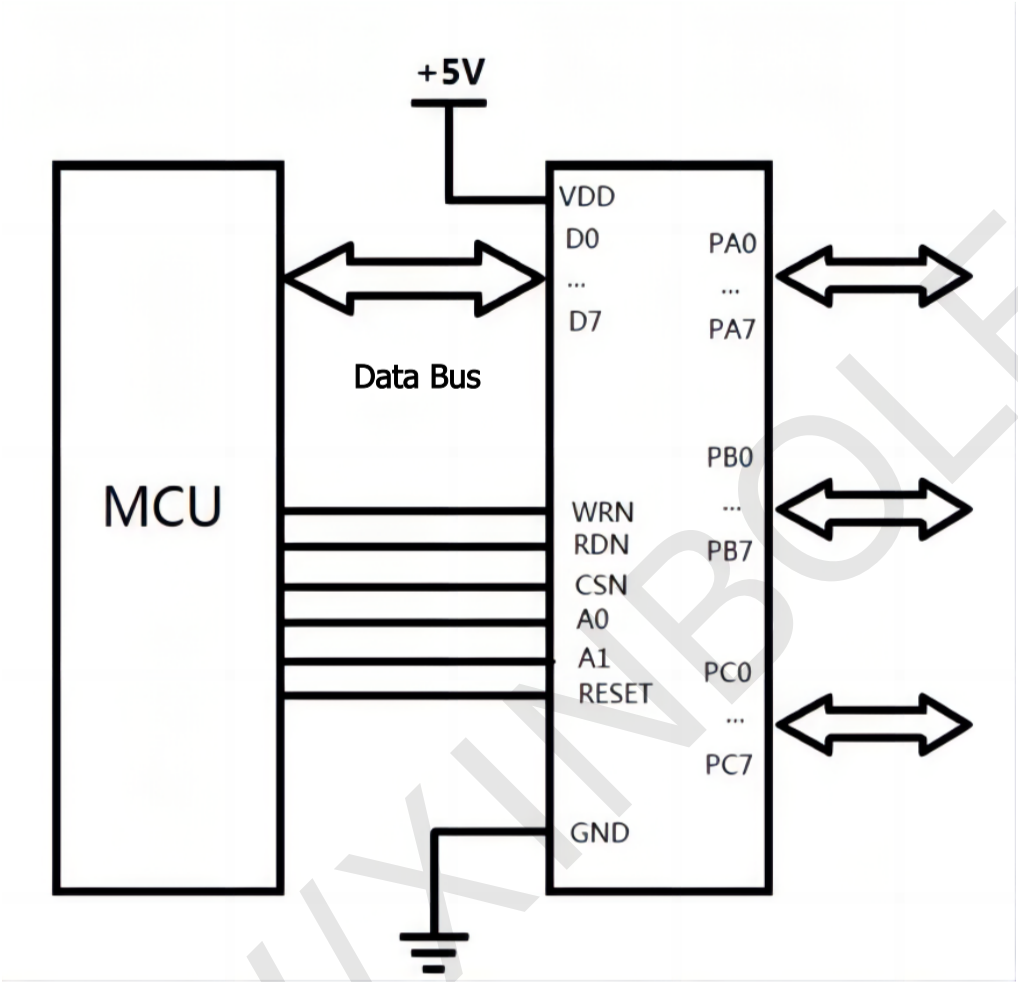




The following table shows the combination of output input states in different cases of mode2.

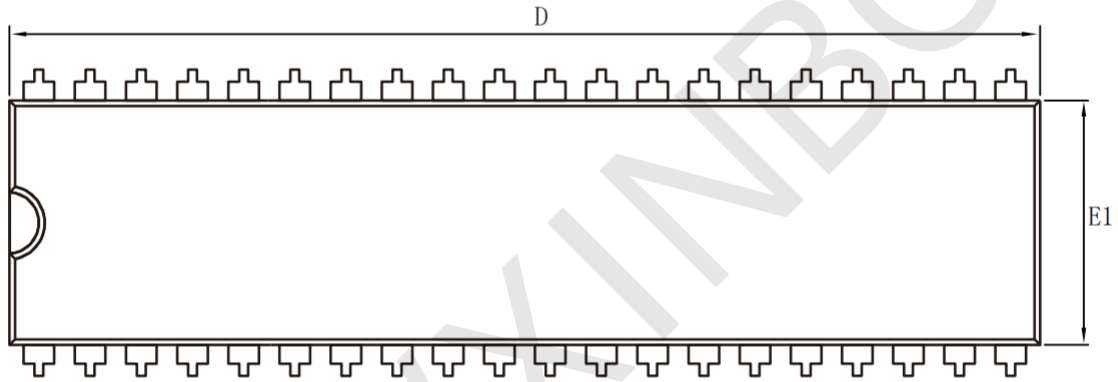
Word of control			PAPB PC port functions									
D2	**D1**	**D0**	**Port A**	**Port B**	**PC0**	**PC1**	**PC2**	**PC3**	**PC4**	**PC5**	**PC6**	**PC7**
0	0	0	Mode2 I/O	MODE 0 output	output			INTR A	STB A	IBF A	ACK A	OBF A
0	0	1	Mode2 I/O	MODE 0 output	input			INTR A	STB A	IBF A	ACK A	OBF A
0	1	0	Mode2 I/O	MODE 0 input	output			INTR A	STB A	IBF A	ACK A	OBF A
0	1	1	Mode2 I/O	MODE 0 input	input			INTR A	STB A	IBF A	ACK A	OBF A
1	0	X	Mode2 I/O	MODE 1 output	INTR B	OBF B	ACK B	INTR A	STB A	IBF A	ACK A	OBF A
1	1	X	Mode2 I/O	MODE 1 input	INTR B	IBF B	STB B	INTR A	STB A	IBF A	ACK A	OBF A

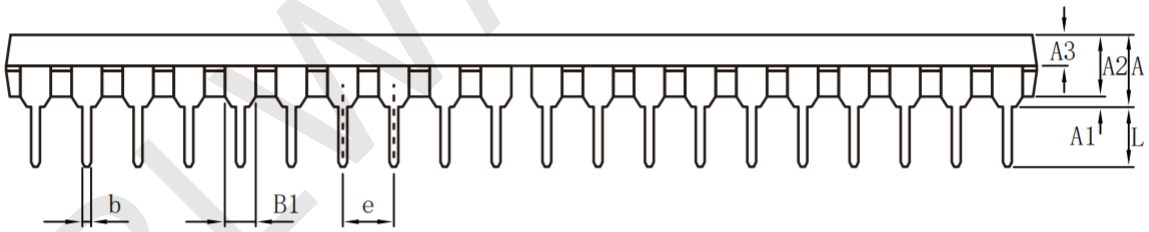
Typical application line

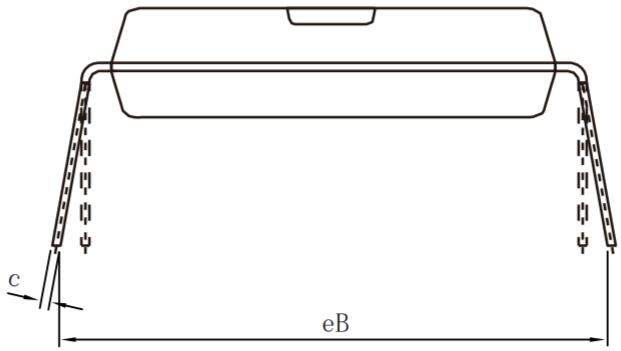


· DIP-40

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	4.160	4.560	A	0.164	0.180
A1	0.510		A1	0.020	
A2	3.400	3.950	A2	0.134	0.156
A3	1.740	1.840	A3	0.069	0.072
b	0.440	0.530	b	0.072	0.021
B1	1.27(REF)		B1	0.05(REFz)	
c	0.250	0.300	c	0.010	0.012
D	52.15	52.42	D	2.050	2.060
E1	13.70	13.90	E1	0.539	0.547
e	2.54		e	0.100	
eB	15.24	17.21	eB	0.600	0.678
L	3.000		L	0.118	







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