MP4246

6A Buck-Boost Converter with Four Integrated MOSFETs and I²C Interface

DESCRIPTION

The MP4246 is a synchronous buck-boost converter with four integrated MOSFETs (SWA, SWB, SWC, and SWD). The device can deliver up to 6A of output current (I_{OUT}) at certain input supply ranges with excellent efficiency.

The MP4246 is suitable for USB power delivery (PD) and wireless charging applications. The device can work with an external USB PD controller or wireless charging controller via the I²C interface. The I²C interface and one-time programmable (OTP) memory provide flexibility for configurable features.

Fault condition protections include constant current (CC) limiting, output over-voltage protection (OVP), input OVP, and thermal shutdown (TSD).

The MP4246 requires a minimal number of readily available, standard external components. The MP4246 is available in a small QFN-19 (4mmx5mm) package with wettable flanks.

FEATURES

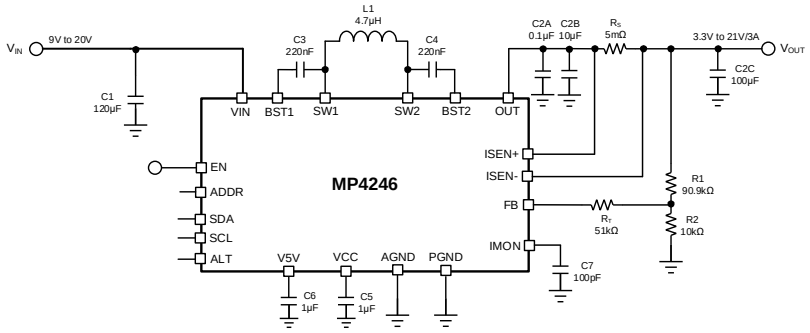
- 6A Buck-Boost Converter with Four Integrated MOSFETs
- 4V to 22V Operating Input Voltage (V_{IN}) Range, with a Withstand V_{IN} Up to 36V
- 24V Input Over-Voltage (OV) Shutdown Protection
- 1V to 22V Output Voltage (V_{OUT}) Range
- I²C-Configurable, 0.1V to 2.147V Reference Voltage (V_{REF}) Range with 1mV Resolution
- Up to 98.82% Peak Efficiency
- Integrated 5V/60mA Low-Dropout (LDO) Regulator to Supply the External Microcontroller Unit (MCU)
- Constant Current (CC) Limit with 5% Accuracy
- Selectable Input or Output CC Limit with 5% Accuracy via Factory Trimming
- Accurate Output Current (I_{OUT}) Monitoring
- Selectable 280kHz, 420kHz, 600kHz, or 1MHz Switching Frequency (f_{SW}) with Frequency Spread Spectrum (FSS)
- Selectable Forced Pulse-Width Modulation (PWM) Mode and Automatic Pulse-Frequency Modulation (PFM) or PWM Mode
- Configurable I²C Slave Address
- Line Drop Compensation
- I²C, Alert, and One-Time Programmable (OTP) Memory
- Enable (EN) Shutdown Passive Discharge
- Available in a QFN-19 (4mmx5mm) Package with Wettable Flanks

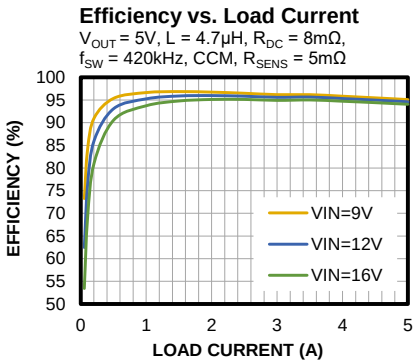
MPL Optimized Performance with MPS Inductor MPL-AY1050 Series

APPLICATIONS

- USB Type-C and USB Power Delivery (PD)
- USB Type-C and USB Type-A Communication Interfaces
- Wireless Charging
- USB Type-C Car Chargers
- Generic Buck-Boost Converters

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP4246GVE-0000	QFN-19 (4mmx5mm)***	*See Below*	1
MP4246GVE-xxxx**			

* For Tape & Reel, add suffix -Z (e.g. MP4246GVE-xxxx-Z).

** "xxxx" is the configuration code identifier for the register setting stored in the one-time programmable (OTP) memory, and it cannot be configured by the user again. Each "x" can be a hexadecimal value between 0 and F. The default code is "0000." Work with an MPS FAE to create this unique number.

*** Wettable flanks

TOP MARKING

MPSYWW
MP4246
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP4246: Part number
LLLLLL: Lot number
E: Wettable flank

EVALUATION KIT EVKT-MP4246

EVKT-MP4246 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EVL4246-V-00A	MP4246 evaluation board	1
2	EVKT-USBI2C-02	Includes one USB-to-I²C communication interface, one USB cable, and one ribbon cable	1
3	MP4246GVE-0000	MP4246 IC (cannot be configured by the user again)	1
4	Online resources	Include the datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

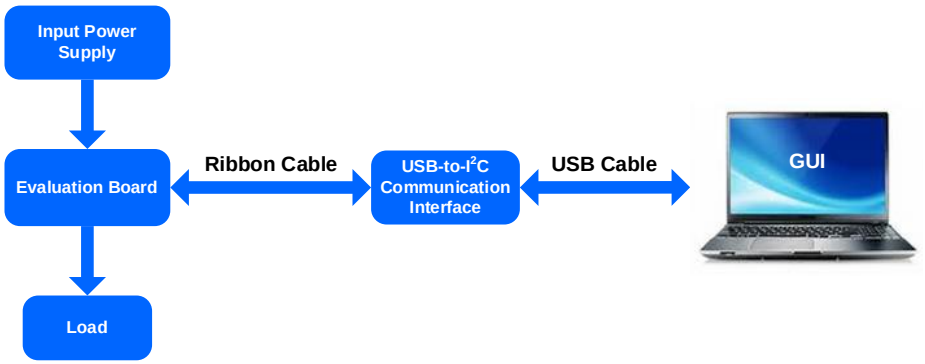
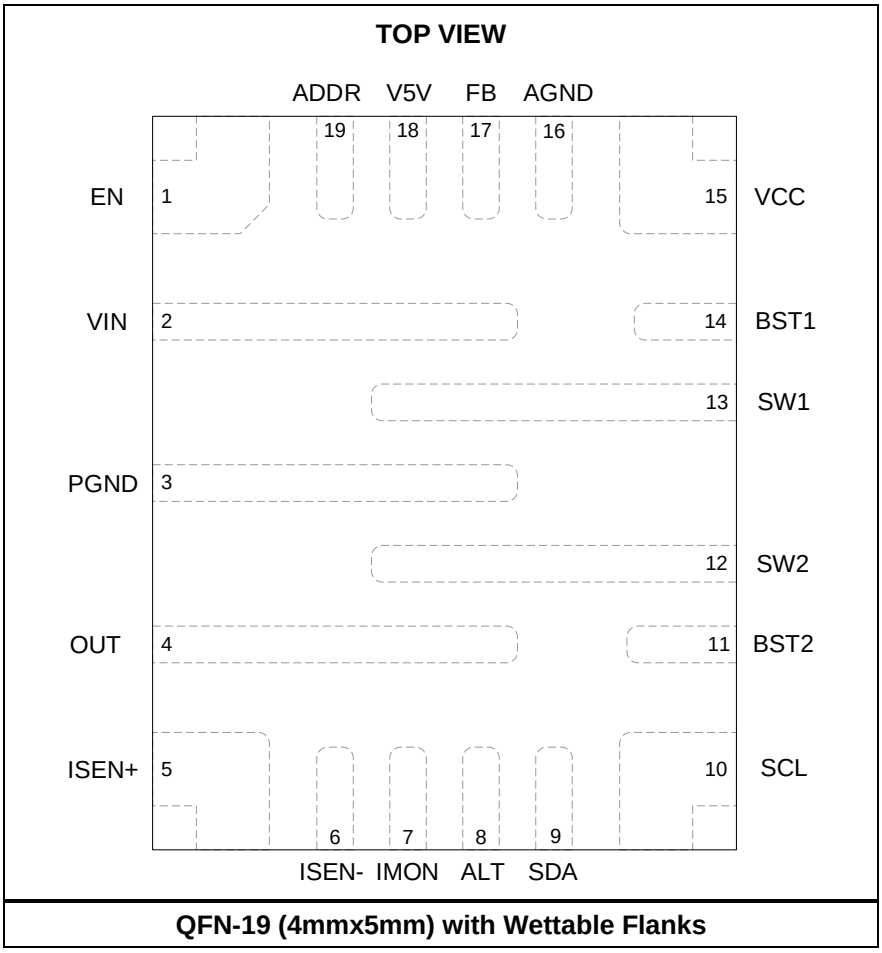


Figure 1: EVKT-MP4246 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-19 (4mmx5mm) with Wettable Flanks

PIN FUNCTIONS

Pin #	Name	Description
1	EN	**Enable input.** Pull the EN pin logic high to enable the chip.
2	VIN	**Power supply voltage.** The MP4246 operates across a 4V to 22V input voltage (V_{IN}), with a withstand V_{IN} up to 36V. The VIN pin is the drain of the first half-bridge's internal power device. An input capacitor (C_{IN}) is required to prevent large voltage spikes at the input. Place C_{IN} as close to the IC as possible.
3	PGND	**Power ground.** The PGND pin requires additional care during the PCB layout. Connect the PGND pin to ground using copper traces and vias.
4	OUT	**Buck-boost output.** The OUT pin is the drain of switch D (SWD). The output capacitor (C_{OUT}) prevents large voltage spikes at the output. Place C_{OUT} as close to the IC as possible.
5	ISEN+	**Positive node of the current-sense input.** The ISEN+ pin can be used for the output current (I_{OUT}) limit.
6	ISEN-	**Negative node of the current-sense input.** The ISEN- pin can be used for the I_{OUT} limit.
7	IMON	**Output current monitor.** The IMON pin outputs a voltage signal that is proportional to I_{OUT}.
8	ALT	**I²C alert.** The ALT pin is an open-drain output. Pull ALT low to indicate the unmasked STATUS register bits.
9	SDA	**I²C data line.**
10	SCL	**I²C clock signal input.**
11	BST2	**Bootstrap 2.** A 0.22µF capacitor is connected between the BST2 and SW2 pins to form a floating supply across the high-side MOSFET (HS-FET) driver.
12	SW2	**Switch node 2 of the buck-boost converter.** Connect the SW2 pin to SW1 using a power inductor. Use a wide PCB trace to make the connection.
13	SW1	**Switch node 1 of the buck-boost converter.** Connect the SW1 pin to SW2 using a power inductor. Use a wide PCB trace to make the connection.
14	BST1	**Bootstrap 1.** A 0.22µF capacitor is connected between the BST1 and SW1 pins to form a floating supply across the HS-FET driver.
15	VCC	**Internal 3.54V low-dropout (LDO) regulator output.** Decouple the VCC pin using a 1µF capacitor.
16	AGND	**Analog ground.** Connect the AGND pin to PGND. In addition, connect AGND to the VCC capacitor's ground node.
17	FB	**Feedback.** Connect the FB pin to an external resistor divider's tap between the output and AGND to set the output voltage (V_{OUT}).
18	V5V	**5V LDO output.** Bypass the V5V pin using a 1µF capacitor. V5V can supply a 60mA I_{OUT}. The 5V LDO turns on once V_{IN} and the EN pin voltage (V_{EN}) exceed their under-voltage lockout (UVLO) thresholds (V_{IN_UVLO} and $V_{EN\_RISING1}$, respectively); the 5V LDO turns off once the VCC voltage (V_{CC}) drops below its UVLO threshold (V_{CC_UVLO}), meaning EN is pulled low, V_{IN} is below 2.4V (typically), or the device reaches the V_{IN} over-voltage protection (OVP) threshold. The status of OPERATION (01h, bit[7]) has no effect on V5V.
19	ADDR	**Multi-function.** The ADDR pin can set the I²C slave address and default state of the OPERATION bit. The status of ADDR is latched after V_{IN} and V_{EN} exceed V_{IN_UVLO} and $V_{EN\_RISING1}$, respectively. ADDR resets only when V_{CC} is below V_{CC_UVLO}.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +40V (2)
Output voltage (V_{OUT}), V_{ISEN+}, and V_{ISEN-} .....
.....0.3V to 24V (28V for <10ns)
V_{SW1} or V_{SW2}.....
-0.3V (-5V for <10ns) to +24V (+30V for <10ns)
V_{BST1} or V_{BST2} ..... V_{SW1} or V_{SW2} + 4V
V_{EN}.....-0.3V to +40V
V_{5V}.....-0.3V to +5.5V
V_{SCL}, V_{SDA}, V_{ALT} .....-0.3V to +6.5V
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (3)
QFN-19 (4mmx5mm)..... 5.3W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings (4)

Human body model (HBM) (5)..... ±2kV
Charged-device model (CDM) ..... ±750V

Recommended Operating Conditions (6)

Operating input voltage (V_{IN}) range .....
.....4V to 22V DC, 36V transient
Operating V_{OUT} range.....1V to 22V
Output current (I_{OUT})..... 6A
V5V LDO output.....5V/60mA
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

EVL4246-V-00A (7).....23.6 ....3.9 .. °C/W
QFN-19(4mmx5mm) (8).....41.2 ....3.9 .. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For slew rates below 20V/ms, the input ramps up from 0V to 40V.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
5) HBM with regard to ground.
6) The device is not guaranteed to function outside of its operating conditions.
7) Measured on the EVL4246-V-00A.
8) Measured on JESD51-7, a 4-layer PCB. The θ_{JA} value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{Q_SD}	V_{EN} = 0V			10	μA
Quiescent supply current	I_{Q1}	No switching, I²C-set OPERATION bit on, EN on, automatic pulse-frequency modulation (PFM) or pulse-width modulation (PWM) mode		900		μA
	I_{Q2}	I²C-set OPERATION bit = off, EN on		130		μA
EN rising threshold 1	$V_{EN\_RISING1}$	EN to enable VCC and V5V		0.68		V
EN hysteresis 1	V_{EN_HYS1}			65		mV
EN rising threshold 2	$V_{EN\_RISING2}$	EN to enable switching		1.32		V
EN hysteresis 2	V_{EN_HYS2}			350		mV
EN pull-down resistor	R_{EN}	EN = 2V		1.25		MΩ
Thermal shutdown (9)	T_{STD}			165		°C
Thermal warning (9)	T_{OTW}			135		°C
Thermal hysteresis (9)	T_{STD_HYS}			20		°C
V5V low-dropout (LDO) regulator	V_{5V}		-2%	5	+2%	V
V5V load regulation	V_{5V_LOG}	I_{CC} = 0mA to 60mA		2	5	%
VCC LDO regulator	V_{VCC}		-2.5%	3.54	+2.5%	V
VCC load regulation	V_{VCC_LOG}	I_{CC} = 20mA		2	5	%
V_{CC} under-voltage lockout (UVLO) rising threshold	$V_{CC\_UVLO\_R}$		2.4	2.55	2.7	V
V_{CC} UVLO hysteresis	$V_{CC\_UVLO\_HYS}$			260		mV
V_{IN} UVLO rising threshold	$V_{IN\_UVLO\_R}$		3.58	3.73	3.88	V
V_{IN} UVLO hysteresis				300		mV
V_{IN} UVLO rising threshold (trimming option, 4.24V version)	$V_{IN\_UVLO\_R\_TRIM}$		4.04	4.24	4.44	V
V_{IN} UVLO hysteresis (trimming option, 4.24V version)				400		mV
Buck-Boost Converter						
Switch A (SWA) on resistance	$R_{DS(ON)\_A}$			10		mΩ
Switch B (SWB) on resistance	$R_{DS(ON)\_B}$			14		mΩ
Switch C (SWC) on resistance	$R_{DS(ON)\_C}$			6		mΩ
Switch D (SWD) on resistance	$R_{DS(ON)\_D}$			6		mΩ
Feedback voltage	V_{FB1}		-2.5%	0.33	+2.5%	V
	V_{FB2}		-2%	0.5	+2%	V
	V_{FB3}		-1.5%	2	+1.5%	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output over-voltage protection (OVP) rising threshold	$V_{FB\_OVP\_R}$		113	118	123	% of V_{FB}
Output OVP falling threshold	$V_{FB\_OVP\_F}$		102	107	112	% of V_{FB}
Input OVP rising threshold	$V_{IN\_OVP\_R}$		23	24	25	V
Input OVP falling threshold	$V_{IN\_OVP\_F}$		22	23	24	V
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW1} = V_{SW2} = 22V, T_J = 25°C			1	µA
		V_{EN} = 0V, V_{SW1} = V_{SW2} = 22V, T_J = -40°C to +150°C			30	µA
Hiccup off-timer	t_{HICCUP}		470	570	670	ms
Switching frequency 1	f_{SW1}		-20%	280	+20%	kHz
Switching frequency 2	f_{SW2}		340	420	500	kHz
Switching frequency 3	f_{SW3}		-20%	600	+20%	kHz
Switching frequency 4	f_{SW4}		-20%	1000	+20%	kHz
Frequency dithering span	f_{SW_RANGE}	2kHz triangle modulation, f_{SW} = 420kHz, buck or boost		±9		%
Soft-start time	t_{SS}	Output from 10% to 90%, V_{OUT} = 5V, constant slew rate for other reference voltage (V_{REF})		1		ms
Minimum on time (9)	$t_{ON\_MIN\_BT}$			180		ns
Minimum off time (9)	t_{OFF_MIN}			180		ns
ISEN+- threshold	I_{OC1}	OC threshold = 1A, R_{SENS} = 5mΩ	4.25	5	5.75	mV
	I_{OC2}	OC threshold = 3.6A, R_{SENS} = 5mΩ	-5%	18	+5%	mV
IMON gain	G_{IMON3A}	T_J = 25°C, I_{OUT} = 3A, R_{SENS} = 5mΩ	-5%	248	+5%	mV/A
Low-side (LS) SWB valley current limit	I_{LIMIT2}	D3h, bits[7:6] = 01b	6.5	9	12.1	A
LS SWC peak current limit	I_{LIMIT3}	D3h, bits[7:6] = 01b	9	13.2	17.4	A
Line drop compensation	V_{DROP}	I_{OUT} = 1A	-20%	100	+20%	mV
Output discharge resistor	R_{DISCHG}	T_J = 25°C	50	90	160	Ω
Mode Transition Threshold						
Buck-boost to buck transition threshold	V_{MODE_TH2}	V_{IN} / V_{OUT}		120		%
Buck-boost to boost transition hysteresis	V_{MODE_HYS2}	V_{IN} / V_{OUT}		82		%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
ALT pin leakage	I_{ALT_LKG}	V_{ALT} = 5V			1	μA
ALT pin pull low resistance	R_{ALT}				50	Ω
I²C Interface Specification (9)						
ADDR configuration voltage level 1	V_{ADDR1}	Set I²C address 67h, EN off			0.2	V_{CC}
ADDR configuration voltage level 2	V_{ADDR2}	Set I²C address 47h, EN off	0.29		0.45	V_{CC}
ADDR configuration voltage level 3	V_{ADDR3}	Set I²C address 27h, EN on	0.57		0.67	V_{CC}
ADDR configuration voltage level 4	V_{ADDR4}	Set I²C address 07h, EN on	0.76			V_{CC}
Input logic high voltage	V_{IH}		1.25			V
Input logic low voltage	V_{IL}				0.9	V
Output voltage logic low	V_{OUT_L}				0.4	V
SCL clock frequency	f_{SCL}			400	1000	kHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}		0	60		ns
Set-up time for a repeated start command	t_{SU_STA}		160			ns
Hold time for a repeated start command	t_{HD_STA}		160			ns
Bus free time between a start and stop command	t_{BUF}		160			ns
Set-up time for a stop command	t_{SU_STO}		160			ns
SCL and SDA rising time	t_R		10		300	ns
SCL and SDA falling time	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance for each bus line	C_B				400	pF
Power Good (PG) Indication						
PG lower rising threshold	$V_{PG\_R\_L}$	PG goes high	86.5	91	96.5	% of V_{FB}
PG lower falling threshold	$V_{PG\_F\_L}$	PG goes low	75	80.5	86	% of V_{FB}
PG upper rising threshold	$V_{PG\_R\_H}$	PG goes low	113	118	123	% of V_{FB}
PG upper falling threshold	$V_{PG\_F\_H}$	PG goes high	102	107	112	% of V_{FB}

Note:

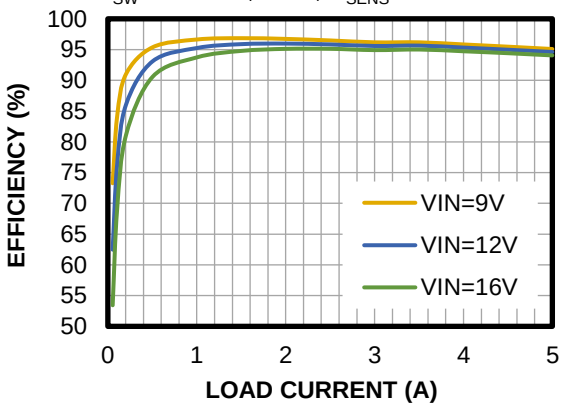
9) Guaranteed by characterization sample test.

TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

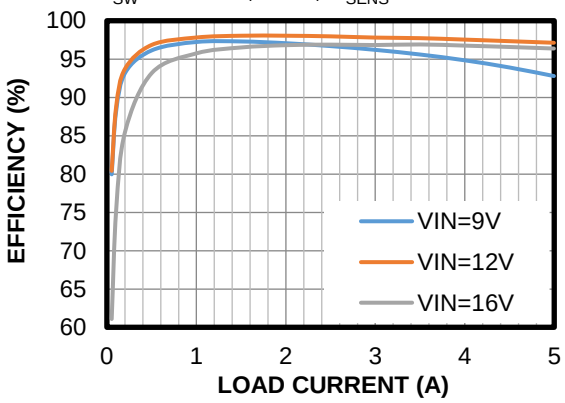
Efficiency vs. Load Current

V_{OUT} = 5V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENS} = 5mΩ



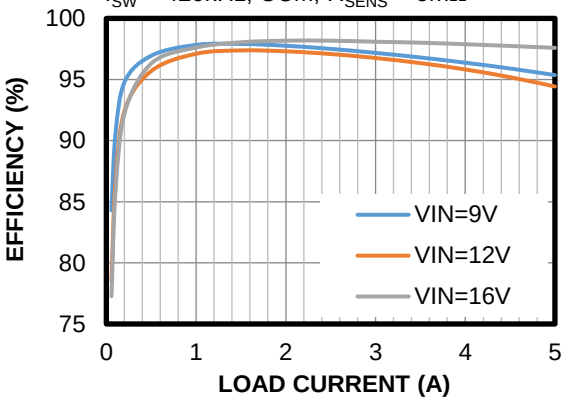
Efficiency vs. Load Current

V_{OUT} = 9V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENS} = 5mΩ



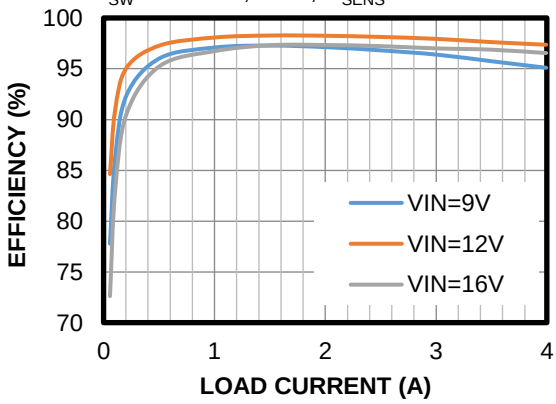
Efficiency vs. Load Current

V_{OUT} = 12V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENS} = 5mΩ



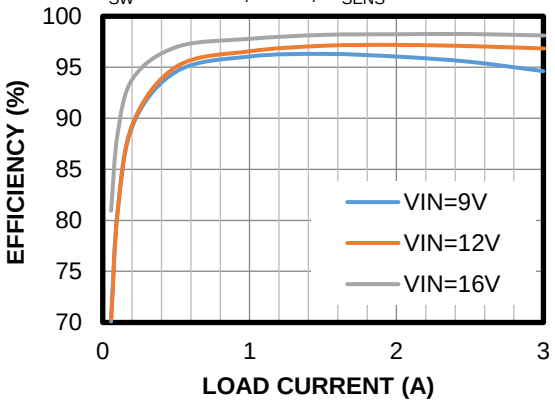
Efficiency vs. Load Current

V_{OUT} = 15V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENS} = 5mΩ



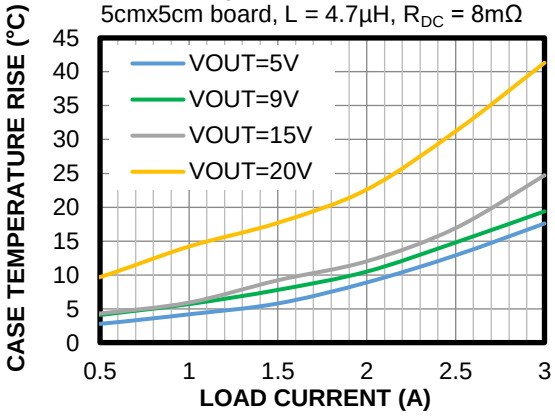
Efficiency vs. Load Current

V_{OUT} = 20V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENS} = 5mΩ



Case Temperature Rise vs. Load Current

V_{IN} = 12V, f_{SW} = 420kHz, based on 5cmx5cm board, L = 4.7µH, R_{DC} = 8mΩ

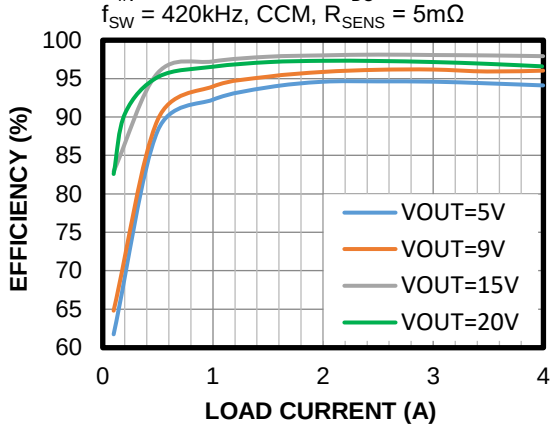


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

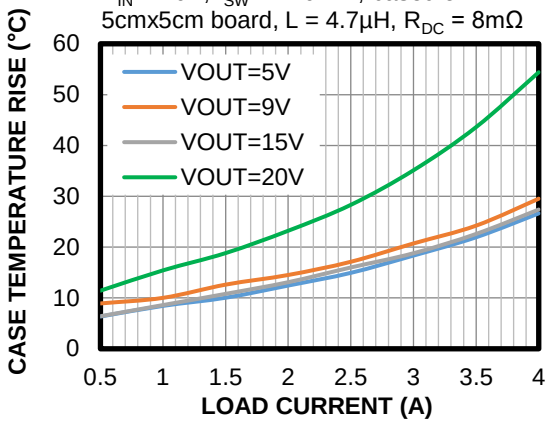
Efficiency vs. Load Current

V_{IN} = 20V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENS} = 5mΩ



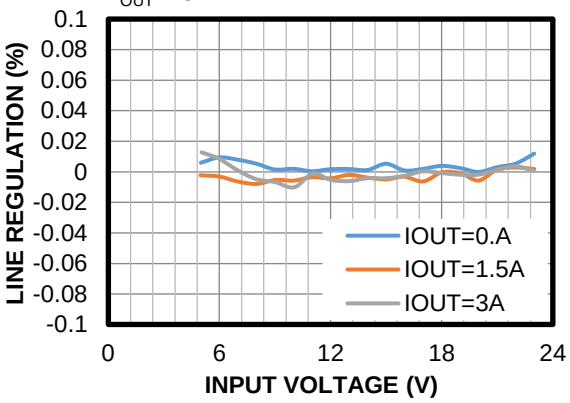
Case Temperature Rise vs. Load Current

V_{IN} = 20V, f_{SW} = 420kHz, based on 5cmx5cm board, L = 4.7µH, R_{DC} = 8mΩ



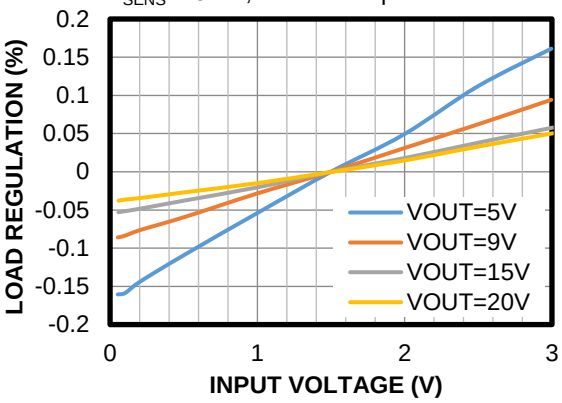
Line Regulation

V_{OUT} = 5V

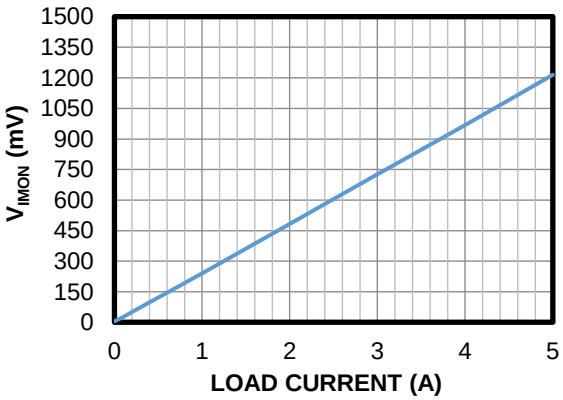


Load Regulation

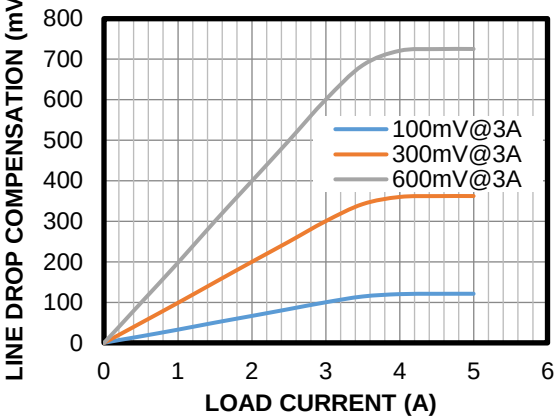
R_{SENS} = 5mΩ, no line compensation



IMON Voltage vs. Load Current



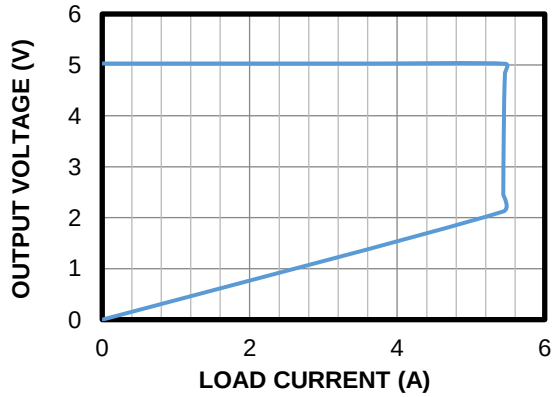
Line Drop Compensation vs. Load Current



TYPICAL CHARACTERISTICS *(continued)*

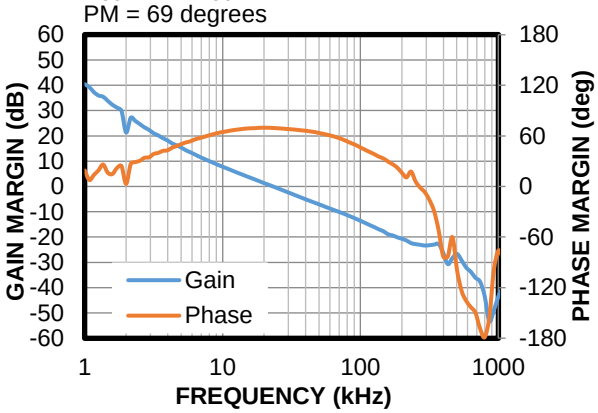
V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

CC/CV Curve



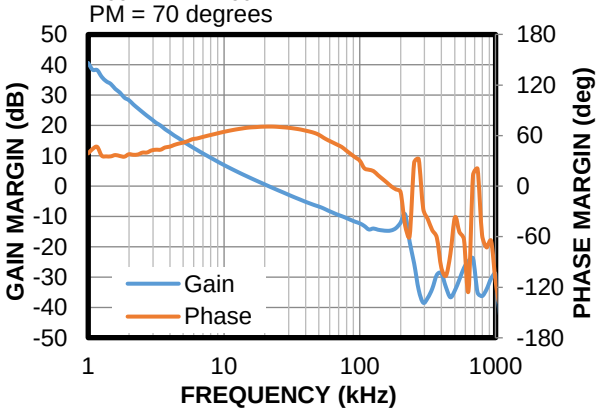
Bode Plot

V_{OUT} = 5V, I_{OUT} = 3A, BW = 23kHz,
PM = 69 degrees



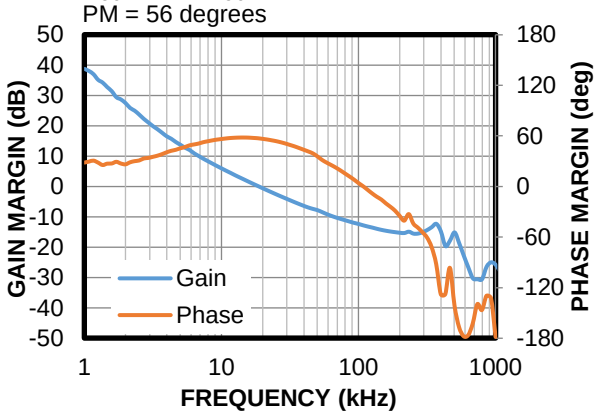
Bode Plot

V_{OUT} = 12V, I_{OUT} = 3A, BW = 21kHz,
PM = 70 degrees



Bode Plot

V_{OUT} = 20V, I_{OUT} = 3A, BW = 19kHz,
PM = 56 degrees

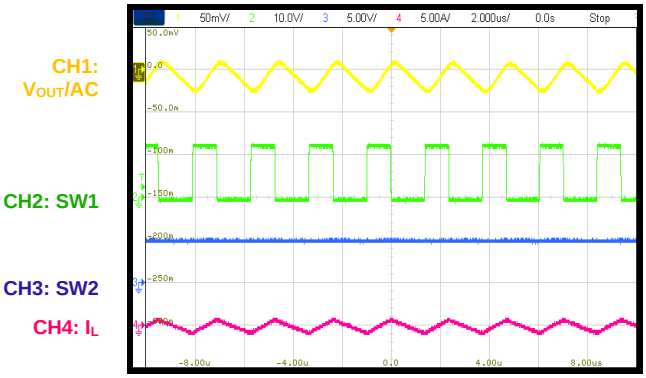


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

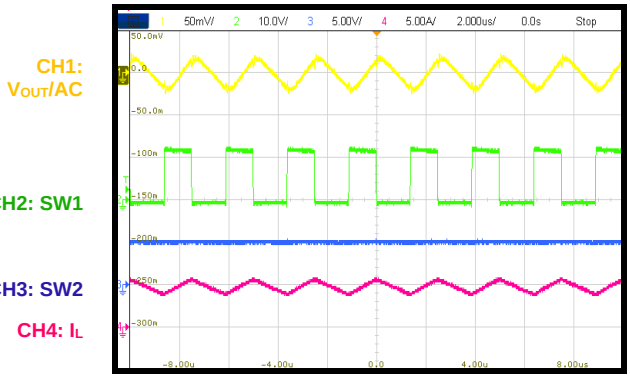
Output Voltage Ripple

V_{OUT} = 5V, load = 0A



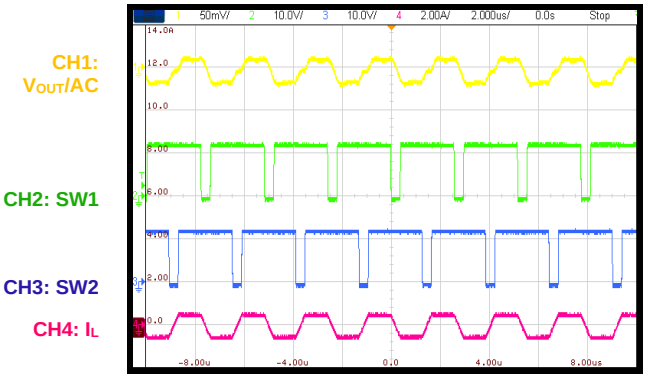
Output Voltage Ripple

V_{OUT} = 5V, load = 5A



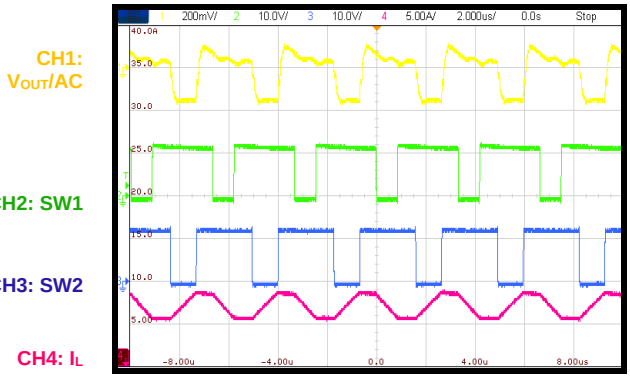
Output Voltage Ripple

V_{OUT} = 12V, load = 0A



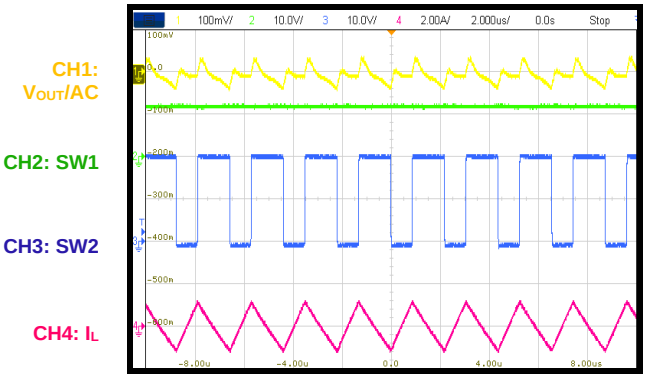
Output Voltage Ripple

V_{OUT} = 12V, load = 5A



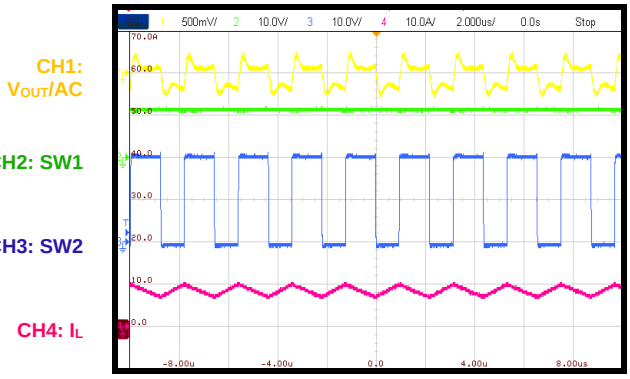
Output Voltage Ripple

V_{OUT} = 20V, load = 0A



Output Voltage Ripple

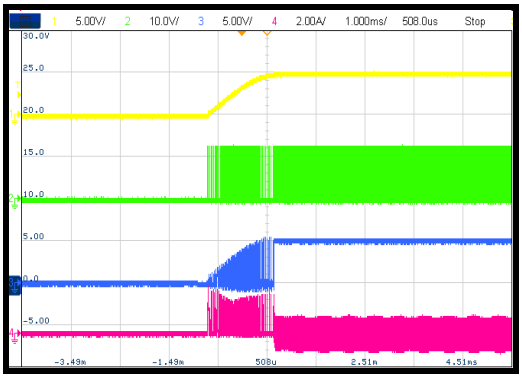
V_{OUT} = 20V, load = 5A



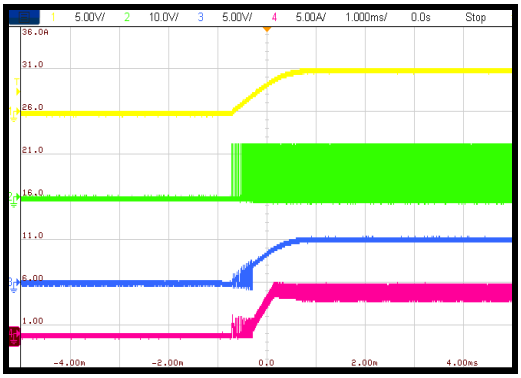
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

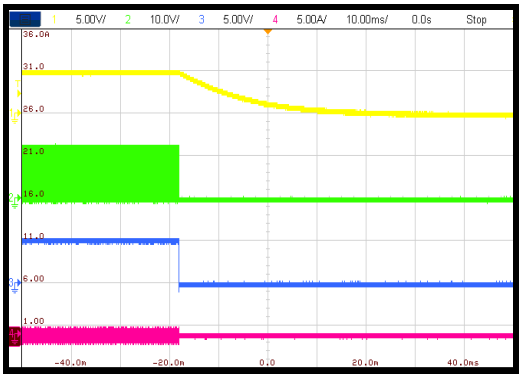
I²C Operation Enabled
Load = 0A



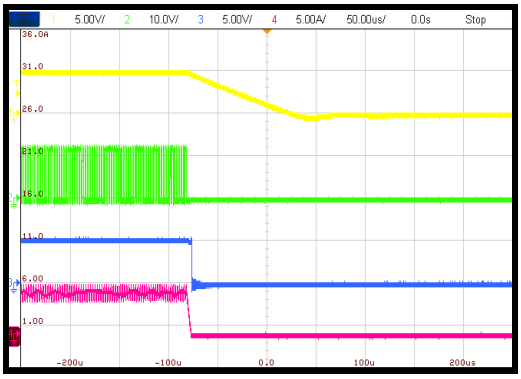
I²C Operation Enabled
Load = 5A



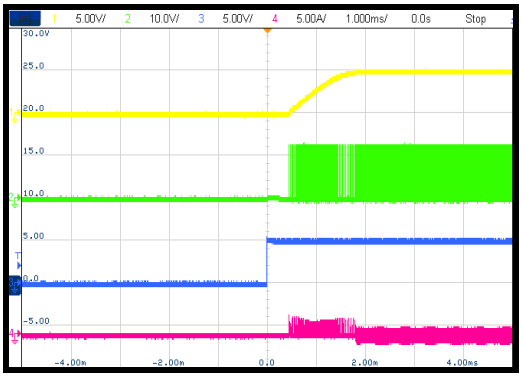
I²C Operation Disabled
Load = 0A



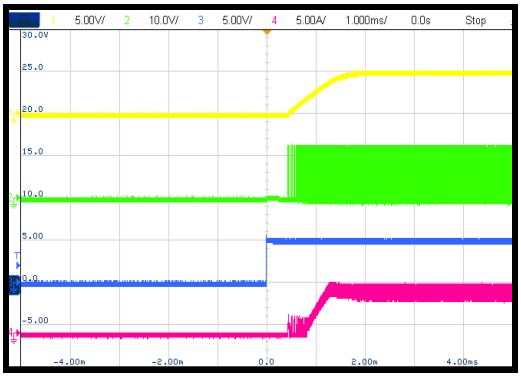
I²C Operation Disabled
Load = 5A



Start-Up through EN
Load = 0A



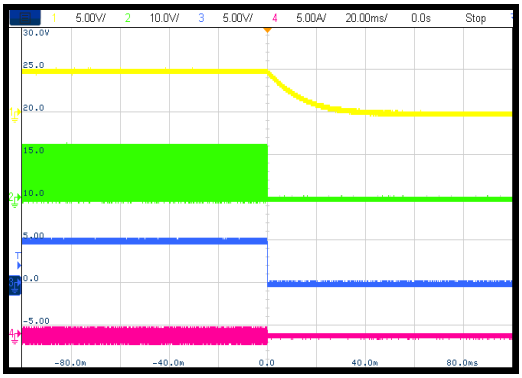
Start-Up through EN
Load = 5A



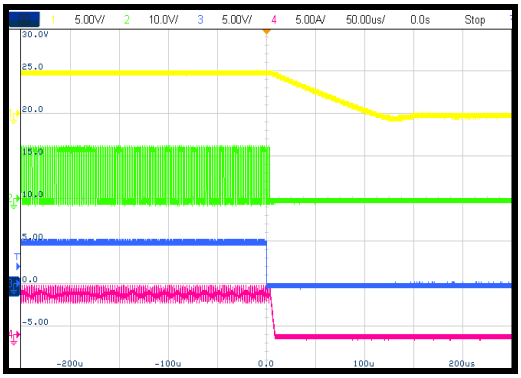
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

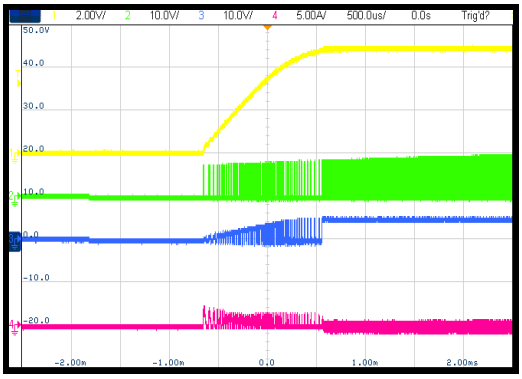
Shutdown through EN
Load = 0A



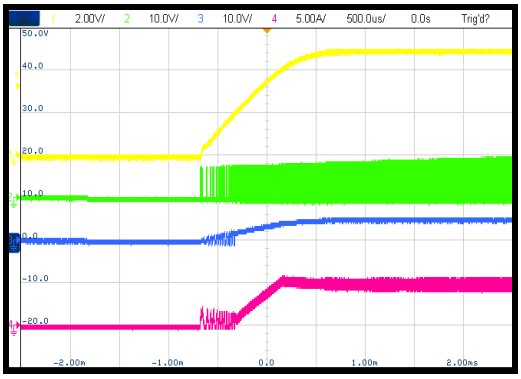
Shutdown through EN
Load = 5A



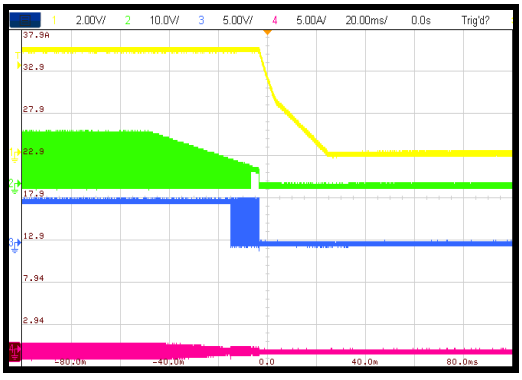
Input Start-Up
Load = 0A



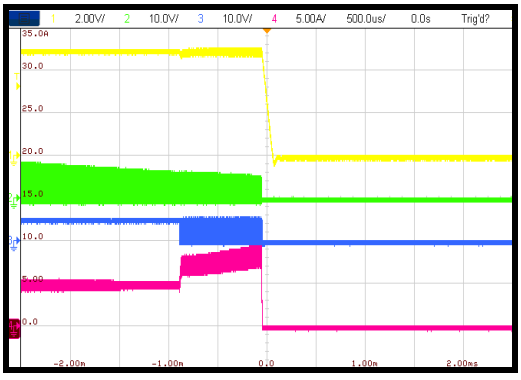
Input Start-Up
Load = 5A



Input Shutdown
Load = 10mA, EN divider ratio = 1:5



Input Shutdown
Load = 5A, EN divider ratio = 1:5

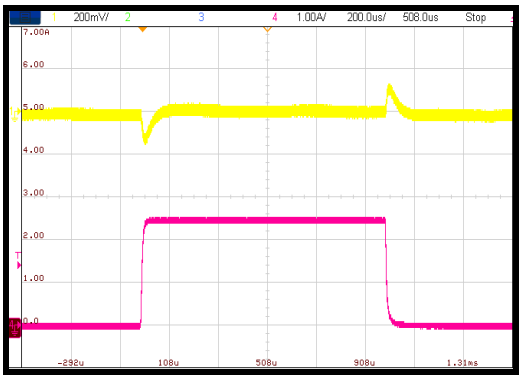


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

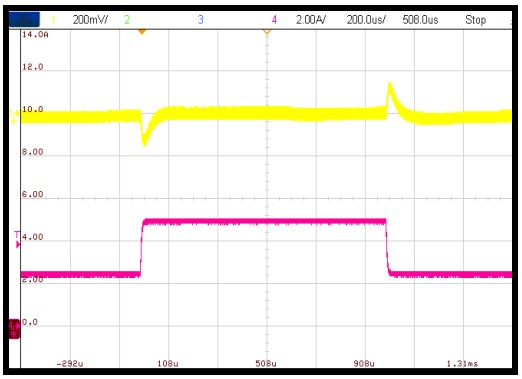
Load Transient Response

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A to 2.5A, 150mA/µs



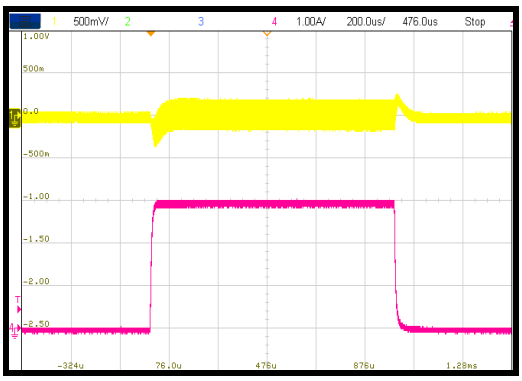
Load Transient Response

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2.5A to 5A, 150mA/µs



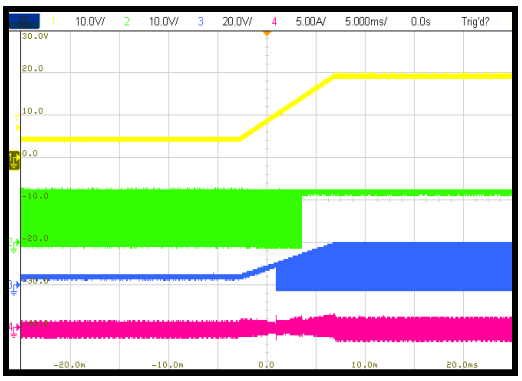
Load Transient Response

V_{IN} = 12V, V_{OUT} = 20V, I_{OUT} = 0A to 3A, 150mA/µs



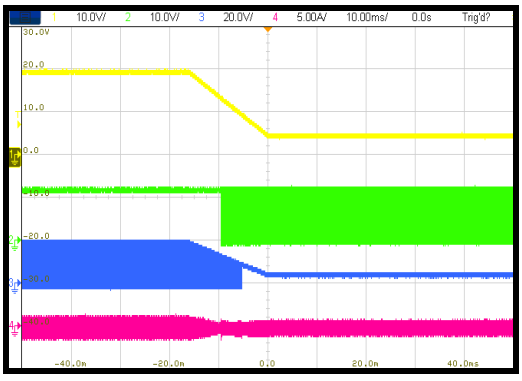
Output Voltage Transition

V_{OUT} = 5V to 20V, I_{OUT} = 0A



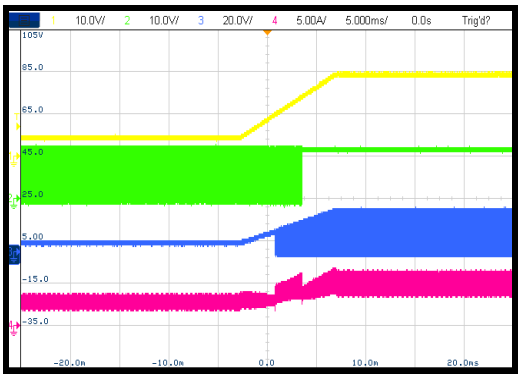
Output Voltage Transition

V_{OUT} = 20V to 5V, I_{OUT} = 0A



Output Voltage Transition

V_{OUT} = 5V to 20V, I_{OUT} = 3A

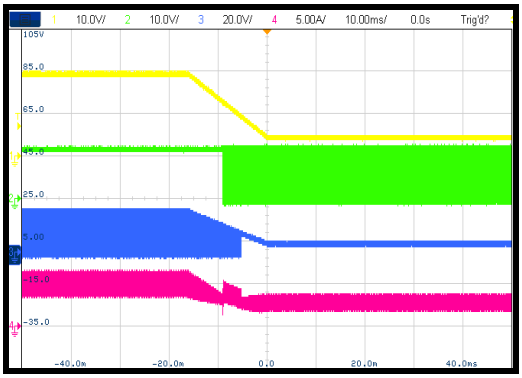


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

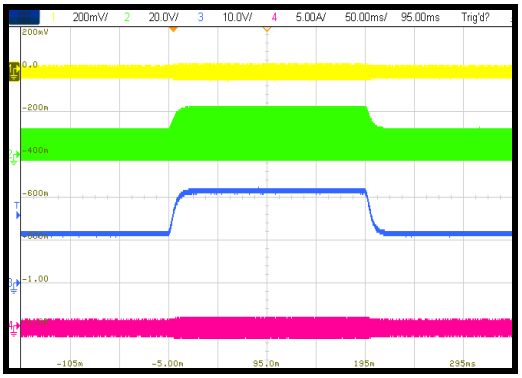
Output Voltage Transition

V_{OUT} = 20V to 5V, I_{OUT} = 3A



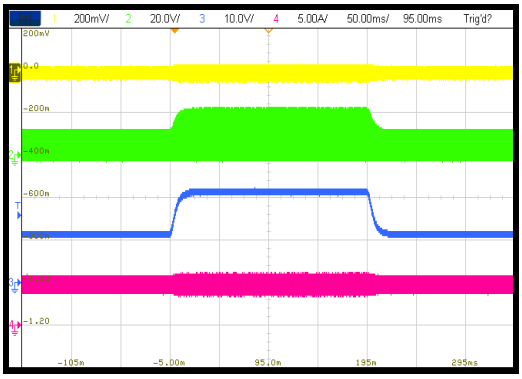
Input Voltage Transient Response

V_{IN} = 12V to 22V, V_{OUT} = 5V, load = 0A



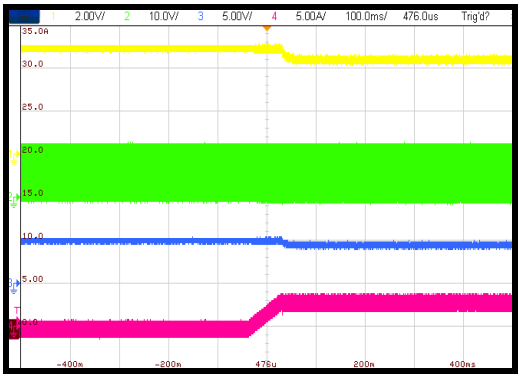
Input Voltage Transient Response

V_{IN} = 12V to 22V, V_{OUT} = 5V, load = 5A

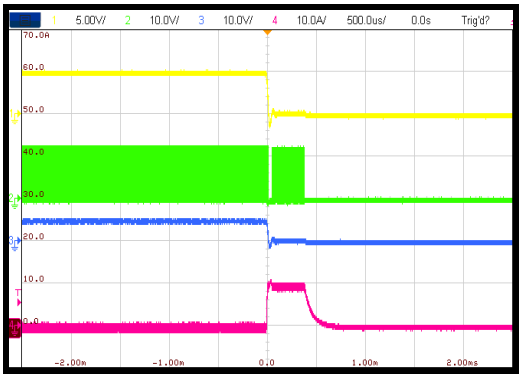


CC Entry

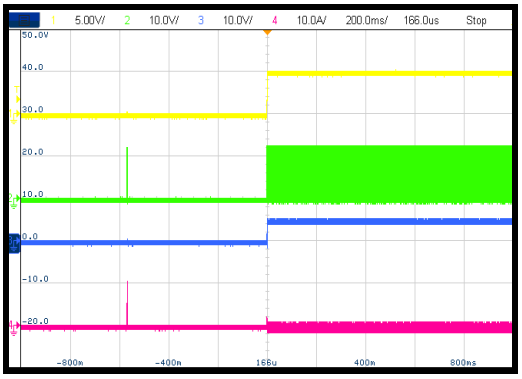
CV load = 4.5V, CC limit = 3A



Short-Circuit Protection Entry



Short-Circuit Protection Recovery



FUNCTIONAL BLOCK DIAGRAM

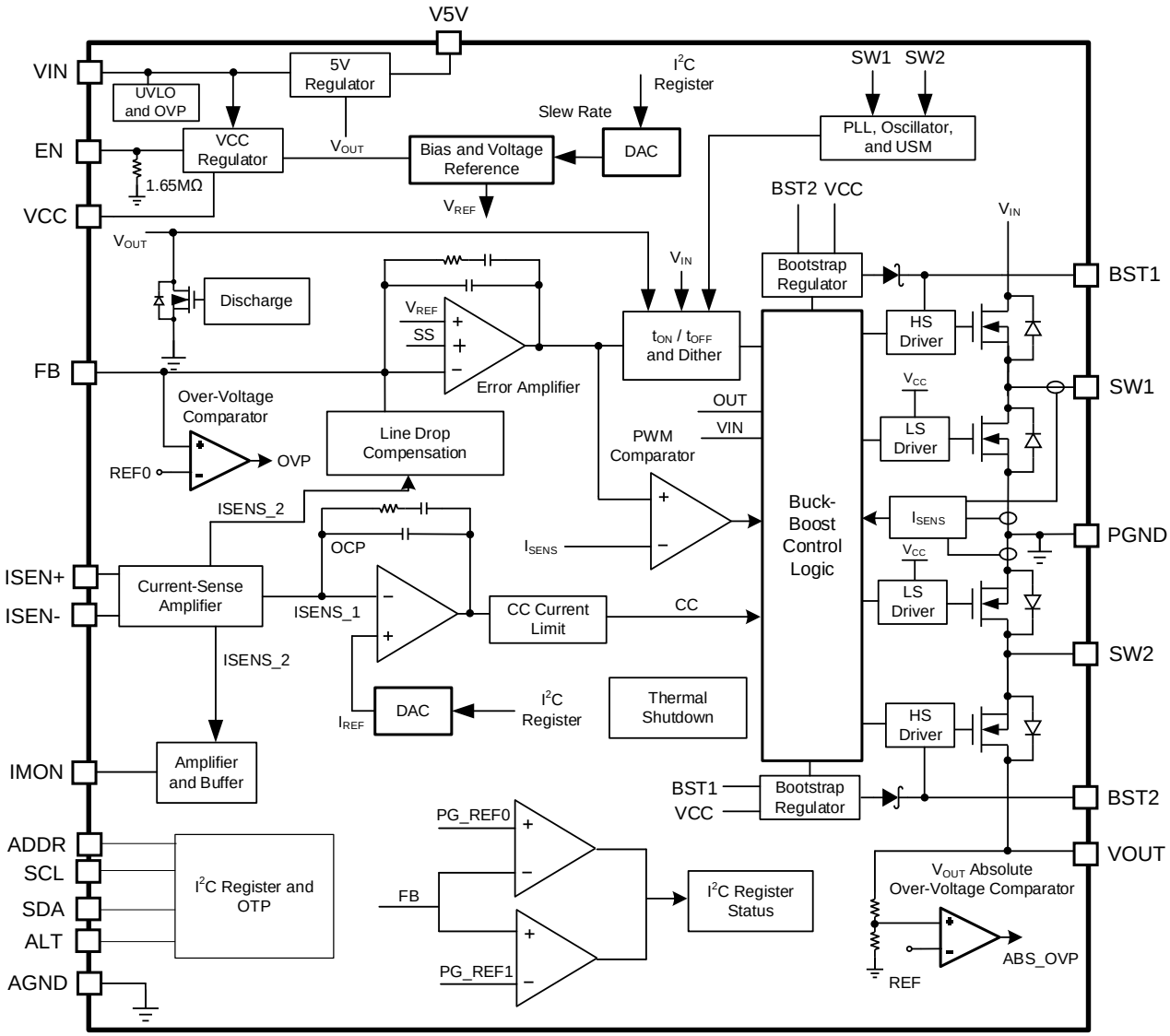


Figure 2: Functional Block Diagram

OPERATION

The MP4246 is a buck-boost converter with four integrated MOSFETs. The device works with a fixed frequency for all modes (buck, boost, and buck-boost). A special buck-boost control strategy provides high efficiency across the full input range, with a smooth transient between different modes. Figure 2 on page 18 shows the functional block diagram.

Buck-Boost Operation

The MP4246 can regulate the output voltage (V_{OUT}) above, equal to, or below the input voltage (V_{IN}). The device has a one-inductor, four-switch (SWA, SWB, SWC, and SWD) power structure (see Figure 3).

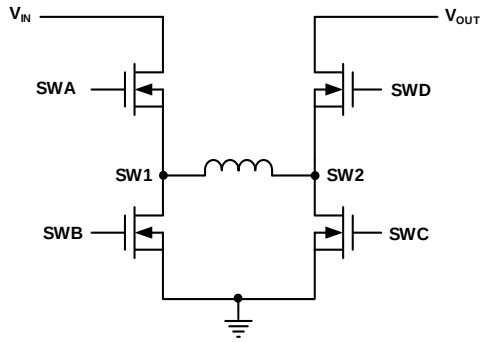


Figure 3: Buck-Boost Topology

Based on this architecture, the MP4246 can operate in buck mode, boost mode, or buck-boost mode with different V_{IN} inputs (see Figure 4).

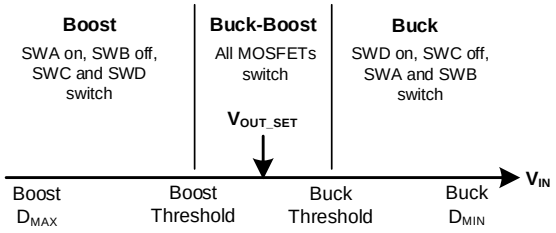


Figure 4: Buck-Boost Operation Range

Buck Mode (V_{IN} > V_{OUT})

When V_{IN} significantly exceeds V_{OUT}, the MP4246 operates in buck mode. SWA and SWB switch for buck regulation. Meanwhile, SWC is off, and SWD remains on to conduct the inductor current (I_L).

In each buck mode cycle, SWA turns on first when the FB voltage (V_{FB}) drops below the reference voltage (V_{REF}). After SWA turns off, SWB turns on to conduct I_L until it triggers the COMP control signal. By repeating this operation, the converter regulates V_{OUT}.

Boost Mode (V_{IN} < V_{OUT})

When V_{IN} is significantly below V_{OUT}, the MP4246 operates in boost mode. In boost mode, SWC and SWD switch for boost regulation. Meanwhile, SWB is off, and SWA remains on to conduct I_L.

In each boost mode cycle, SWC turns on to conduct I_L. When I_L rises and triggers the control signal on the COMP pin, SWC turns off and SWD turns on for the freewheeling current. Then SWC turns on and off repeatedly to regulate V_{OUT} in boost mode.

Buck-Boost Mode (V_{IN} ≈ V_{OUT})

When V_{IN} is almost equal to V_{OUT}, the MP4246 cannot provide sufficient energy to the load in buck mode due to SWA's minimum off time. In boost mode, the converter supplies too much power to the load due to SWC's minimum on time. Under these conditions, the MP4246 adopts buck-boost control to regulate the output (see Figure 5).

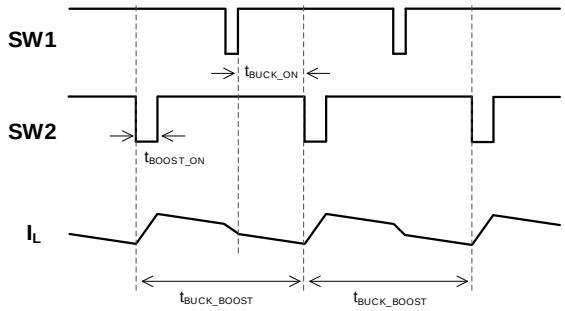


Figure 5: Buck-Boost Waveform

If V_{IN} is almost equal to V_{OUT}, the device operates in buck-boost mode, and one boost switching is inserted into each buck switching period. The MOSFETs turn on in the following sequence:

1. SWA and SWC
2. SWA and SWD
3. SWB and SWD
4. SWA and SWD

This process allows I_L to meet the COMP voltage (V_{COMP}) requirement while also suppling sufficient current to the output.

VCC Power Supply

The MP4246's internal circuit (including the gate drivers) is powered by VCC. When V_{IN} is supplied and EN is high (V_{IN} > 3.73V and V_{EN} > 0.68V), the MP4246 tries to regulate the VCC voltage (V_{CC}) at 3.54V. VCC is only supplied by V_{IN}. VCC, BST1, and BST2 have separate under-voltage lockout (UVLO) thresholds that keep the gate signal off.

Enable (EN) Control

The MP4246's high-voltage EN pin can be connected to VIN via a resistor. It also can configure the EN divider resistor to set the VIN on/off threshold (see Figure 6).

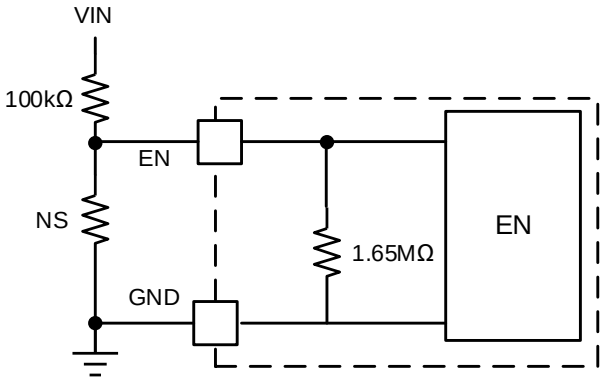


Figure 6: EN Connection

EN provides two different thresholds. If the EN pin voltage (V_{EN}) exceeds 0.68V, then VCC and V5V start to work. If V_{EN} exceeds 1.32V, then switching is enabled (see Figure 7).

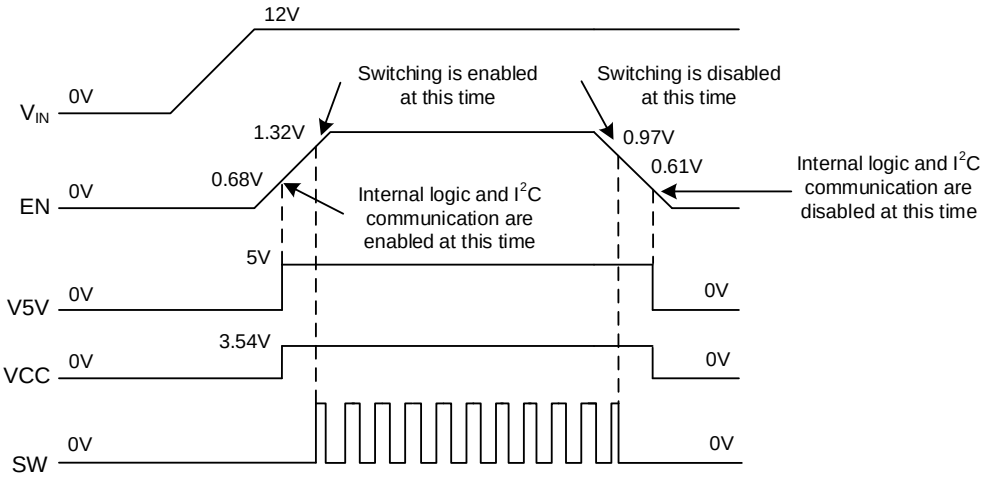


Figure 7: EN On/Off Sequence

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors V_{IN} and V_{CC}. The MP4246 is enabled when V_{IN} and V_{CC} exceed their UVLO rising thresholds ($V_{IN\_UVLO\_R}$ and $V_{CC\_UVLO\_R}$, respectively). If V_{IN} drops below its UVLO falling threshold, the IC stops switching and initiates V_{OUT} discharge. The entire IC is disabled once V_{CC} drops below its UVLO threshold.

Internal Soft Start (SS)

Soft start (SS) prevents the converter's V_{OUT} from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to V_{CC}. When V_{SS} is below V_{REF}, the error amplifier (EA) uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the EA uses V_{REF} as the reference. The MP4246 fixes the soft-start time (t_{SS}) at 1ms when V_{OUT} is set to 5V.

If the output of the MP4246 is pre-biased to a set voltage during start-up, then the IC disables the switching of both the high-side and low-side MOSFETs (HS-FET and LS-FET, respectively) until the voltage on the internal soft-start capacitor (C_{SS}) exceeds the internal V_{FB}.

Constant Current (CC) Mode Over-Current-Protection

The MP4246 senses the output current (I_{OUT}) or input current (I_{IN}) via the ISEN+ and ISEN- pins. If I_{OUT} or I_{IN} exceeds the set current-limit threshold, then the MP4246 enters constant current (CC) limit mode. In this mode, the current amplitude is limited. As the load resistance is reduced, once I_{OUT} or I_{IN} reaches the current-limit threshold, V_{OUT} drops until V_{FB} drops below the under voltage (UV) threshold (typically 40% below V_{REF}). Once the UV threshold is triggered and V_{OUT} drops below 2.97V, the MP4246 enters hiccup mode to periodically restart the part.

This protection mode is especially useful when the output is dead-shorted to ground, which significantly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. Once the over-current (OC) condition is removed, the MP4246 exits hiccup mode.

Select a constant current-limit mode that works on the input or output side using factory trimming. See Figure 14 on page 39 for the output side connection, and see Figure 15 on page 39 for the input side connection.

I²C bit HICCUP_EN (D4h, bit[5]) can disable hiccup mode.

Switching Current Limit

The MP4246 senses the LS-FET current in the loop control. This allows the device to provide valley current limiting in buck mode and peak current limiting in boost mode during each cycle-by-cycle switching period. In buck mode, the next period does not start until I_L drops to the valley current limit, allowing the device to fold back the frequency when the valley current limit is triggered.

Based on the cycle-by-cycle switching current limit, the MP4246's maximum input current (I_{IN_MAX}) in buck mode can be calculated with Equation (1):

$$I_{IN\_MAX}(A) = \frac{V_{OUT}}{V_{IN}} \times \eta \times \left(\text{Valley Current Limit (A)} + \frac{V_{IN} - V_{OUT}}{2 \times L(\mu H) \times f_{SW}(kHz)} \times \frac{V_{OUT}}{V_{IN}} \times 10^3\right) \quad (1)$$

Where η is the efficiency.

I_{IN_MAX} in boost mode can be calculated with Equation (2):

$$I_{IN\_MAX}(A) = \text{Peak Current Limit (A)} - \frac{V_{IN}}{2 \times L(\mu H) \times f_{SW}(kHz)} \times \frac{V_{OUT} - V_{IN}}{V_{OUT}} \times 10^3 \quad (2)$$

The buck valley current limit is typically 9.6A. The boost peak current limit is typically 13.5A. These current limits are configurable via I²C command D3h, bits[7:6].

Output Over-Voltage Protection (OVP)

The MP4246 provides output over-voltage protection (OVP). If V_{FB} exceeds 118% of V_{REF}, then SWA, SWB, SWC, and SWD turn off. The resistor discharge path from the OUT pin to ground turns on. If V_{FB} drops to 107% of V_{REF}, then the chip resumes normal operation.

In addition, the MP4246 provides output absolute OVP. If V_{OUT} exceeds the output absolute OVP threshold (typically 25.5V rising and 24V falling), then the absolute OVP is triggered, switching is disabled, and the discharge resistor turns on.

Input Over-Voltage Protection (OVP)

The MP4246 provides input OVP and can withstand V_{IN} up to 36V. When V_{IN} exceeds the input OVP threshold (V_{IN_OVP}) (typically 24V) and 2µs, SWA, SWB, SWC, and SWD turn off to disable V_{OUT}, and the V5V low-dropout (LDO) regulator turns off. Two V_{IN} OVP thresholds (24V and 27.5V) are selectable through factory trimming.

Bootstrap (BST) Power

A capacitor between BST1 and SW1, and a capacitor between BST2 and SW2 are required to supply the power. These capacitors are powered by the internal diode from VCC or charged by each other. The regulated voltage of BST1 and BST2 is typically 3.54V. The BST power provides its own UVLO control.

Forced Continuous Conduction Mode (FCCM) or Forced Pulse-Width Modulation (PWM) Mode

In forced continuous conduction mode (FCCM), the buck on time and boost off time are determined by the internal circuit to achieve a fixed frequency based on the V_{IN} / V_{OUT} ratio. When the load decreases, the average I_{IN} drops, and I_L may go negative from V_{OUT} to V_{IN}

during the off time (SWD on). This forces I_L to work in continuous mode with a fixed frequency, producing a lower output voltage ripple (ΔV_{OUT}) compared to automatic pulse-frequency modulation (PFM) or pulse-width modulation (PWM) mode.

Automatic Pulse-Frequency Modulation (PFM), Automatic Pulse-Width Modulation Mode, or Pulse-Skip Mode (PSM)

In automatic PFM or PWM mode, once I_L drops to 0A, SWD turns off to prevent the current from flowing from V_{OUT} to PGND. This forces I_L to work in discontinuous conduction mode (DCM). At the same time, the internal off-timer clock stretches once the MP4246 enters DCM. The frequency drops when the I_L conduction period decreases, reducing power loss and ΔV_{OUT}.

If V_{COMP} drops to the pulse-skip mode (PSM) threshold, the MP4246 stops switching to minimize further switching power loss. The MP4246 recovers switching once V_{COMP} exceeds the PSM threshold. The switching pulse skips based on V_{COMP} under very light-load conditions. PSM achieves significantly higher efficiency compared to FCCM at light loads; however, ΔV_{OUT} in PSM may be higher compared to FCCM due to the group switching pulse.

Switching Frequency and Frequency Spread Spectrum (FSS)

The MP4246 configures the switching frequency (f_{SW}) with the 2-bit FREQ command. f_{SW} can be selected at 280kHz, 420kHz, 600kHz, or 1MHz. A 420kHz f_{SW} is typically recommended.

The MP4246 provides a frequency spread spectrum (FSS) function. Set DITHER_ENABLE (D0h, bit[7]) to 1 to enable this function. Set DITHER_ENABLE to 0 to disable the function. The purpose of spread spectrum is to minimize the peak emissions at certain frequencies.

The MP4246 uses a 2kHz triangle waveform to modulate the internal oscillator. The frequency span for spread spectrum operation is ±9% (see Figure 8).

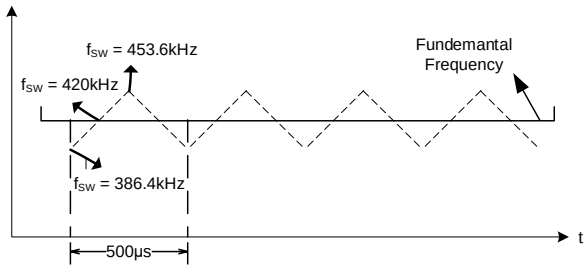


Figure 8: Frequency Spread Spectrum

The MP4246's spread frequency can be enabled for a 280kHz, 420kHz, 600kHz, or 1MHz f_{SW}.

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, then the chip is enabled. The bandgap reference block starts first, generating a stable V_{REF} and reference currents, and then the internal VCC regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

To enable the buck-boost output, I2C_EN must be turned on. I2C_EN is the logic or the result of two signals: the ADDR pin and the OPERATION bit (01h, bit[7]). For more details, refer to the ADDR Function section on page 23 and the OPERATION (01h) section on page 28.

Several events can shut down the chip: V_{EN} going low, V_{IN} going low, and thermal shutdown. Figure 9 shows the start-up and shutdown state machine.

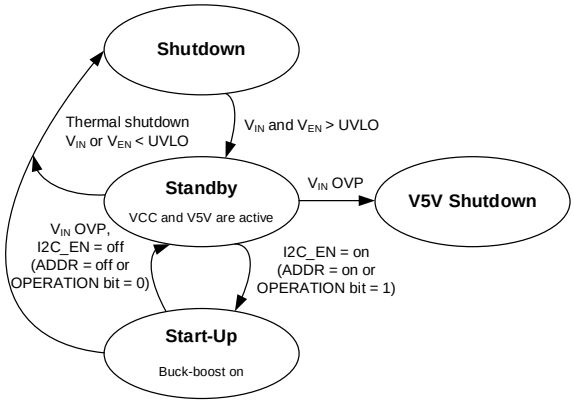


Figure 9: Start-Up and Shutdown State Machine

Slew-Rate Control and Output Discharge

The MP4246 sets the V_{OUT} change slew rate via the internal slew rate bits (D3h, bits[4:3] for the rising slew rate, and D3h, bits[2:1] for the falling slew rate. There are four types of V_{REF} change (rising and falling) slew rates that can be selected for different application requirements.

During a voltage transient, the discharge function works. The discharge function is disabled automatically after the V_{REF} change finishes. If the output capacitance (C_{OUT}) is too high, V_{OUT} may not discharge to the target voltage by the time the V_{REF} change completes. If this occurs, the OVP discharge function can continue discharging C_{OUT}.

The output discharge function is enabled if the following conditions are met:

1. V_{REF} is changed.
2. The output OVP threshold (exceeds 118% of V_{FB}) is triggered.
3. The I²C OPERATION bit is off, or the EN pin is off. Discharge works until a 250ms delay passes.
4. If V_{IN} UVLO is triggered but VCC has residual voltage, then the MP4246 discharges V_{OUT} for a limited time. This discharge function is disabled after V_{CC} drops below its UVLO threshold.

V5V Low-Dropout (LDO) Regulator

The V5V low-dropout (LDO) regulator uses V_{IN} as the input supply and outputs a fixed 5V voltage that can supply a 60mA load current. The V5V LDO is enabled once V_{IN} exceeds UVLO threshold and V_{EN} exceeds the EN rising threshold 1 ($V_{EN\_RISING1}$) (0.68V). In addition, the V5V LDO can use V_{OUT} as the input supply when V_{IN} is below 6V but V_{OUT} exceeds 6V. V5V remains on even when V_{IN} is below its UVLO threshold, until V_{CC} drops below its UVLO threshold. Once V_{IN} OVP is triggered, the V5V LDO turns off.

Output Line Drop Compensation

The MP4246 can compensate for a V_{OUT} drop, such as high impedance caused by a long trace, to maintain a fairly constant load-side voltage.

See the LINE_DROP_COMPENSATION bit (D2h, bits[1:0]) description on page 33 for more details regarding the line drop compensation amplitude.

ADDR Function

The ADDR pin can configure I²C slave address and the default I2C_EN status. I2C_EN is the logic or the result of the OPERATION bit value in the I²C and the ADDR pin status. The resistor divider on ADDR determines the values of bits[A7:A6] for the 7-bit I²C address, and bits[A5:A1] are I²C-configurable or one-time programmable (OTP) memory-configurable (see Figure 10).

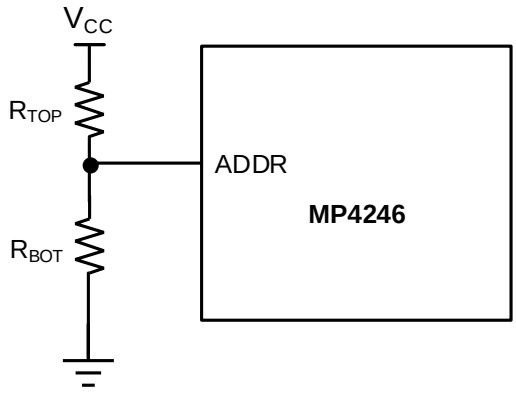


Figure 10 ADDR Connection

Table 1 shows the top resistance (R_{TOP}), bottom resistance (R_{BOT}), and I2C_EN values for bits[A5:A1] = 00111b (default).

Table 1: R_{TOP}, R_{BOT}, and I2C_EN of ADDR

Device Address	R_{TOP}	R_{BOT}	I2C_EN (10) (11)
67h	NS	0Ω	Off
47h	100kΩ	66.5kΩ	Off
27h	60.4kΩ	100kΩ	On
07h	0Ω	NS	On

Notes:

10) I2C_EN = on means that V_{OUT} is on by default once V_{IN} and V_{EN} exceed their respective UVLO thresholds.

11) I2C_EN = off means that V_{OUT} is off by default, and the user must set the OPERATION bit to 1 (either via the I²C or OTP) to enable V_{OUT}.

The ADDR status is latched after V_{IN} and V_{EN} exceed their UVLO thresholds. ADDR resets only when V_{CC} is below its UVLO threshold (pull the EN pin low or V_{IN} is below 2.4V typically).

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 165°C, the entire chip shuts down. Once the temperature falls below the lower threshold (typically 135°C), the chip is enabled and resumes normal operation.

I²C INTERFACE

I²C Serial Interface

The power management bus (PMBus) is an open-standard power management protocol that defines a means of communication with power conversion and other devices.

The I²C is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the lines, a master device generates an SCL signal and device address, then arranges the communication sequence. This is based on I²C operation principles.

Start and Stop Commands

The start and stop commands are signaled by the master device, which signifies the beginning and end of the I²C transfer. A start (S) command is defined as the SDA signal transitioning from high to low while SCL is high. A stop (P) command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 11).

The master then generates the SCL clocks and transmits the device address and the read/write (R/W) direction bit on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data is followed by an acknowledge (ACK) bit.

I²C Update Sequence

The MP4246 requires a start command, a valid I²C address, a register address byte, and a data byte for a single data update. The device acknowledges that is has received each byte by pulling the SDA line low during a single clock pulse's high period. A valid I²C address selects the MP4246. The device performs an update on the LSB byte's falling edge.

I²C Bus Message Format

Figure 12 on page 26 shows the I²C message format. Unshaded cells indicate that the bus host is actively driving the bus, and the shaded cells indicate that the MP4246 is driving the bus. The different symbols are defined below:

- S = Start command
- Sr = Repeated start command
- P = Stop command
- R = Read bit
- $\overline{W}$ = Write bit
- A = Acknowledge bit (0)
- $\overline{A}$ = Acknowledge bit (1)

"A" represents the ACK bit. ACK is typically active low (logic 0) if the transmitted byte is successfully received by a device.

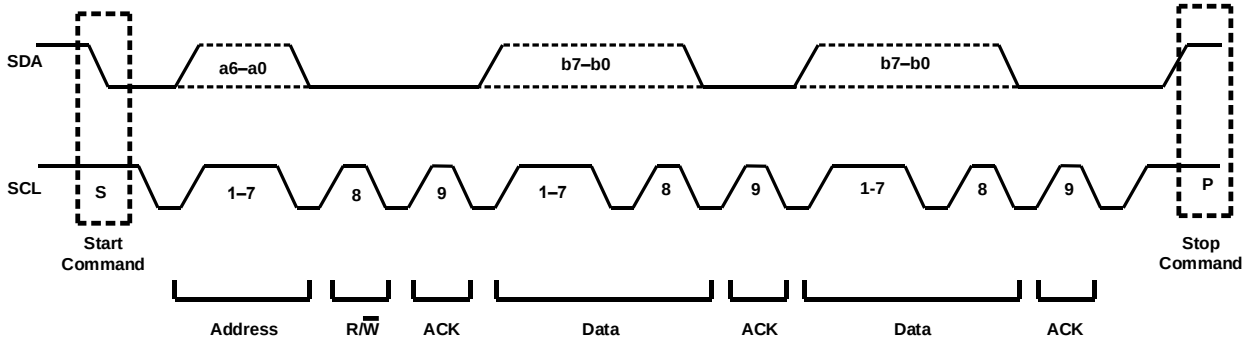


Figure 11: Data Transfer across the I²C

a) Send Byte

1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	P

b) Write Byte

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	P

c) Write Word

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P

d) Read Byte

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	$\overline{A}$	P

e) Read Word

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte Low	A

8	1	1
Data Byte High	$\overline{A}$	P

Figure 12: I²C Message Format

SUPPORTED I²C COMMANDS

Once V_{IN} and V_{EN} exceed their respective UVLO thresholds, the I²C is enabled. The default register value is based on MP4246-0000.

Command Code	Command Name	Type	Description	Data Format	Unit	OTP	Default Value
01h	OPERATION	R/W byte	On/off	Reg	-	Yes	0
03h	CLEAR_FAULTS	Send byte		Reg	-	No	-
21h	VOUT_COMMAND	R/W word		Linear (L16)	V	Yes	V_{REF} = 0.5V
79h	STATUS_WORD	R word		Reg	-	No	-
7Dh	STATUS_TEMPERATURE	R byte		Reg	-	No	-
D0h	MFR_CTRL1	R/W byte		Reg	-	Yes	-
D1h	MFR_CURRENT_LIMIT	R/W byte	Sets the constant current (CC) limit	Reg	-	Yes	5.4A
D2h	MFR_CTRL2	R/W byte		Reg	-	Yes	-
D3h	MFR_CTRL3	R/W byte		Reg	-	Yes	-
D4h	MFR_CTRL4	R/W byte		Reg	-	Yes	-
D8h	MFR_STATUS_MASK	R/W byte	Masks the ALT# pin indication	Reg	-	Yes	-
D9h	MFR_OTP_ CONFIGURATION_CODE	R/W byte	One-time programmable (OTP) memory configuration code	Reg	-	Yes	-
DAh	MFR_OTP_REVISION_ NUMBER	R/W byte	OTP software revision	Reg	-	Yes	-

Data Format

Linear16 (L16) format is used for VOUT_COMMAND. Figure 13 shows how to read V_{OUT}.

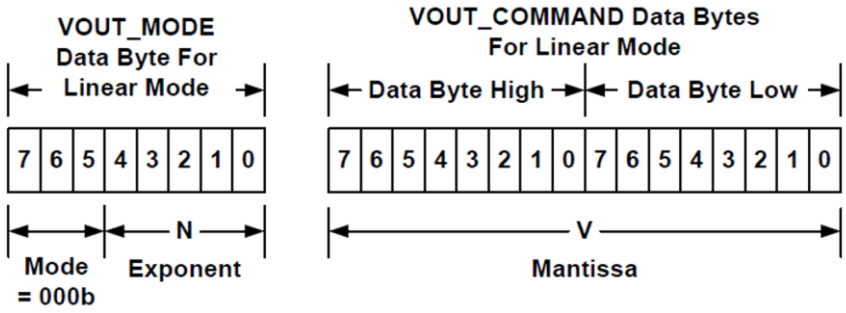


Figure 13: Read V_{OUT}

The MODE bits are set to 000b. The voltage can be calculated with Equation (3):

$$Voltage = V \times 2^{N} \quad (3)$$

Where Voltage is the parameter of interest (in V), *V* is a 16-bit unsigned binary integer, and *N* is a 5-bit, two's complement, binary integer.

REGISTER MAP

OPERATION (01h)

The OPERATION command configures the converter's operational state. The default OPERATION value is set via the one-time programmable (OTP) memory and the ADDR pin. If either OTP = 80h or the ADDR turns on EN, the chip automatically turns on the output. The default OTP bit is 00h. After start-up, the OPERATION bit can be changed via the I²C.

Bits	Access	Bit Name	Default	Description
7	R/W	OPERATION	1'b0	Sets the on/off state. The EN pin has higher control priority than this bit. 0: The output is off (default) 1: The output is on
6:0	R/W	RESERVED	7'b0000 000	Reserved.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command clears any fault bits that have been set. This command clears all bits in all status registers simultaneously. Meanwhile, the device clears (releases) its ALT# signal output if the ALT# signal has been asserted.

If the MP4246 latches off due to a fault condition, issuing a CLEAR_FAULTS command does not restart the device. If the fault remains present when the bit is cleared, then the fault bit is immediately set again and the host is notified by the fault condition. This command is write-only (see Figure 12 on page 26).

VOUT_COMMAND (21h)

The VOUT_COMMAND sets the output voltage. It follows the L16 linear data format.

Command	VOUT_COMMAND															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Data byte high								Data byte low							
Default Value (V_{REF} = 0.5V)	5120 decimal															

V_{OUT} (in V) can be calculated with Equation (4):

$$V_{OUT} = V \times 2^{-10} \quad (4)$$

Where *V* is a 16-bit, unsigned binary integer of VOUT_COMMAND, bits[15:0].

The valid V_{OUT} range is between 1V and 21.47V. Any voltages outside of this range are considered abnormal. The feedback resistor ratio should be V_{OUT} / V_{FB} = 10. The VOUT_COMMAND resolution is 10mV. The Internal reference voltage (V_{REF}) is equal to V_{OUT} / 10. The internal V_{REF} range is between 0.1V and 2.147V with 1mV/step, for a total of 2047 steps. This value is controlled by the 11-bit digital-to-analog converter (DAC). When the DAC input is set to 0, the DAC output is 0.1V.

STATUS_WORD (79h)

The STATUS_WORD command returns 2 bytes of information with a summary of the MP4246's fault condition. Based on the information in these bytes, the host can obtain more information by reading the relevant status registers. All STATUS_WORD bits remain set, except for the PG_STATUS# bits. This bit always reflects the current state of the POWER_GOOD signal (if present).

Byte	Bits	Access	Bit Name	Default	Description
Low	7	R	RESERVED	1'b0	Reserved. The default value is 0b.
	6	R	RESERVED	1'b0	Reserved. The default value is 0b.
	5	R	VOUT_OV_FAULT	1'b0	Indicates whether an output over-voltage (OV) fault has occurred.
	4	R	IOUT_OC_FAULT	1'b0	Indicates whether an output over-current (OC) fault has occurred. If the device reaches the constant current (CC) limit or the peak current limit, or if the device enters hiccup mode, then this bit is set.
	3	R	VIN_OV_FAULT	1'b0	Indicates whether an input voltage (V_{IN}) OV fault has occurred.
	2	R	TEMPERATURE	1'b0	Indicates whether a temperature fault or warning has occurred.
	1	R	RESERVED	1'b0	Reserved. The default value is 0b.
	0	R	RESERVED	1'b0	Reserved. The default value is 0b.
High	7	R	VOUT	1'b0	Indicates whether an output voltage (V_{OUT}) fault or warning has occurred.
	6	R	IOUT/POUT	1'b0	Indicates whether an output current (I_{OUT}) fault has occurred. If the device reaches the CC limit or peak current limit, or if the device enters hiccup mode, then this bit is set.
	5	R	RESERVED	1'b0	Reserved. The default value is 0b.
	4	R	OC_EXIT	1'b0	Indicates whether I_{OUT} has exited the CC limit. This bit is only set high when I_{OUT} exits CC mode (before entering hiccup mode). This bit does not reset once the device recovers from hiccup mode.
	3	R	PG_STATUS#	1'b0	The POWER_GOOD signal, if present, is ignored. If this bit is set 1, V_{OUT} is not power good. Once V_{OUT} is power good, this bit is cleared.
	2	R	RESERVED	1'b0	Reserved. The default value is 0b.
	1	R	RESERVED	1'b0	Reserved. The default value is 0b.
	0	R	RESERVED	1'b0	Reserved. The default value is 0b.

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command returns 1 data byte with information regarding the MP4246.

Bits	Access	Bit Name	Default	Description
7	R	OT_FAULT	1’b0	Indicates whether an over-temperature (OT) fault has occurred. The OTP entry threshold 165°C.
6	R	OT_WARNING	1’b0	Indicates whether an over-temperature warning (OTW) has occurred. The OTW entry threshold is 135ºC.
5	R	RESERVED	1’b0	Reserved.
4	R	RESERVED	1’b0	Reserved.
3	R	RESERVED	1’b0	Reserved.
2	R	RESERVED	1’b0	Reserved.
1	R	RESERVED	1’b0	Reserved.
0	R	RESERVED	1’b0	

I²C Register Map

Add	Name	Type	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
D0h	MFR_CTRL1	R/W	DITHER_ ENABLE	FREQ		PWM/PFM_ MODE		OUTPUT_ OVP_ EN	OUTPUT_ DISCHARGE_ EN	RSENS
D1h	MFR_CURRENT_ LIMIT	R/W	LDC_ DISABLE	CONSTANT_CURRENT_LIMIT (0.5A to 6.35A, 50mA/step)						
D2h	MFR_CTRL2	R/W	RESERVED						LINE_DROP_ COMPENSATION	
D3h	MFR_CTRL3	R/W	SWITCHING_ CURRENT_LIMIT		CC_ ADJ	SLEW_ RATE_ RISE		SLEW_ RATE_ FALL		FREQ_ MODE
D4h	MFR_CTRL4	R/W	CC_BLANK_ TIMER		HICCUP_ EN	I2C_ADDRESS (A5-A1)				
D8h	MFR_STATUS_ MASK	R/W	MFR_STATUS_MASK							
D9h	MFR_OTP_ CONFIGURATION_ CODE	R/W	MFR_OTP_CONFIGURATION_CODE							
DAh	MFR_OTP_ REVISION_ NUMBER	R/W	MFR_OTP_REVISION_NUMBER							

I²C Slave Address

The I²C slave address is 07h by default. The ADDR pin controls the value of bits[A7:A6], and OTP controls the value of bits[A5:A1] (see Table 2).

Table 2: I²C Slave Address and OPERATION Bit

ADDR Pin Voltage	I²C Address, Bits[A7:A1]		OPERATION Bit Default Value
	Binary	Hex	
Pull low	1100 111 (default)	67h	Off
37% x V_{CC}	1000 111 (default)	47h	Off
62% x V_{CC}	0100 111 (default)	27h	On
V_{CC}	0000 111 (default)	07h	On

MFR_CTRL1 (D0h)

Reset Value: Set via the OTP

The MFR_CTRL1 command sets the frequency mode, sets enable/disable output OVP and discharge, and selects the sense resistance (R_{SENS}).

Bits	Access	Bit Name	Default	Description
7	R/W	DITHER_ENABLE	1'b0	Enables the dither function. 0: No dither (default) 1: Enables the frequency spread spectrum (FSS) function
6:5	R/W	FREQ	2'b 01	Sets the buck-boost switching frequency (f_{SW}). 00: 280kHz 01: 420kHz (default) 10: 600kHz 11: 1MHz
4:3	R/W	PWM/PFM_MODE	2'b 01	Sets buck-boost mode. 00: Reserved 01: Forced pulse-width modulation (PWM) mode (default) 10: Automatic pulse-frequency modulation (PFM) or PWM mode 11: Reserved.
2	R/W	OUTPUT_OVP_EN	1'b1	Enables output over-voltage protection (OVP) control. 1: Enabled (default) 0: Disabled
1	R/W	OUTPUT_ DISCHARGE_EN	1'b1	Enables the output discharge function. 1: The MP4246 turns on the output discharge function during V_{EN}, V_{IN}, or I^2C off period (default) 0: Disables the output discharge function during V_{EN}, V_{IN}, or I^2C off period. This discharge works for a fixed 250ms.
0	R/W	RSENS	1'b0	Selects the external current-sense resistance. 0: 5mΩ (default) 1: 10mΩ

MFR_CURRENT_LIMIT (D1h)

Reset Value: Set via the OTP

The MFR_CURRENT_LIMIT command sets the output CC limit threshold.

Name	LDC_ DISABLE	CONSTANT_CURRENT_LIMIT						
Format	Direct, unsigned binary integer							
Bits	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value (5.4A)	0	108 integer						

The real-world over-current output current (I_{OUT_OC}) (in A) is calculated with Equation (5):

$$I_{OUT\_OC}\ (A) = IOUT\_LIM \times 0.05 \quad (5)$$

Where IOUT_LIM is a 7-bit, unsigned binary integer of IOUT_LIM, bits[6:0].

The 0.05 ratio is proportional to the resistance of the RSENS bit. To accurately calculate I_{OUT_OC}, the value of D0h, bit[0] must match the actual resistance of the RSENS bit used.

The I_{OUT_OC} resolution (or minimum step) is 50mA, with a 6.35A maximum.

Bit[7] enables line drop compensation control. If bit[7] = 0, then line drop compensation is controlled by D2h. If bit[7] = 1, then line drop compensation is disabled.

MFR_CTRL2 (D2h)

Reset Value: Set via the OTP

The MFR_CTRL2 command sets V_{OUT} compensation vs. I_{OUT}.

Bits	Access	Bit Name	Default	Description
7:2	R	RESERVED	6'b0000 00	Reserved.
1:0	R/W	LINE_DROP_ COMPENSATION	2'b00	Sets V_{OUT} compensation vs. load current. 00: No compensation (default) 01: V_{OUT} compensates 100mV at 3A I_{OUT} 10: V_{OUT} compensates 300mV at 3A I_{OUT} 11: V_{OUT} compensates 600mV at 3A I_{OUT} These compensation amplitudes are fixed for any V_{OUT}. Line drop compensation is enabled for 3V and above V_{OUT}. It is clamped when I_{OUT} >3.6A.

MFR_CTRL3 (D3h)

Reset Value: Set via the OTP

The MFR_CTRL3 command sets the switching current limit, V_{OUT} slew rate, and frequency mode in buck-boost mode.

Bits	Access	Bit Name	Default	Description
7:6	R/W	SWITCHING_ CURRENT_LIMIT	2'b01	Sets the current limit of switch B (SWB) and switch C (SWC). bits[7:6] / SWC Peak Current Limit / SWB Valley Current Limit 00 / 9A / 6.6A 01 (default) / 13.5A / 9.6A 10 / 17.9A / 12.6A 11 / 22.4A / 15.5A
5	R/W	CC_ADJ	1'b0	Adjusts CC limit vs. V_{OUT} gain. 0: Does not add 50mA to the CC limit (default) 1: Adds 50mA to the CC limit
4:3	R/W	SLEW_RATE_RISE	2'b01	Sets the V_{OUT} adjusted rising slew rate. 00: 0.08mv/µs V_{REF} rising slew rate 01: 0.16mv/µs V_{REF} rising slew rate (default) 10: 0.4mv/µs V_{REF} rising slew rate 11: 0.8mv/µs V_{REF} rising slew rate The V_{OUT} slew rate can be calculated with the following equation: V_{OUT} slew rate = V_{REF} slew rate x feedback ratio Where the feedback ratio is 10 for the Typical Application Circuits section on page 39.

2:1	R/W	SLEW_RATE_FALL	2'b10	Sets the V_{OUT} adjusted falling slew rate. 00: 0.02mv/µs V_{REF} falling slew rate 01: 0.04mv/µs V_{REF} falling slew rate 10: 0.1mv/µs V_{REF} falling slew rate (default) 11: 0.2mv/µs V_{REF} falling slew rate The V_{OUT} slew rate can be calculated with the following equation: V_{OUT} slew rate = V_{REF} slew rate x feedback ratio Where the feedback ratio is 10 for the Typical Application Circuits section on page 39.
0	R/W	FREQ_MODE	1'b1	Sets the frequency mode under buck-boost conditions. 0: Reduces the frequency to half of the frequency in buck and boost mode 1: Maintains the same frequency as buck and boost mode (default)

MFR_CTRL4 (D4h)

Reset Value: Set via the OTP

The MFR_CTRL4 command sets the CC blank timer and I²C address, and controls hiccup mode at the current limit. The I²C slave address is 07h by default. The ADDR pin controls the A7 to A6 bits value, and the OTP controls the A5 to A1 bits value.

Bits	Access	Bit Name	Default	Description
7:6	R/W	CC_BLANK_TIMER	2'b01	Sets the blank time before the MP4246 enters CC mode. 00: 320µs 01: 2ms (default) 10: 16ms 11: 80ms
5	R/W	HICCUP_EN	1'b1	Enables hiccup mode at the current limit. 0: Disabled 1: Enabled (default)
4:0	R/W	I2C_ADDRESS	5'b0011 1	Sets the I²C slave address, bits[A5:A1]. Bits[A7:A6] are determined by the ADDR pin. The default value is 00111b. The I²C slave address is 07h when ADDR is pulled to VCC.

MFR_STATUS_MASK (D8h)

Reset Value: Set via the OTP

The MFR_STATUS_MASK command only can mask off the behavior of the ALT# pin, while STATUS_WORD (79h) and OTP in STATUS_TEMPERATURE (7Dh) indicates each event.

Bits	Access	Bit Name	Default	Description
7	R/W	VOUT_MSK	1'b1	0: Not masked 1: Mask is enabled (default)
6	R/W	IOUT/POUT_MSK	1'b0	0: Not masked (default). This bit masks IOUT_OC_FAULT, IOUT/POUT, and OC_EXIT 1: Mask is enabled
5	R/W	VIN_MSK	1'b1	0: Not masked 1: Mask is enabled (default)

4	R/W	TEMP_MSK	1'b1	Masks the temperature. 0: Not masked 1: Mask is enabled (default)
3:2	R/W	PG_MSK	2'b11	Controls masking the PG rising and falling edges. PG rising means V_{OUT} transitions from not power good to power good. 00: Not masked. The ALT pin indicates both the PG rising and PG falling edges 01: The ALT pin only indicates PG rising, meaning PG_STATUS# changes from 1 to 0 10: The ALT pin only indicates the PG falling edge, meaning PG_STATUS# changes from 0 to 1 11: The ALT pin does not indicate any PG edge changes (default) Note that ALT is not pulled down during the first PG rising.
1	R/W	RESERVED	1'b0	Reserved. The default value is 0b.
0	R/W	UNKNOWN_MSK	1'b1	0: Not masked 1: Mask is enabled

MFR_OTP_CONFIGURATION_CODE (D9h)

Reset Value: Set via the OTP

The MFR_OTP_CONFIGURATION_CODE command sets the OTP configuration code.

Bits	Access	Bit Name	Description
7:0	R/W	OTP_CONFIGURATION_CODE	Sets the OTP configuration code defined by MPS.

MFR_OTP_REVISION_NUMBER (DAh)

Reset Value: Set via the OTP

The MFR_OTP_REVISION_NUMBER command sets the OTP software revision number.

Bits	Access	Bit Name	Description
7:0	R/W	OTP_REVISION_NUMBER	Sets the OTP software revision number defined by MPS.

APPLICATION INFORMATION

Selecting the Inductor

The inductor selection is based on the mode. The inductance for buck mode (L_{BUCK}) can be calculated with Equation (6):

$$L_{BUCK} = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

Where ΔI_L is the peak-to-peak inductor ripple current, which is 30% to 50% of the maximum load current (I_{LOAD_MAX}).

For boost mode, the inductor should limit ΔI_L between 30% and 50% of I_{IN_MAX}. The target inductance for boost mode (L_{BOOST}) can be calculated with Equation (7):

$$L_{BOOST} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I_L} \quad (7)$$

I_{IN_MAX} can be calculated with Equation (8):

$$I_{IN\_MAX} = \frac{V_{OUT} \times I_{LOAD\_MAX}}{V_{IN} \times \eta} \quad (8)$$

Where ΔI_L is about 30% to 50% of I_{IN_MAX}, and η is the efficiency.

Choosing a larger inductance reduces the ripple current but also increases the size of the inductor and reduces the converter's achievable bandwidth by moving the right half-plane zero to lower frequencies. Choose an inductor that meets the application requirements.

Selecting the Input Capacitor

I_{IN} in buck mode is discontinuous, and I_{IN} in boost mode is continuous. This means a capacitor is required to supply the AC current to the converter in buck mode while maintaining the DC V_{IN}. Ceramic capacitors are recommended for the best performance and should be placed as close to the VIN pin as possible. Capacitors with X5R or X7R ceramic dielectrics are recommended because they are fairly stable amid temperature fluctuations. The capacitors must also have a ripple current rating greater than the converter's maximum input ripple current.

The input ripple current in buck mode (I_{CIN}) can be calculated with Equation (9):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (9)$$

The worst-case condition in buck mode occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (10):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (10)$$

For simplification, choose the input capacitor (C_{IN}) with an RMS current rating greater than half of I_{LOAD_MAX}.

C_{IN} determines the converter's input voltage ripple (ΔV_{IN}). If there is a ΔV_{IN} requirement in the system, choose C_{IN} to meet the specification.

ΔV_{IN} in buck mode can be calculated with Equation (11):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (12):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (12)$$

ΔV_{IN} in boost mode can be estimated with Equation (13):

$$\Delta V_{IN} = \frac{V_{IN}}{8 \times f_{SW}^2 \times L \times C_{IN}} \times (1 - \frac{V_{IN}}{V_{OUT}}) \quad (13)$$

If using polymer, hybrid, or low-ESR electrolytic capacitors, the ESR dominates the impedance at f_{SW}. ΔV_{IN} in boost mode can be estimated with Equation (14):

$$\Delta V_{IN} = \frac{V_{IN}}{f_{SW} \times L} \times (1 - \frac{V_{IN}}{V_{OUT}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{IN}}) \quad (14)$$

Selecting the Output Capacitor

In boost mode, I_{OUT} is discontinuous, meaning the output capacitor (C_{OUT}) must be capable of reducing ΔV_{OUT}.

A higher capacitance may be required to reduce ΔV_{OUT} and transient response. It is recommended to use low-ESR capacitors, such as ceramic capacitors with X5R or X7R dielectrics. If using ceramic capacitors, the impedance of the capacitor at f_{SW} is dominated by the capacitance, which means ΔV_{OUT} is independent of the ESR. ΔV_{OUT} in buck mode can be estimated with Equation (15):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

If using polymer, hybrid, or low-ESR electrolytic capacitors, the ESR dominates the impedance at f_{SW}. In this scenario, ΔV_{OUT} in buck mode can be estimated with Equation (16):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (16)$$

Where R_{ESR} is the equivalent series resistance of C_{OUT}.

ΔV_{OUT} in boost mode can be estimated with Equation (17):

$$\Delta V_{OUT} = \frac{(1 - \frac{V_{IN}}{V_{OUT}}) \times I_{LOAD}}{C_{OUT} \times f_{SW}} \quad (17)$$

If using polymer, hybrid, or low-ESR electrolytic capacitors, the ESR dominates the impedance at f_{SW}. ΔV_{OUT} in boost mode can be estimated with Equation (18):

$$\Delta V_{OUT} = \frac{(1 - \frac{V_{IN}}{V_{OUT}}) \times I_{OUT}}{C_{OUT} \times f_{SW}} + \frac{I_{OUT} \times R_{ESR} \times V_{OUT}}{V_{IN}} \quad (18)$$

Choose C_{OUT} to meet the ΔV_{OUT} and load transient response requirements of the design. Consider the capacitance derating when designing applications with high output voltages.

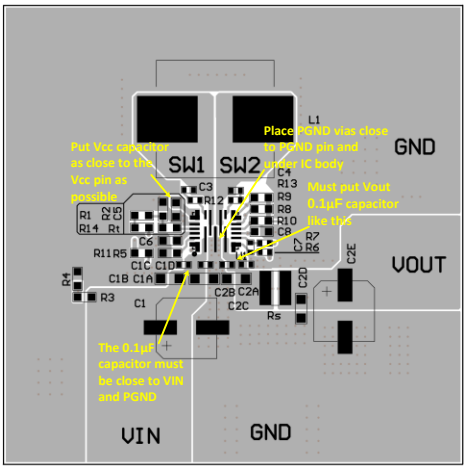
PCB Layout Guidelines (12)

Efficient PCB layout is critical for efficient operation and thermal dissipation. For the best results, refer to Figure 13 **Error! Reference source not found.**and follow the guidelines below:

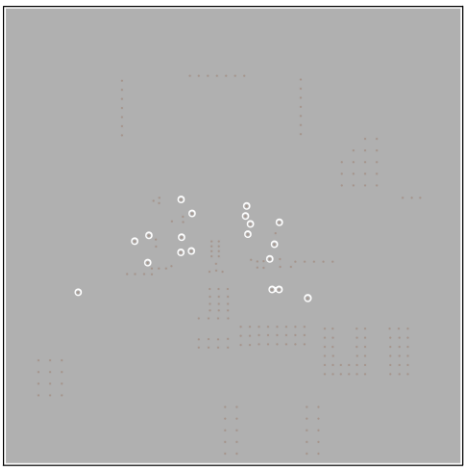
1. In buck mode, place the filter C_{IN} and VIN pin as close together as possible.
2. In boost mode, place the filter C_{OUT} and the OUT pin as close together as possible.
3. Use short, direct, and wide traces to connect OUT.
4. If necessary, add vias to ground after the output filter.
5. Use a large copper plane for PGND, and add multiple vias to improve thermal dissipation.
6. Connect AGND to PGND.
7. To improve EMI performance, place two ceramic input decoupling capacitors as close as possible to VIN, OUT, and PGND.
8. Place the input filter at the bottom layer for improved EMI performance.
9. Place the VCC decoupling capacitor as close as possible to VCC.
10. Kelvin connect the output current-sense traces (ISEN+ and ISEN-).

Note:

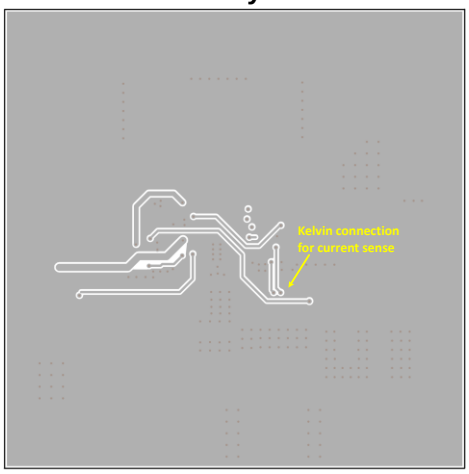
12) The recommended layout is based on the Typical Application Circuits section (see Figure 14 on page 39).



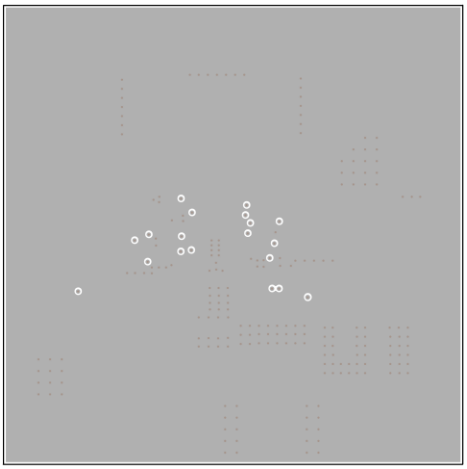
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 13: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

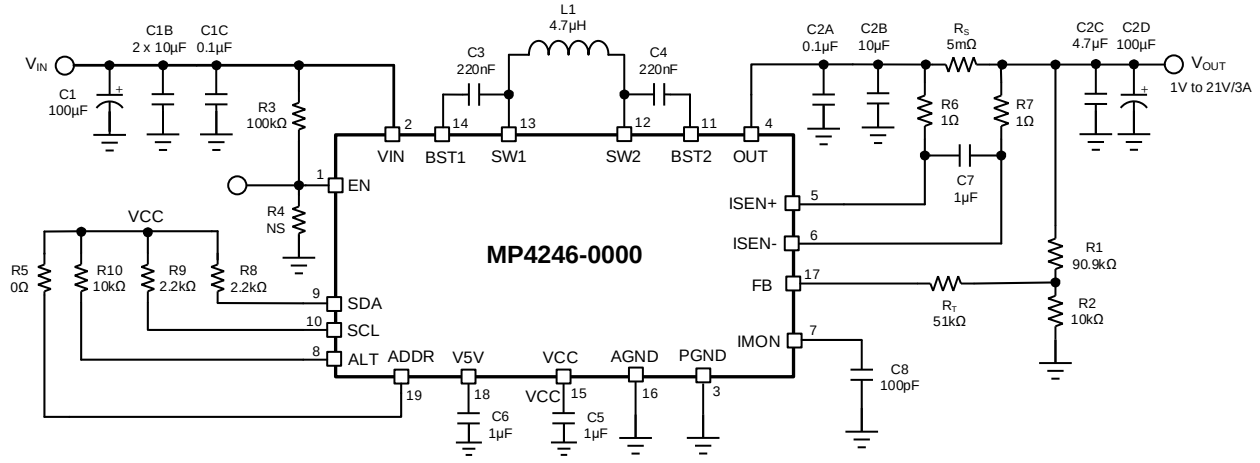


Figure 14: Typical Application Circuit (V_{IN} = 5V to 20V, default f_{SW} = 420kHz, V_{OUT} = 5V default (1V to 21V adjustable via the I²C), up to 5A applications) (13) (14)

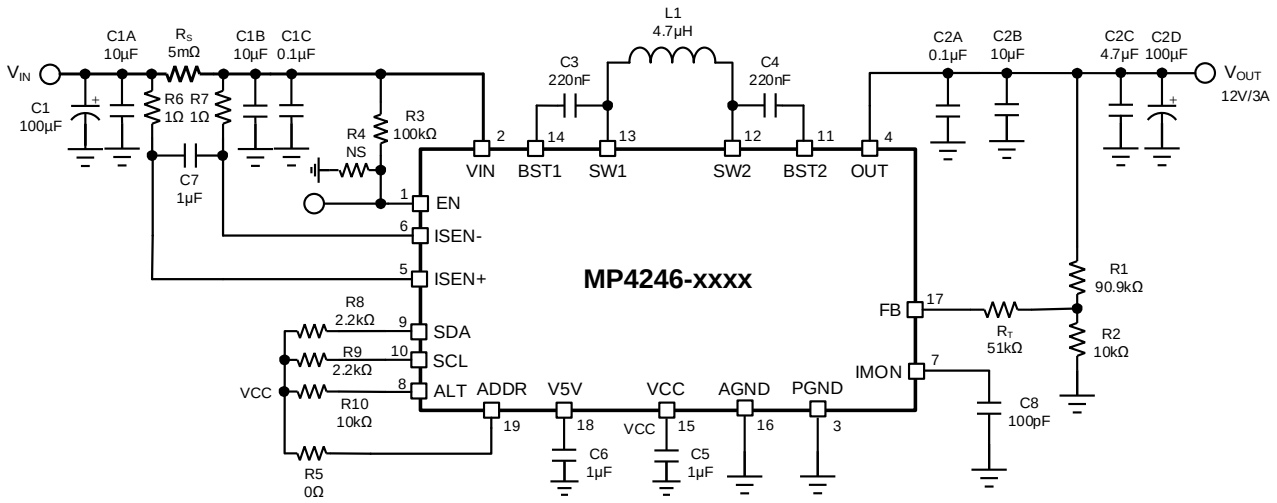


Figure 15: Typical Application Circuit (V_{IN} = 9V to 16V, V_{OUT} = 12V/3A application with R_S on the input side) (13) (14)

Notes:

13) ADDR sets the I²C address and I2C_EN status. I2C_EN is the logic or result of the OPERATION bit and ADDR pin status. When ADDR is connected to V_{CC}, I2C_EN is on. V_{OUT} starts up automatically when V_{IN} and V_{EN} exceed their respective UVLO thresholds. When ADDR is connected to AGND, I2C_EN is off. When V_{IN} and V_{EN} exceed their respective UVLO thresholds, V_{OUT} does not start up until the OPERATION bit is written to 1. For more details, see Table 1 on page 23.

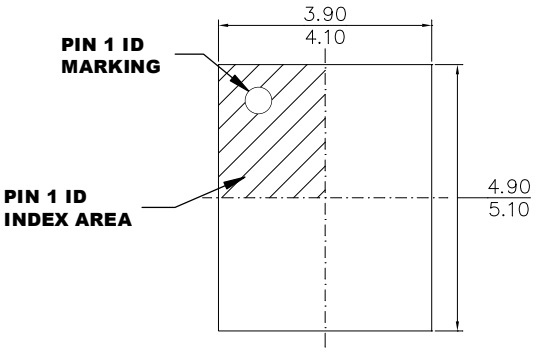
14) The V5V output is 5V and can supply the external MCU with a 60mA capability.

MP4246GVE-0000-Z CONFIGURATION

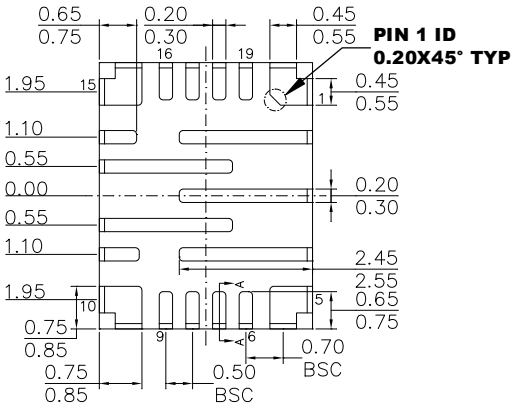
OTP Items	Description	Value
OPERATION bit	Configures the converter's operational state	0: Off (default)
Output voltage (V_{OUT})	V_{OUT} and reference voltage (V_{REF}) = 0.5V	5V (default)
Dither enable	Enables frequency spread spectrum (FSS) t	0: Disabled
FREQ bit	Sets f_{SW}	01: 420kHz (default)
Pulse-frequency modulation (PFM) or pulse-width modulation (PWM) mode	Automatic PFM/PWM or forced PWM mode	01: Forced PWM mode (default)
Output over-voltage protection (OVP) enable	Output OVP enable/disable	1: Enabled (default)
Output discharge enable	Output discharge function enable/disable during V_{IN}, I²C, and the EN off period	1: Enabled (default)
RSENS bit	Selects the sensing resistance (R_{SENS})	0: 5mΩ (default)
Line drop compensation enable	Line drop compensation enable/disable	0: Enables line drop compensation (default)
Current limit	Output current limit	5.4 (default)
Line drop compensation gain	Sets V_{OUT} compensation vs. load current	00: No compensation (default)
Switching current limit	Switch B (SWB) valley current limit and switch C (SWC) peak current limit	01: 13.5A SWC peak current limit, 9.6A SWB valley current
Adjusted current limit	Adjusts the constant current (CC) limit vs V_{OUT} gain	0: Does not add 50mA to the CC limit (default)
Rising slew rate	Sets the V_{REF} adjusted rising slew rate. V_{OUT} slew rate = V_{REF} slew rate x feedback ratio, where the feedback ratio is 10.	01: 0.16mV/µs (default)
Falling slew rate	Sets the V_{REF} adjusted falling slew rate. V_{OUT} slew rate = V_{REF} slew rate x feedback ratio, where the feedback ratio is 10.	10: 0.1mV/µs (default)
FREQ_MODE bit	Sets the frequency mode under buck-boost conditions	1: Maintains the same frequency as buck and boost mode
CC blank timer	Sets the blank time before the device enters CC mode	01: 2ms (default)
Hiccup enable	Enables or disables hiccup mode at the current limit	1: Enabled
Over-temperature warning (OTW)	Enables or disables OTW	135°C (default)
I²C address	Sets the I²C slave address	00111:07
V_{OUT} mask	Masks the ALT pin indication	1: Masked
Output current (I_{OUT}) or output current (P_{OUT}) mask		0: Not masked
Input voltage (V_{IN}) mask		1: Masked
Temperature mask		1: Masked
Power good (PG) status mask		11: The ALT pin does not indicate any PG edge changes
Reserved mask		0: Not masked
Unknown mask		1: Masked

PACKAGE INFORMATION

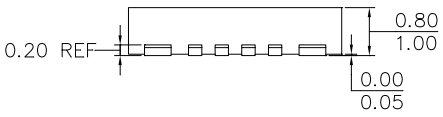
QFN-19 (4mmx5mm)



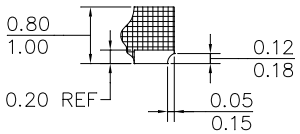
TOP VIEW



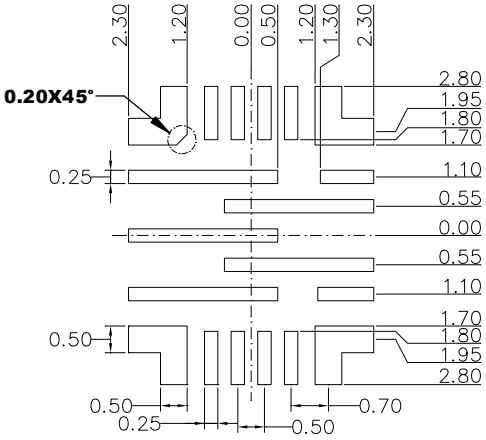
BOTTOM VIEW



SIDE VIEW



SECTION A-A

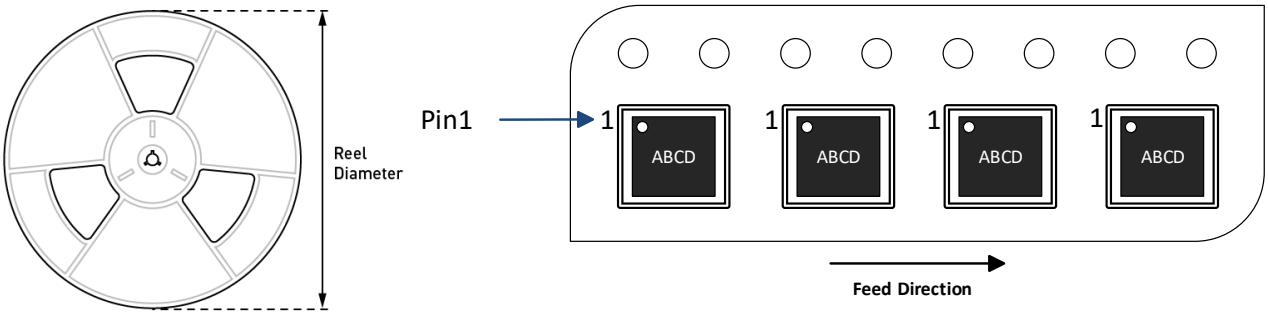


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4246GVE-0000-Z	QFN-19 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm
MP4246GVE-xxxx-Z	QFN-19 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/16/2024	Initial Release	-