



# MP24881

## 60V, 1.1A, Synchronous Step-Down LED Driver with PWM and Analog Dimming Function

### DESCRIPTION

The MP24881 is a 60V, monolithic, synchronous step-down LED driver with an integrated N-channel MOSFET and rectifier. It delivers up to 1.1A of continuous LED current ( $I_{LED}$ ) to high-power LEDs. The wide 10V to 60V input voltage ( $V_{IN}$ ) range accommodates a variety of step-down lighting applications. Hysteretic current mode minimizes the loop compensation design and achieves fast transient response, which makes the 25kHz pulse-width modulation (PWM) dimming frequency possible.

The MP24881 supports analog dimming with a PWM or analog signal input, which helps remove the flicker caused by the PWM frequency ( $f_{PWM}$ ). The separated PWM and analog dimming input port enables all PWM signal-controlled hybrid dimming. The hybrid dimming depth can reach as low as 0.1%.

Full protections include current-sense (CS) short protection, low-side (LS) reverse over-current protection (OCP), high-side (HS) OCP, and thermal shutdown.

The MP24881 is available in an SOIC-8EP package.

### FEATURES

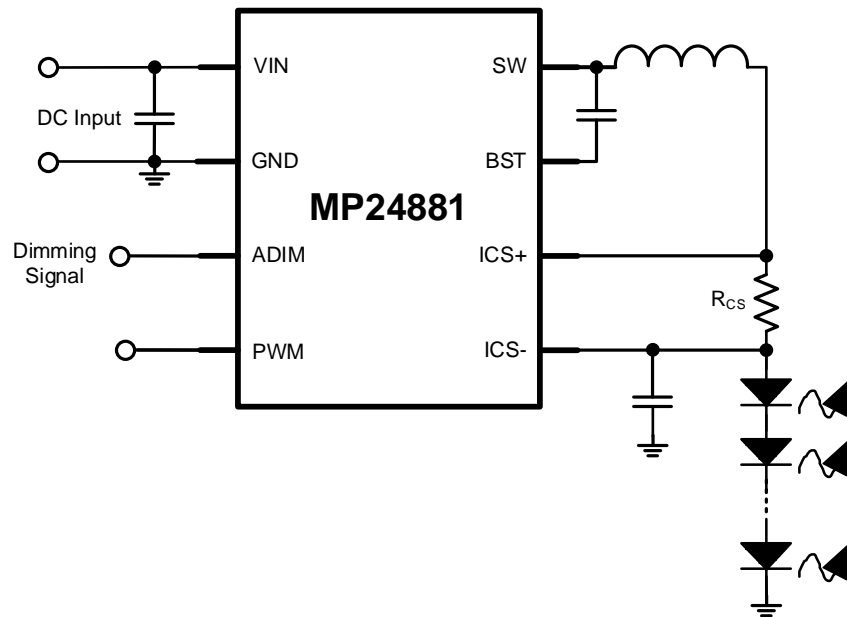
- Wide 10V to 60V Operating Input Voltage ( $V_{IN}$ ) Range
- Up to 1.1A of LED Current ( $I_{LED}$ )
- Synchronous Step-Down Converter
- Internal 100mΩ High-Side MOSFET (HS-FET)
- Internal 110mΩ Synchronous Rectifier (SR)
- Hysteretic Control
- Up to 2MHz Switching Frequency ( $f_{SW}$ )
- 100mV Reference Voltage ( $V_{REF}$ )
- LED Common Cathode Connection
- Excellent Pulse-Width Modulation (PWM) Dimming Performance:
  - Up to 25 kHz PWM Dimming Frequency
  - 20000:1 Wide Dimming Range
- Down to 0.1% Dimming Depth
- All PWM Signal-Controlled Hybrid Dimming
- High-Side (HS) Over-Current Protection (OCP)
- Current-Sense (CS) Short Protection
- Low-Side (LS) Reverse OCP
- Thermal Shutdown
- Available in an SOIC-8EP Package

### APPLICATIONS

- Landscape Lighting
- General LED Lighting

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## TYPICAL APPLICATION



## ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP24881GN	SOIC-8EP	See Below	2a

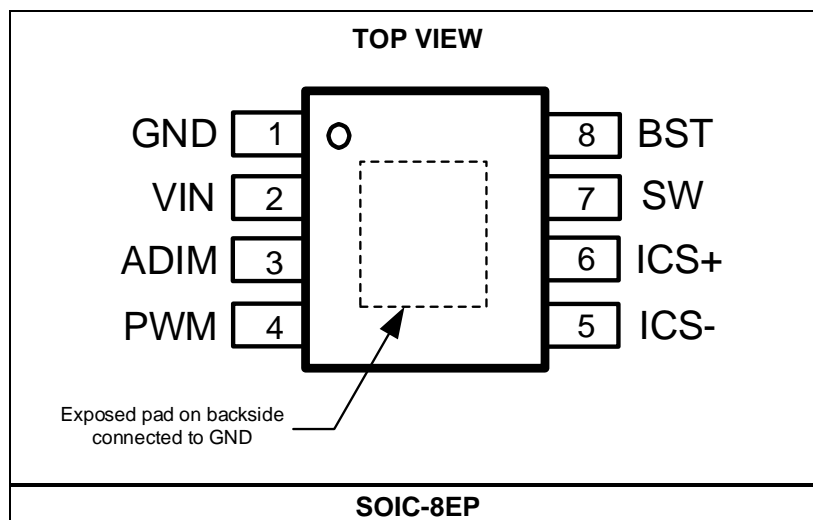
\* For Tape & Reel, add suffix -Z (e.g. MP24881GN-Z).

## TOP MARKING

**MP24881**  
**LLLLLLLL**  
**MPSYWW**

MPS: MPS prefix  
 Y: Year code  
 WW: Week code  
 MP24881: Part number  
 LLLLLLLL: Lot number

## PACKAGE REFERENCE



## PIN FUNCTIONS

Pin #	Name	Description
1	GND	<b>Power ground.</b> Electrically connect the GND pin to the system power ground plane using the shortest and lowest impedance possible.
2	VIN	<b>Power supply input.</b> The VIN pin supplies power to the converter and internal control circuitry. Connect VIN to a large bulk input capacitor to achieve a stable power source. It is recommended to connect a ceramic bypass capacitor between VIN and ground to minimize noise. Place the bypass capacitor as close to the chip as possible.
3	ADIM	<b>Analog dimming input.</b> Apply a 0.5V to 1.5V analog signal to the ADIM pin to enter analog dimming mode. The direct pulse-width modulation (PWM) signal input is also enabled. It is recommended to use a minimum 10kHz PWM signal frequency to improve the output current ripple ( $\Delta I_{OUT}$ ). The PWM signal amplitude must exceed the PWM input high threshold ( $V_{APWM\_H}$ ). If ADIM is pulled below 0.2V during its off delay time ( $t_{OFF\_DELAY\_ADIM}$ ), switching stops and the logic circuit shuts down except for the analog dimming-related functions. If analog dimming is not necessary, float ADIM.
4	PWM	<b>On/off control input and PWM dimming input.</b> Apply a 100Hz to 25kHz PWM signal to the PWM pin to enable PWM dimming. The PWM signal amplitude must exceed the PWM high threshold ( $V_{PWM\_H}$ ). If the PWM pin is pulled below the PWM low threshold ( $V_{PWM\_L}$ ) during the PWM off delay time ( $t_{OFF\_DELAY}$ ), switching stops and the logic circuit shuts down to reduce power loss.
5	ICS-	<b>Current-sense (CS) negative input.</b> The ICS- pin is one of the inputs to the internal high-side (HS) CS amplifier. Connect ICS- to the external sense resistor's negative side as well as the LED load and output capacitor ( $C_{OUT}$ ). To ensure sensing accuracy, connect $C_{OUT}$ to the sense resistor using the shortest wire.
6	ICS+	<b>CS positive input.</b> The ICS+ pin is one of the inputs to the internal HS CS amplifier. Connect ICS+ to the external sense resistor's positive side as well as one side of the external power inductor.
7	SW	<b>Power switch output.</b> Connect the SW pin to one side of the external power inductor.
8	BST	<b>Bootstrap for the high-side MOSFET (HS-FET) gate driver.</b> Connect a capacitor between the SW and BST pins to form a floating supply across the upper MOSFET driver.
-	Exposed pad	<b>Exposed pad.</b> Connect the exposed pad (EP) on the bottom to the ground plane to achieve optimal heat sinking and normal operation.

ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Input voltage ( $V_{IN}$ ) ..... -0.3V to +65V  
 SW voltage ( $V_{SW}$ ) ..... -0.3V to ( $V_{IN} + 0.3V$ )  
 BST voltage ( $V_{BST}$ ) ..... ( $V_{SW} - 0.3V$ ) to ( $V_{SW} + 6V$ )  
 ICS+ voltage ( $V_{ICS+}$ ), ICS- voltage ( $V_{ICS-}$ ) .....  
 ..... -0.3V to +65V  
 $V_{ICS+}$ ,  $V_{ICS-}$  ..... -0.3V to +6V  
 All other pins ..... -0.3V to +6V  
 Continuous power dissipation... ( $T_A = 25^\circ C$ ) <sup>(2)</sup>  
 SOIC-8EP ..... 2.5W  
 Junction temperature ( $T_J$ ) ..... 150°C  
 Lead temperature ..... 260°C  
 Storage temperature ..... -65°C to +150°C

## ESD Ratings

Human body model (HBM) (ICS+) ..... 1.2kV  
 HBM (all other pins) ..... 2kV  
 Charged-device model (CDM) ..... 2kV

Recommended Operating Conditions <sup>(3)</sup>

Supply voltage ( $V_{IN}$ ) ..... 10V to 60V  
 Operating junction temp ( $T_J$ ) ..... -40°C to +125°C

Thermal Resistance <sup>(4)</sup>  $\theta_{JA}$   $\theta_{JC}$ 

SOIC-8EP ..... 50 ..... 10... °C/W

## Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_J$  (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) = ( $T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can cause excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on a Resolved JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

Typical values are at  $V_{IN} = 24V$ ,  $T_J = 25^{\circ}C$ , all voltages with respect to ground. Minimum and maximum values are at  $V_{IN} = 24V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Input Supply Voltage</b>						
Input voltage operating range	$V_{IN}$		5.7		60	V
$V_{IN}$ under-voltage lockout (UVLO) threshold	$V_{IN\_UVLO}$	$V_{IN}$ falling	5.2	5.45	5.7	V
$V_{IN}$ UVLO hysteresis	$V_{IN\_UVLO\_HYS}$		120	175	240	mV
<b>Input Supply Current</b>						
Shutdown current	$I_{IN\_SD}$	$V_{PWM} = 0V$			90	$\mu A$
Quiescent current (normal)	$I_{IN\_Q\_NOR}$	No switching		1.33	1.6	mA
Operating current	$I_{IN}$	$f_{SW} = 2MHz$		50		mA
<b>Enable (EN) and Pulse-Width Modulation (PWM) Dimming</b>						
PWM high threshold	$V_{PWM\_H}$	$V_{PWM}$ rising	1.14	1.3	1.36	V
PWM low threshold	$V_{PWM\_L}$	$V_{PWM}$ falling	0.96	1	1.12	V
PWM pull-up current <sup>(5)</sup>	$I_{PWM}$	$V_{PWM} = 0V$		30		$\mu A$
PWM off delay time	$t_{OFF\_DELAY}$		10	16	22	ms
<b>Analog Dimming</b>						
Analog dimming input threshold <sup>(5)</sup>	$V_{ADIM}$	Start-up mode changes		3		V
Analog dimming input hysteresis <sup>(5)</sup>	$V_{ADIM\_HYS}$			0.5		V
Analog dimming high threshold	$V_{ADIM\_H}$	$T_J = 25^{\circ}C$	1.48	1.5	1.52	V
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$	1.47	1.5	1.53	V
Analog dimming low Threshold	$V_{ADIM\_L}$	$T_J = 25^{\circ}C$	0.493	0.5	0.507	V
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$	0.478	0.5	0.529	V
Analog dimming shutdown threshold	$V_{ADIM\_SD}$		0.175	0.21	0.24	V
PWM input high threshold	$V_{APWM\_H}$		1.52	1.6	1.68	V
PWM input low threshold	$V_{APWM\_L}$		0.37	0.4	0.45	V
ADIM off delay time	$t_{OFF\_DELAY\_ADIM}$		10	16	22	ms
Analog pull-up current <sup>(5)</sup>	$I_{ADIM}$	$V_{ADIM} = 0V$		30		$\mu A$
<b>Bootstrap (BST)</b>						
Bias voltage for high-side (HS) driver	$V_{BST} - V_{SW}$	$6V \leq V_{IN} \leq 60V$	4.85	5.2	5.55	V
		$V_{IN} = V_{IN\_UVLO} + 50mV$	3.6			V
BST operating current	$I_{BST}$	No switching	15	20	26	$\mu A$
BST UVLO	$V_{BST\_UVLO}$	$V_{BST} - V_{SW}$ falling edge	2.7	3	3.3	V
BST UVLO hysteresis	$V_{BST\_UVLO\_HYS}$			180		mV

## ELECTRICAL CHARACTERISTICS (continued)

Typical values are at  $V_{IN} = 24V$ ,  $T_J = 25^{\circ}C$ , all voltages with respect to ground. Minimum and maximum values are at  $V_{IN} = 24V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>High-Side MOSFET (HS-FET) and Low-Side MOSFET (LS-FET)</b>						
HS-FET on resistance	$R_{DS(ON)_{HS}}$	$T_J = 25^{\circ}C$		100	130	m $\Omega$
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$		100	170	m $\Omega$
LS-FET on resistance	$R_{DS(ON)_{LS}}$	$T_J = 25^{\circ}C$		110	145	m $\Omega$
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$		110	190	m $\Omega$
Switch leakage current	$I_{SW\_LKG}$	$V_{IN} = 60V$ , $V_{SW} = 0V$	-1		+1	$\mu A$
Zero-current detection (ZCD) threshold (turns off the sync switch) <sup>(5)</sup>	$I_{ZCD}$	When the sync rectifier is on		50		mA
HS to low-side (LS) dead time <sup>(5)</sup>	$t_{DT\_HL}$	HS-FET off to LS-FET on		20		ns
LS to HS dead time <sup>(5)</sup>	$t_{DT\_LH}$	LS-FET off to HS-FET on		20		ns
<b>LED Current Regulation</b>						
Sense voltage high threshold	$V_{ICS\_H}$	$V_{ICS+} - -V_{ICS-}$ rising	110	115	120	mV
Sense voltage low threshold	$V_{ICS\_L}$	$V_{ICS+} - -V_{ICS-}$ falling	81	85	89	mV
Average sense voltage	$V_{ICS}$	$(V_{ICS+} - -V_{ICS-}) / 2$ , $T_J = 25^{\circ}C$	97.5	100	102.5	mV
		$(V_{ICS+} - -V_{ICS-}) / 2$ , $T_J = -40^{\circ}C$ to $+125^{\circ}C$	96.5	100	103.5	mV
Current-sense (CS) gain	$G_{CS}$	$V_{IN} = 45V$ , $T_J = 25^{\circ}C$	9.85	10	10.15	
HS-FET maximum on time <sup>(5)</sup>	$t_{ON\_MAX\_H}$			40		$\mu s$
HS-FET minimum on time <sup>(5)</sup>	$t_{ON\_MIN\_H}$			40		ns
Sense voltage high propagation delay <sup>(5)</sup>	$t_{PD\_H}$	$V_{ICS+} - -V_{ICS-}$ rising to reach $V_{ICS\_H}$ and SW falling		55		ns
Sense voltage low propagation delay <sup>(5)</sup>	$t_{PD\_L}$	$V_{ICS+} - -V_{ICS-}$ falling to reach $V_{ICS\_L}$ and SW rising		55		ns
<b>Over-Current Protection (OCP)</b>						
HS OCP threshold	$I_{OCP\_H}$	$V_{ICS+} - -V_{ICS-} = 80mV$	3	3.5	4	A
OCP sense voltage threshold	$V_{ICS\_OCP}$	$V_{ICS+} - -V_{ICS-}$ falling	34	47	59	mV
CS short-circuit protection (SCP) threshold	$I_{SCP\_CS}$	$V_{ICS+} - -V_{ICS-} = 30mV$	1.5	1.75	2.5	A
Hiccup time for OCP and CS shorts <sup>(5)</sup>	$t_{HICCUP}$			16		ms
LS reverse OCP threshold during BST charge	$I_{OCP\_LB\_BST}$		-0.42	-0.3	-0.2	A
LS reverse OCP threshold during switching	$I_{OCP\_LB\_SW}$		-0.67	-0.45	-0.35	A
Hiccup time for LS reverse OCP <sup>(5)</sup>	$t_{HICCUP\_LB}$			420		$\mu s$
Leading edge blanking time <sup>(5)</sup>	$t_{LEB}$	For peak current limit and OCP		50		ns

## ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are  $V_{IN} = 24V$ ,  $T_J = 25^{\circ}C$ , all voltages with respect to ground. Minimum and maximum values are at  $V_{IN} = 24V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Thermal Shutdown</b>						
Thermal shutdown threshold <sup>(5)</sup>	$T_{SD}$	$T_J$ rising		160		$^{\circ}C$
Thermal shutdown hysteresis <sup>(5)</sup>	$T_{HYS}$			30		$^{\circ}C$

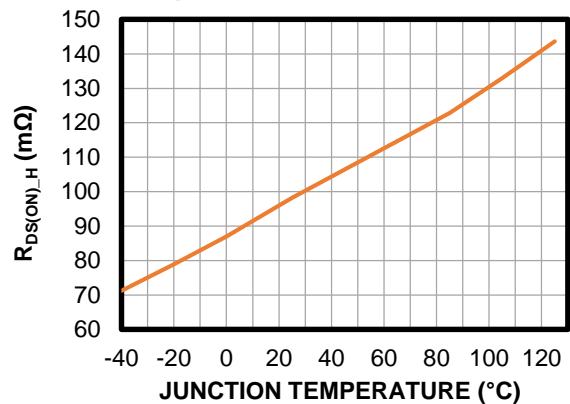
**Note:**

5) Guaranteed by design.

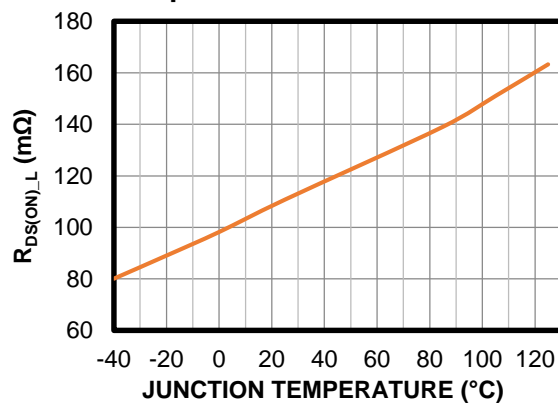
## TYPICAL CHARACTERISTICS

$V_{IN} = 24V$ , unless otherwise noted.

**HS-FET On Resistance vs. Temperature**

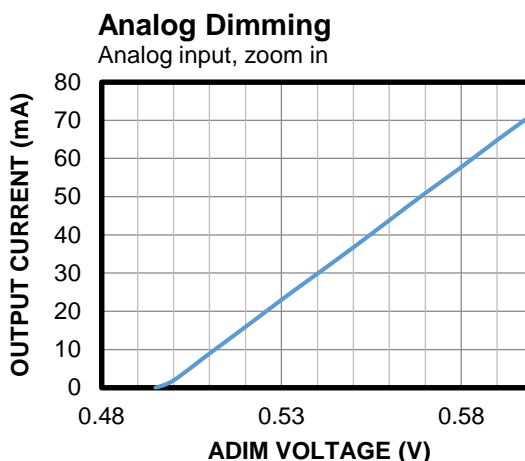
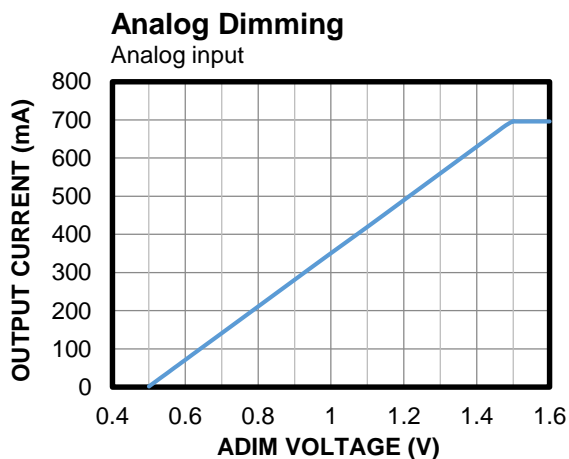
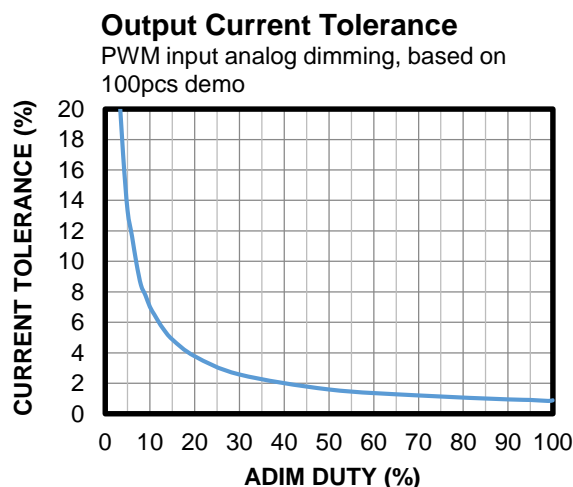
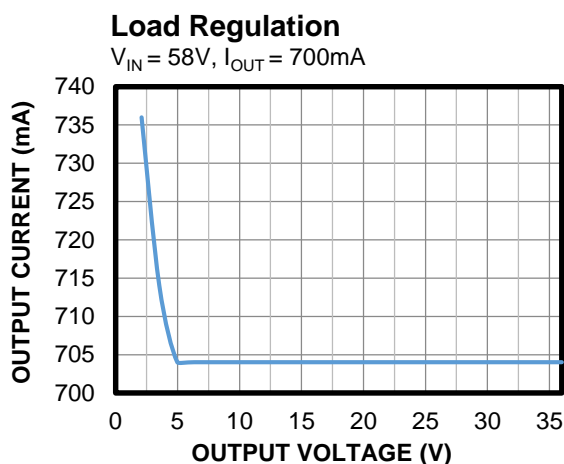
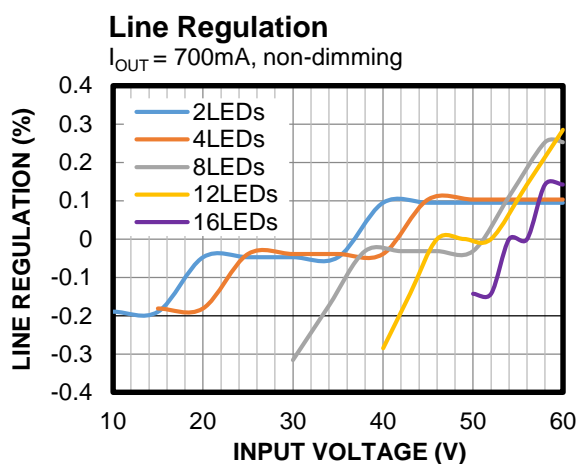
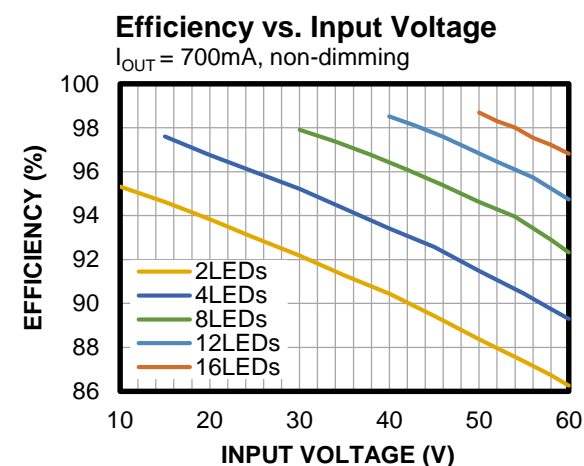


**LS-FET On Resistance vs. Temperature**



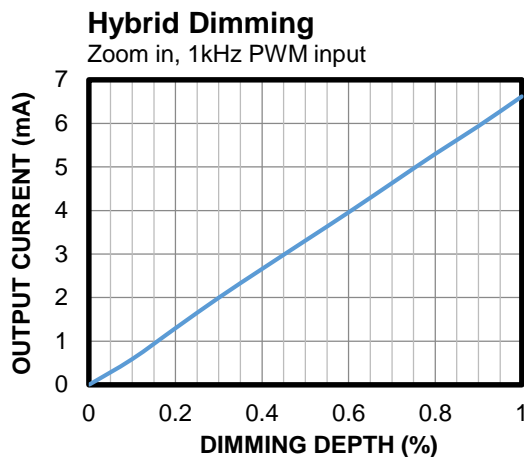
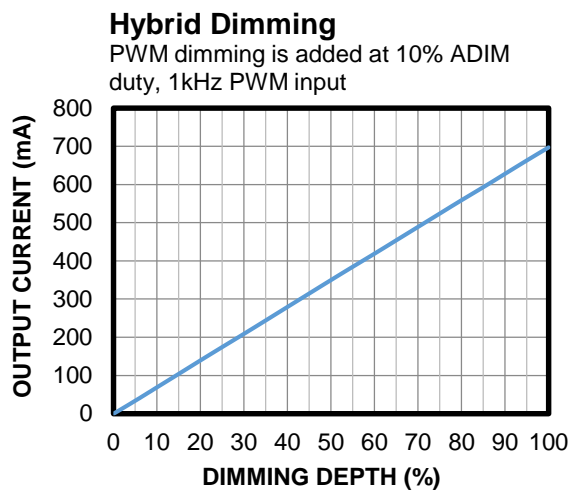
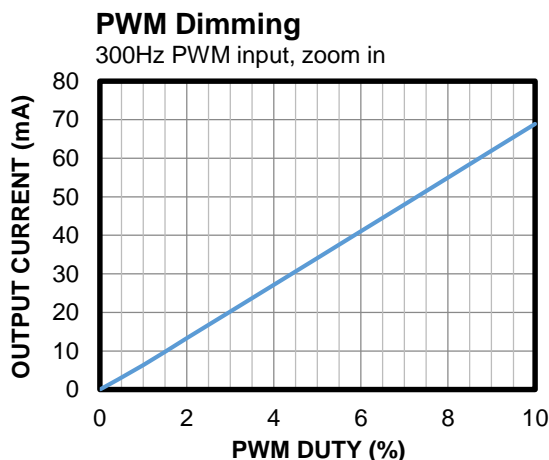
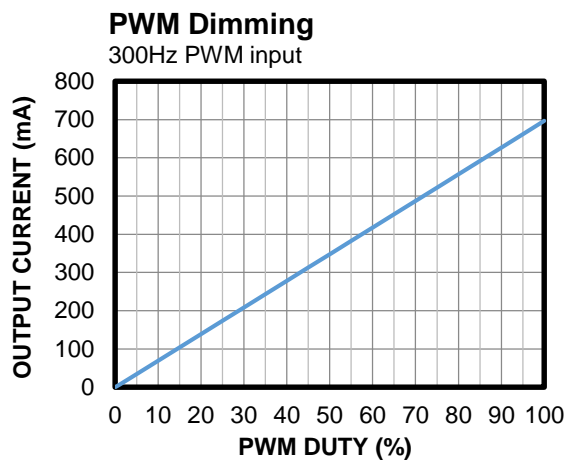
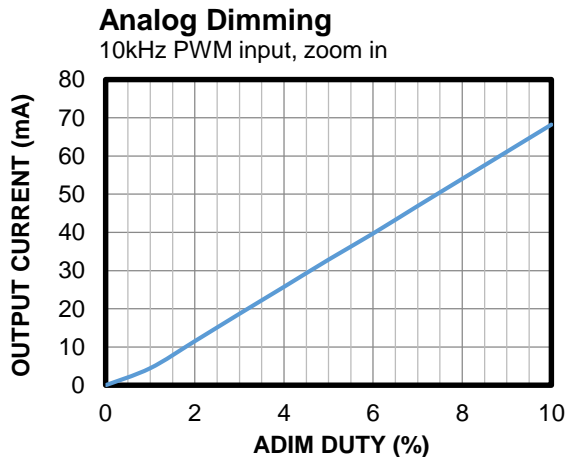
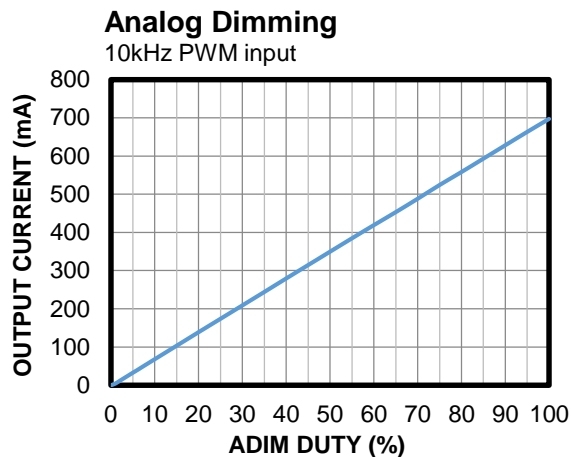
# TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board.  $V_{IN} = 56V$ ,  $I_{OUT} = 1A$ ,  $L = 100\mu H$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.



# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.  $V_{IN} = 56V$ ,  $I_{OUT} = 1A$ ,  $L = 100\mu H$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

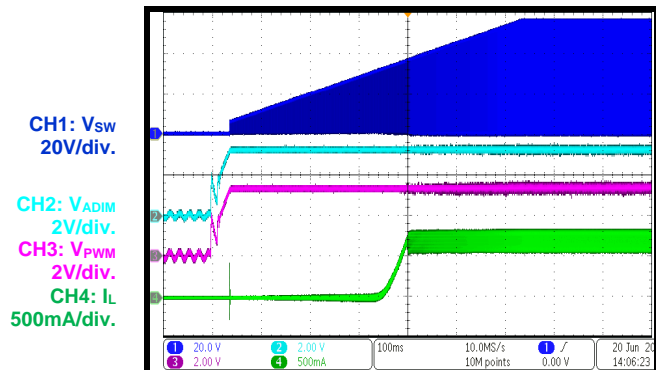


# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.  $V_{IN} = 56V$ ,  $I_{OUT} = 1A$ ,  $L = 100\mu H$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

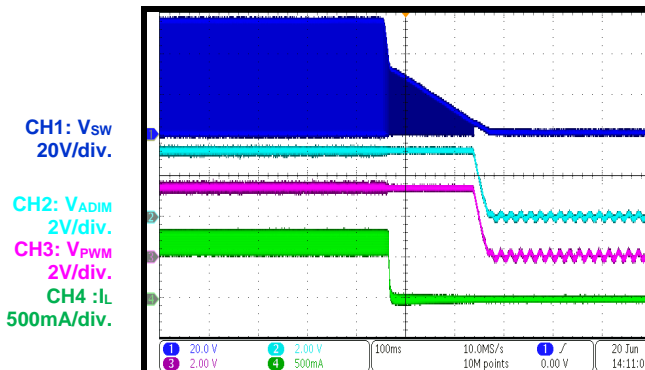
## Start-Up through VIN

Float ADIM and PWM



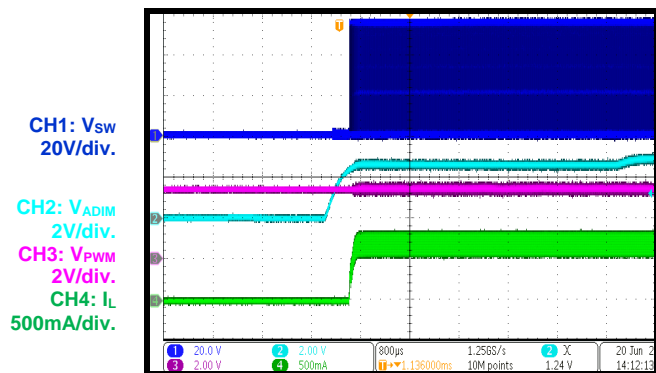
## Shutdown through VIN

Float ADIM and PWM



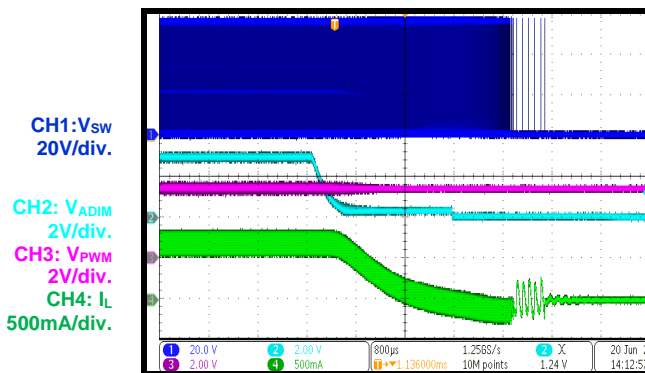
## Start-Up through ADIM

Float PWM



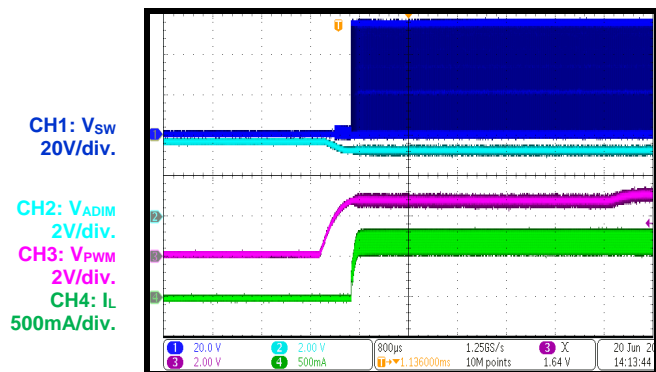
## Shutdown through ADIM

Float PWM



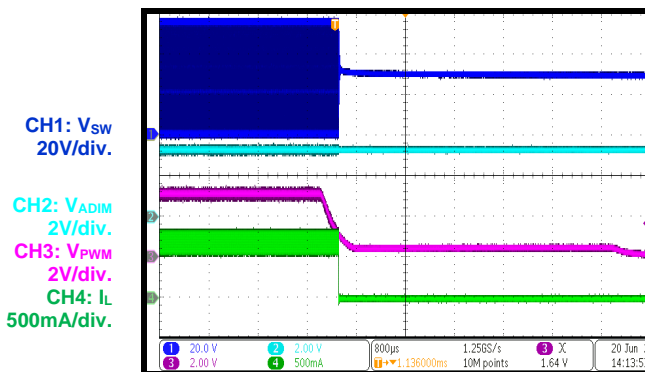
## Start-Up through PWM

Float ADIM



## Shutdown through PWM

Float ADIM

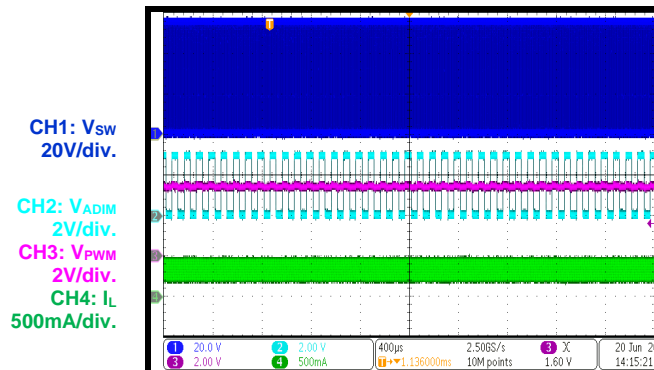


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.  $V_{IN} = 56V$ ,  $I_{OUT} = 1A$ ,  $L = 100\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

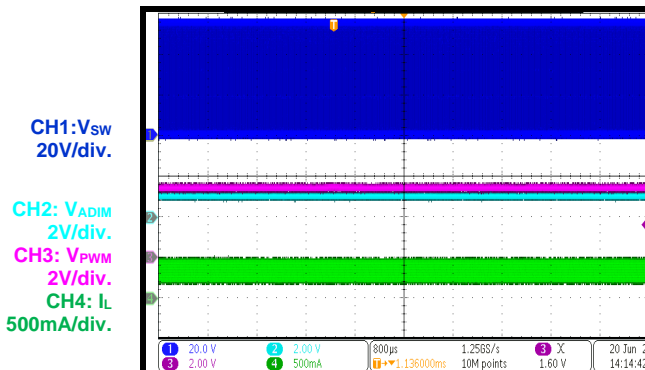
### Analog Dimming

ADIM duty = 50% at 10kHz



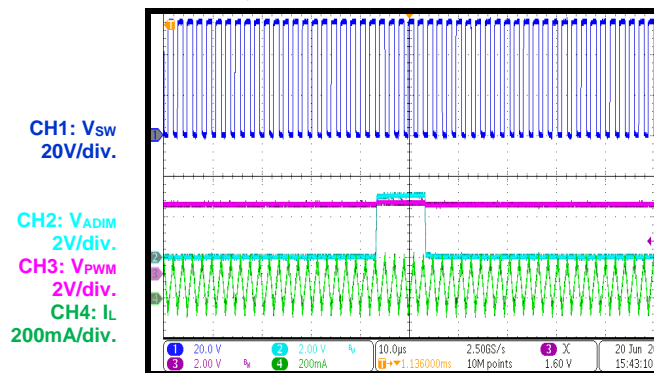
### Analog Dimming

$V_{ADIM} = 1V$



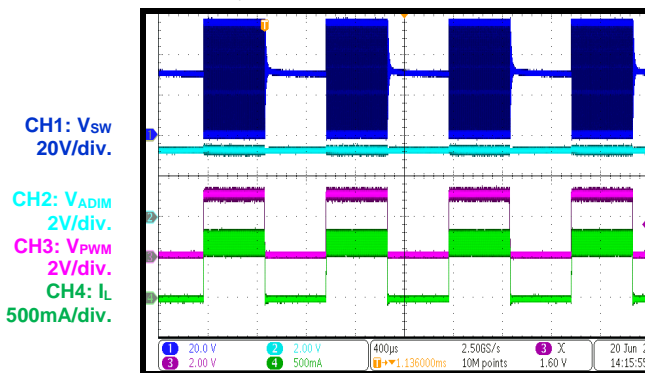
### Analog Dimming

ADIM duty = 10% at 10kHz



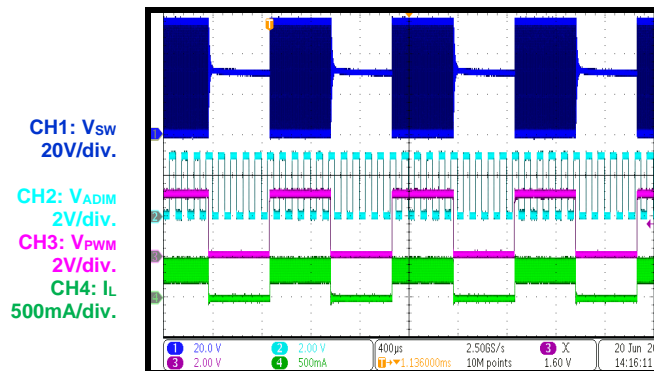
### PWM Dimming

PWM duty = 50% at 1kHz



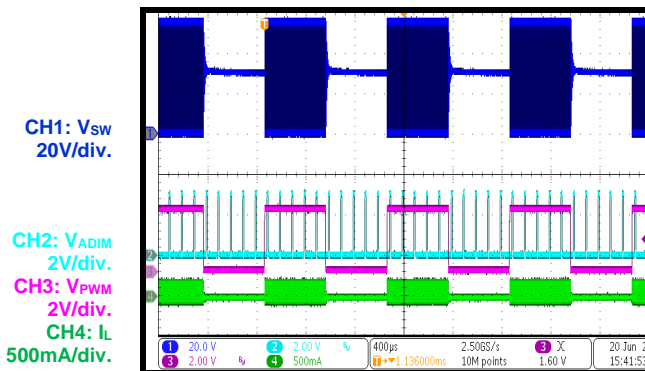
### Hybrid Dimming

ADIM duty = 50% at 10kHz, PWM duty = 50% at 1kHz



### Hybrid Dimming

ADIM duty = 10% at 10kHz, PWM duty = 50% at 1kHz

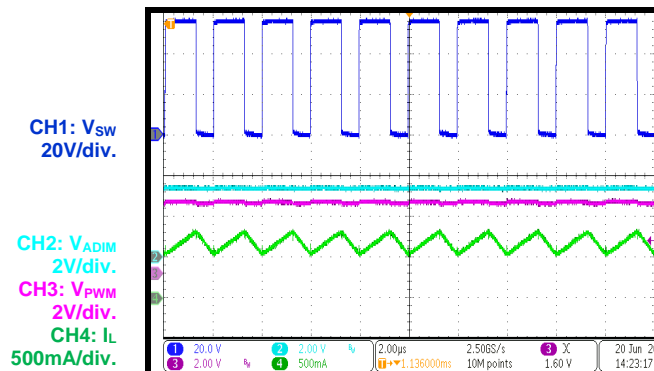


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.  $V_{IN} = 56V$ ,  $I_{OUT} = 1A$ ,  $L = 100\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

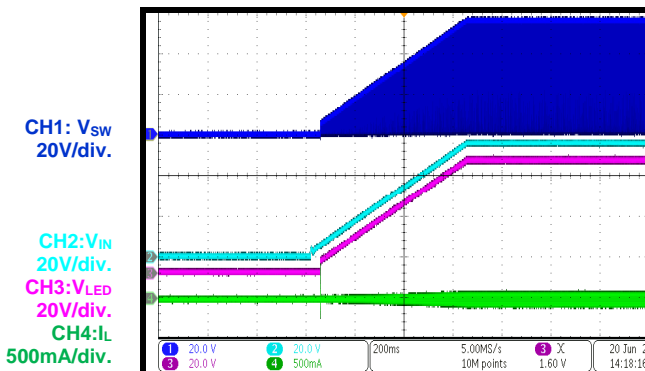
### Steady State

Float ADIM and PWM



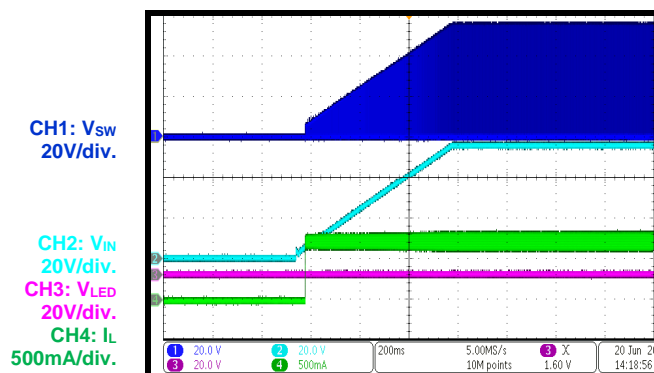
### Open LED Before Start-Up through $V_{IN}$

Float ADIM and PWM



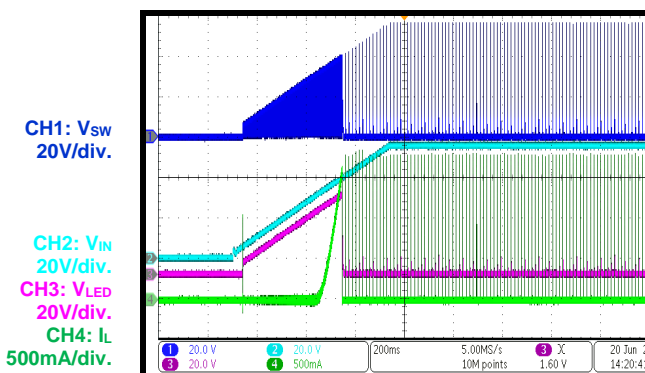
### Short LED Before Start-Up through $V_{IN}$

Float ADIM and PWM



### Short $R_{CS}$ Before Start-Up through $V_{IN}$

Float ADIM and PWM



## FUNCTIONAL BLOCK DIAGRAM

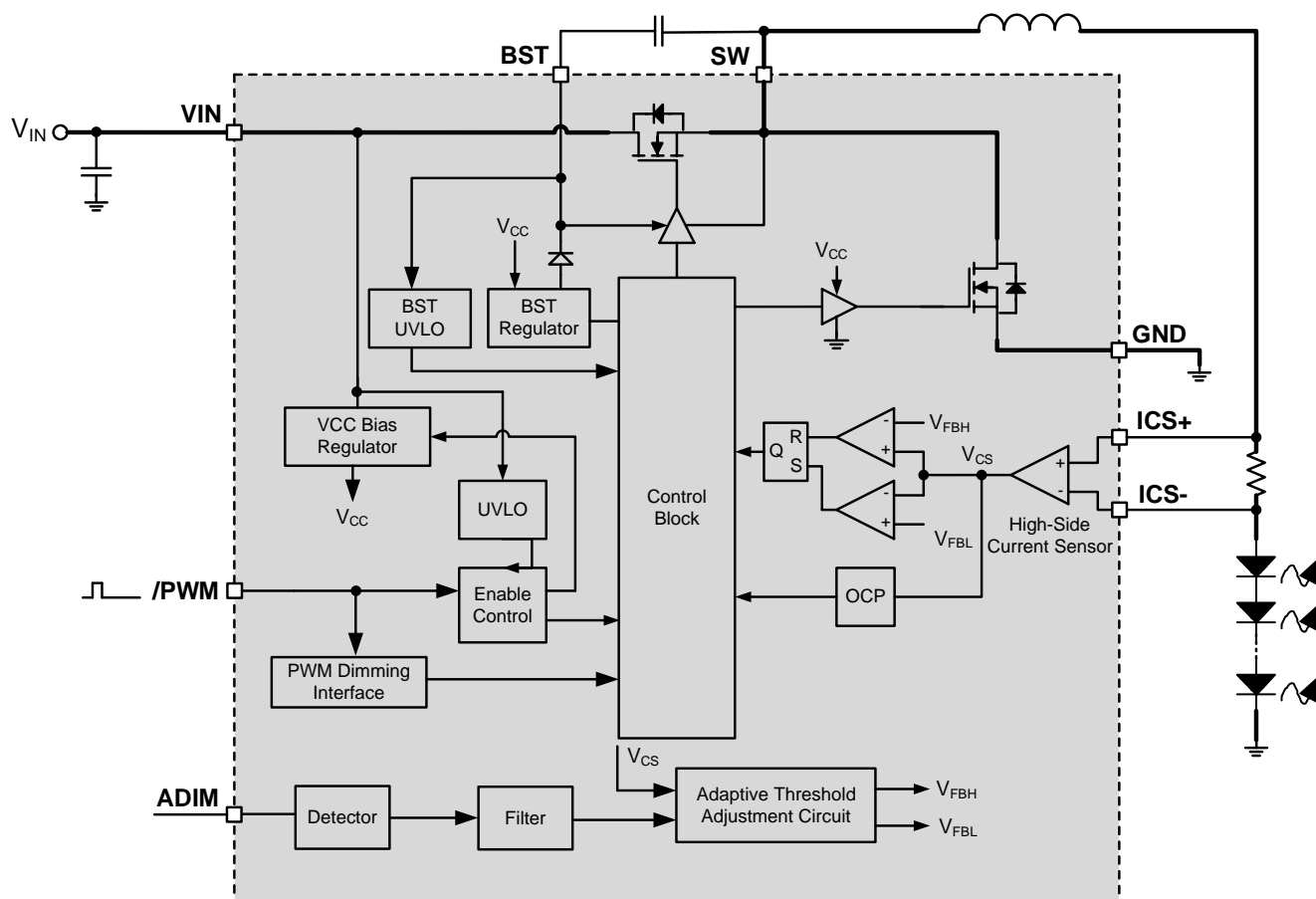


Figure 1: Functional Block Diagram

## OPERATION

The MP24881 is a 60V, 1.1A, fully integrated, synchronous step-down LED driver. The device operates as a stable current source to deliver up to 1.1A of continuous LED current ( $I_{LED}$ ) to the LED string. The MP24881 provides pulse-width modulation (PWM) dimming, analog dimming, and analog dimming with a PWM input, and hybrid dimming, using a deep dimming ratio. For hybrid dimming, the dimming ratio can reach 0.1%.

### Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) prevents the chip or certain blocks from operating at an insufficient supply voltage. The MP24881 incorporates two internal fixed UVLO comparators for monitoring the  $V_{IN}$  and BST pins.

Once the input voltage ( $V_{IN}$ ) drops below its UVLO threshold, the chip is disabled. If  $V_{IN}$  drops below the  $V_{IN}$  UVLO threshold ( $V_{IN\_UVLO}$ ), all switching remains disabled until  $V_{IN}$  exceeds the sum of  $V_{IN\_UVLO}$  and the  $V_{IN}$  UVLO hysteresis threshold ( $V_{IN\_UVLO\_HYS}$ ).

At the bootstrap (BST) UVLO threshold ( $V_{BST\_UVLO}$ ), there is no adequate driving capacity for the LED driver's high-side MOSFET (HS-FET). The HS-FETs stop switching, and the device initiates the pre-charge period again. The BST charger conducts the low-side MOSFETs (LS-FETs) to attempt to charge up the BST voltage ( $V_{BST}$ ). The LED driver starts up again once  $V_{BST}$  exceeds the sum of  $V_{BST\_UVLO}$  and the BST UVLO hysteresis threshold ( $V_{BST\_UVLO\_HYS}$ ).

### Start-Up

If  $V_{IN}$  exceeds the sum of  $V_{IN\_UVLO}$  and  $V_{IN\_UVLO\_HYS}$ , the MP24881 starts up. Before entering normal operation, the device must implement the pre-charge. Once the power supplies are ready, the LED driver begins switching. If PWM dimming is applied, the device's operation follows the corresponding PWM control signals. If analog dimming is applied, the device's operation follows the corresponding analog signal.

### Hysteretic Current Control with Adaptive Threshold Adjustment

The MP24881 is a synchronous step-down LED driver that operates in hysteretic current control mode to accurately regulate  $I_{LED}$ .

Hysteretic current control minimizes the loop compensation design and achieves fast transient response, making it ideal for fast PWM dimming performance.

During normal operation, the ICS+ and ICS- pins monitor the  $I_{LED}$  sensed voltage across the sensing resistor. The HS-FET turns on and remains on until the difference between the ICS+ voltage ( $V_{ICS+}$ ) and the ICS- voltage ( $V_{ICS-}$ ) reaches the high threshold. Then the HS-FET turns off and the low-side (LS) sync rectifier switches on to conduct the inductor current ( $I_L$ ) until the difference between  $V_{ICS+}$  and  $V_{ICS-}$  drops below the low threshold.

The two thresholds are adaptively adjusted to compensate for all the circuit delays, resulting in accurate  $I_{LED}$  regulation, with an average 100mV reference voltage ( $V_{REF}$ ) between ICS+ and ICS-.

### Bootstrap (BST)

The BST circuitry is required to drive the LED driver's high-side (HS) N-channel MOSFET. The external flying capacitor is charged to maintain a sufficient driving voltage above the SW voltage ( $V_{SW}$ ) via the internal BST regulator.

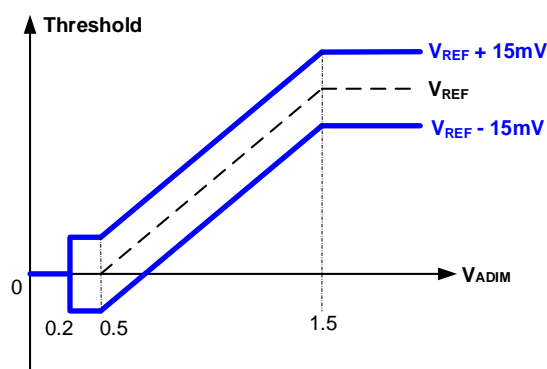
During start-up, the BST pre-charge process starts before the converter is ready to operate. The sync low-side MOSFET (LS-FET) turns on to force SW low, and the BST regulator charges the flying capacitor via the BST pin. The LS-FET turns off after a short interval, then turns on and off several times based on the set duty cycle before building up sufficient driving voltage across the flying capacitor. The short interval limits the reverse current from the discharging output capacitor.

Additional external circuitry can also be implemented to ensure  $V_{BST}$  remains within the normal operating range.

## Analog Dimming

The MP24881 supports PWM dimming, analog dimming, and analog dimming with a PWM signal input, and hybrid dimming.

Apply a DC signal to the ADIM pin to enable analog dimming.  $I_{OUT}$  drops from 100% to 0% when ADIM changes from the analog dimming high threshold ( $V_{ADIM\_H}$ ) to the analog dimming low threshold ( $V_{ADIM\_L}$ ). Figure 2 shows the high and low thresholds of the sensed voltage under dimming conditions.



**Figure 2: High and Low Thresholds of the Sensed Voltage under Analog Dimming Conditions**

The direct PWM signal input can also be enabled. It is recommended to use a minimum 10kHz PWM signal frequency to suppress the output current ripple ( $\Delta I_{OUT}$ ). The PWM signal amplitude must exceed the PWM input high threshold ( $V_{APWM\_H}$ ). If the ADIM pin is pulled below the analog dimming shutdown threshold ( $V_{ADIM\_SD}$ ) and lasts for its off delay time ( $t_{OFF\_DELAY\_ADIM}$ ), then switching stops and the logic circuit shuts down except for the analog dimming-related function. If the analog dimming function is not required, float ADIM. It is recommended to use a 100pF ceramic capacitor for noise suppression.

It is recommended to use a 3% minimum analog dimming depth to achieve improved dimming performance.

## Pulse-Width Modulation (PWM) Dimming

Apply a 100Hz to 25kHz PWM signal to the PWM pin to enable PWM dimming. The PWM signal amplitude must exceed the PWM high threshold ( $V_{PWM\_H}$ ). If the PWM pin is pulled below the PWM low threshold ( $V_{PWM\_L}$ ) and lasts for the PWM off delay time ( $t_{OFF\_DELAY}$ ),

then switching stops and the logic circuit shuts down to reduce power loss.

## Hybrid Dimming

To enable hybrid dimming, apply a PWM signal to the PWM pin, and apply a PWM or analog signal to the ADIM pin. The hybrid dimming depth can reach as low as 1%.

It is recommended to apply a PWM or DC signal at the ADIM pin to achieve analog dimming from 100% to 10%. Maintain a stable ADIM signal, and apply a PWM signal at the PWM pin from 100% to the requested depth. The total dimming depth is  $0.1 \times \text{PWM duty}$ . The duty of the minimum PWM signal that is applied to the PWM pin must not drop below 1% under this condition.

If an analog dimming depth deeper than 10% is required for hybrid dimming, analog dimming can reach as low as 3%. When the PWM signal is applied to the PWM pin, the duty of this PWM signal must not drop below 2%.

## High-Side MOSFET (HS-FET) Over-Current Protection (OCP)

Under normal conditions, the switching current is regulated by the reference high and low thresholds. The HS-FET turns off after reaching the high threshold. If the sense resistor fails or a smaller, improper sense resistor is used, the peak current is exceedingly high before reaching the reference HS threshold. A HS over-current protection (OCP) shuts down the MP24881 immediately. The device attempts operation again after the hiccup time for OCP and CS shorts ( $t_{HICCU}$ ) completes.

## Current-Sense (CS) Short-Circuit Protection (SCP)

$I_{LED}$  is consistently regulated even when the LED string is shorted. If the sensing resistor is shorted or the resistor and LED load are shorted together without any protections, then the output current ( $I_{OUT}$ ) may be large enough to damage the chip. In this scenario, whenever the HS-FET current exceeds the current-sense (CS) short-circuit protection (SCP) threshold ( $I_{SCP\_CS}$ ), and the CS voltage ( $V_{ICS+} - V_{ICS-}$ ) drops below the OCP sense voltage threshold ( $V_{ICS\_OCP}$ ), CS SCP is triggered and the MP24881 shuts down

immediately. The device initiates operation again after  $t_{\text{HICCUP}}$  completes.

#### **Low-Side MOSFET (LS-FET) Reverse Over-Current Protection (OCP)**

When the LS-FET turns on, if the LS-FET reverse current between SW and GND exceeds the LS reverse OCP threshold, then the MP24881 shuts down immediately. The device attempts operation again after the hiccup time for LS reverse OCP ( $t_{\text{HICCUP\_LB}}$ ) completes. The reverse OCP threshold during BST charge and stable operation are not the same. The LS reverse OCP threshold during BST charge and the LS reverse OCP threshold during switching protect the MP24881 from any uncontrollable and unsafe states. A smaller inductance results in greater overshoot current, which is introduced by the internal propagation delay. The inductance must not drop below 100 $\mu$ H;

otherwise, reverse OCP may be triggered under steady-state conditions or during start-up.

#### **Output Open Load**

The MP24881 does not require output open-load protection as a step-down current regulator. If the output of the LED driver is open, the output voltage ( $V_{\text{OUT}}$ ) rises as high as  $V_{\text{IN}}$ .

#### **Thermal Protection**

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds the thermal shutdown threshold ( $T_{\text{SD}}$ ), the over-temperature (OT) fault shuts down the entire device. Thermal shutdown protection is automatically recoverable. Once the die temperature drops below its lower threshold ( $T_{\text{SD}} - T_{\text{HYS}}$ ), the device starts up again.

## APPLICATION INFORMATION

### Selecting the LED Current-Sense Resistor

$I_{LED}$  is set via a sensing resistor ( $R_{CS}$ ) that is connected between the ICS+ and ICS- pins. The mean voltage on  $R_{CS}$  is equivalent to  $V_{FB}$ .  $R_{CS}$  can be calculated with Equation (1):

$$R_{CS} = \frac{V_{FB}}{I_{OUT}} = \frac{100mV}{I_{OUT}} \quad (1)$$

For example, if  $I_{LED} = 1A$ , then  $R_{CS} = 100m\Omega$ .

### Inductor Selection and Setting the Frequency

An inductor ( $L$ ) is required to supply a constant current to the LED. The minimum  $L$  is  $100\mu H$  (see the Low-Side MOSFET (LS-FET) Reverse Over-Current Protection (OCP) section on page 17).  $L$  is related to the switching frequency ( $f_{SW}$ ) and can be calculated with Equation (2):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times 30\% \times I_{OUT} \times V_{IN}} \quad (2)$$

Where  $V_{OUT}$  is the output voltage that drives the LEDs.

A smaller value inductance results in higher  $f_{SW}$ , while the highest frequency is limited by the internal propagation delay and the HS-FET minimum on time ( $t_{ON\_MIN\_H}$ ). The internal propagation delay can also make it difficult to accurately calculate  $L$ .

The peak inductor current ( $I_{PEAK}$ ) can be calculated with Equation (3):

$$I_{PEAK} = (1 + 15\%) \times I_{OUT} \quad (3)$$

Choose an inductor with a nominal DC current rating at least 25% greater than the maximum load current for most applications. For the highest efficiency, the inductor's DC resistance should be less than  $100m\Omega$ .

### Selecting the Input Capacitor

The step-down converter has a discontinuous input current ( $I_{IN}$ ) and requires a capacitor to supply AC current to the converter while maintaining the DC  $V_{IN}$ . Use low-ESR capacitors for the best performance, especially for high  $f_{SW}$  applications.

The RMS current in the input capacitor ( $C_{IN}$ ) ( $I_D$ ) can be calculated with Equation (4):

$$I_D = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}}} \quad (4)$$

With low-ESR capacitors, the input voltage ripple ( $\Delta V_{IN}$ ) can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Choose  $C_{IN}$  with a sufficient RMS current rating and capacitance to achieve a small  $\Delta V_{IN}$ . When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.  $0.1\mu F$ ) as close to the IC as possible.

### Selecting the Output Capacitor

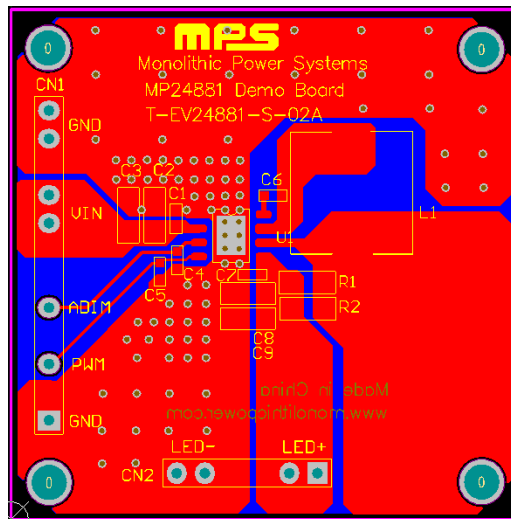
The output capacitor ( $C_{OUT}$ ) maintains small  $\Delta I_{OUT}$  and ensures feedback loop stability.  $C_{OUT}$  is required to support negative current under deep analog dimming, start-up, or shutdown conditions. In addition,  $C_{OUT}$  can achieve stable  $V_{OUT}$  to ensure a clean current sample.  $C_{OUT}$  impedance must be low at  $f_{SW}$ . Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR characteristics. For most applications, a  $2.2\mu F$  ceramic capacitor is sufficient. For applications below 5V, a larger  $C_{OUT}$  is required to ensure that  $\Delta V_{OUT}$  is below 0.5V.

## PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to significantly reduce the voltage spike on the SW node and EMI noise levels. For the best results, refer to Figure 3 and follow the guidelines below:

1. Place the input decoupling capacitor as close to VIN, SW, and GND as possible, using short and wide traces.
2. A ceramic capacitor (0603) is recommended to further shorten the VIN-to-GND loop, which suppresses switching spike voltages.
3. Keep the switch node traces short and away from the feedback network.
4. Place the external current sampling resistors next to ICS+ and ICS-.
5. Place the output capacitor as close to the external current sampling resistors as possible to achieve accurate current sense.
6. To improve thermal conduction, a thermal via grid can be created immediately beneath the exposed pad.

7. It is recommended to use a small barrel diameter (e.g. 15mil) to ensure that the hole is filled up during the plating process, which supports conduction to the other side. If the barrel diameter is too large, solder wicking issues can occur during the reflow soldering process.



**Figure 3: Recommended PCB Layout**

## TYPICAL APPLICATION CIRCUIT

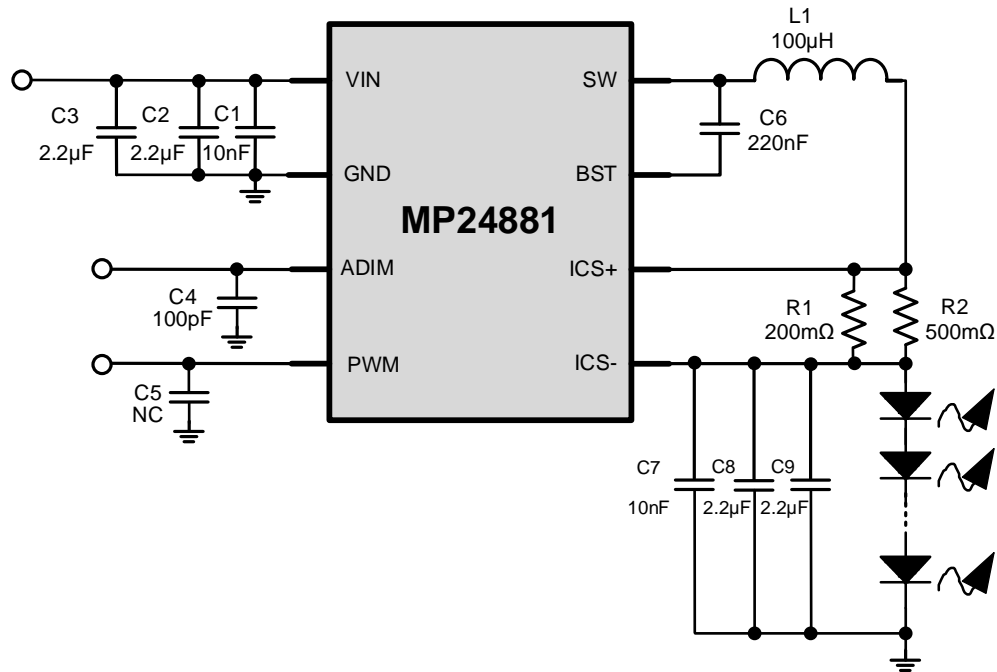
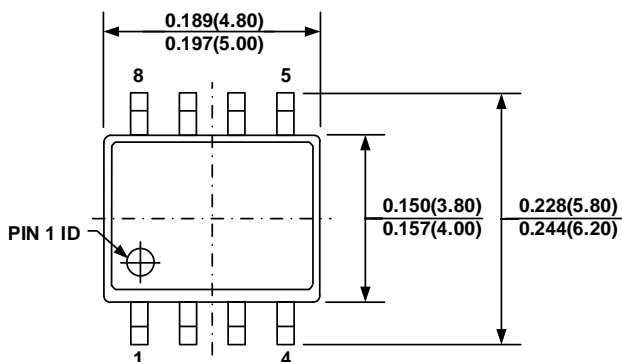


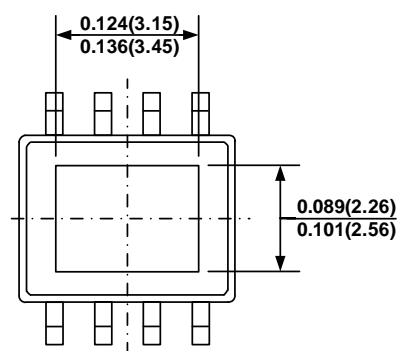
Figure 4: Typical Application Circuit

# PACKAGE INFORMATION

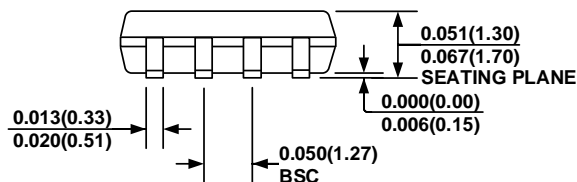
## SOIC-8EP



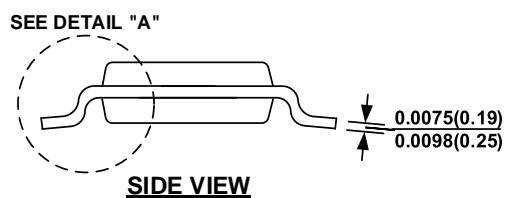
**TOP VIEW**



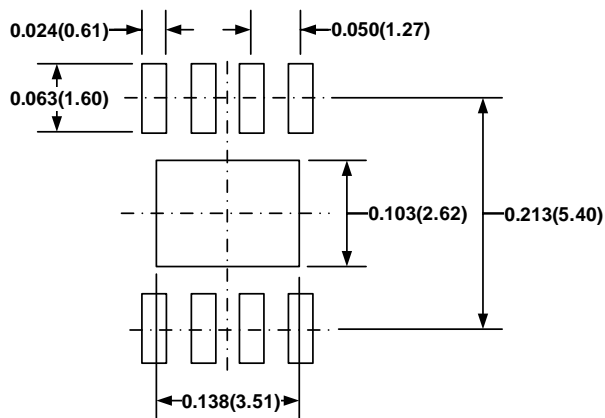
**BOTTOM VIEW**



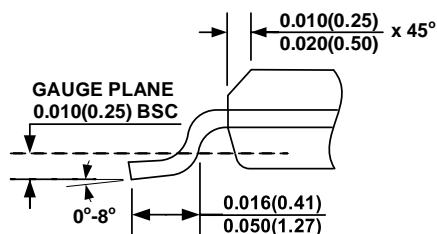
**FRONT VIEW**



**SIDE VIEW**



**RECOMMENDED LAND PATTERN**

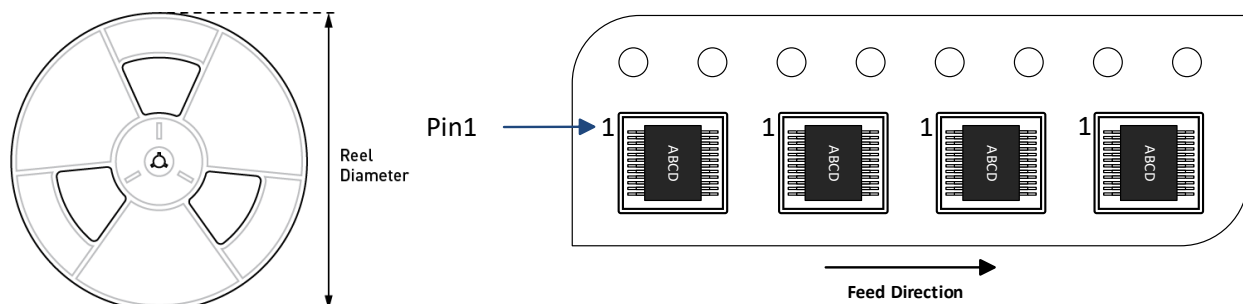


**DETAIL "A"**

### NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP24881GN-Z	SOIC-8EP	2500	100	N/A	13in	12mm	8mm

## REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/12/2023	Initial Release	-

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