■ DESCRIPTION

The FDS9926A is the Dual N-Channel logic enhancement mode power field effect transistor which is produced using high cell density advanced trench technology to provide excellent $R_{DS(ON)}$.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-lin power loss are needed in a very small outline surface mount package

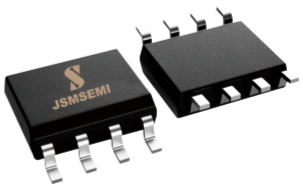
■ FEATURE

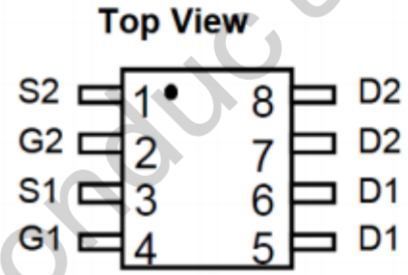
- ***20V/6.0A, $R_{DS(ON)}$=21mΩ(typ.) @V_{GS}=4.5V***
- ***20V/5.2A, $R_{DS(ON)}$=30mΩ(typ.) @V_{GS}=2.5V***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- This is a Full RoHS compliance
- SOP8 package design

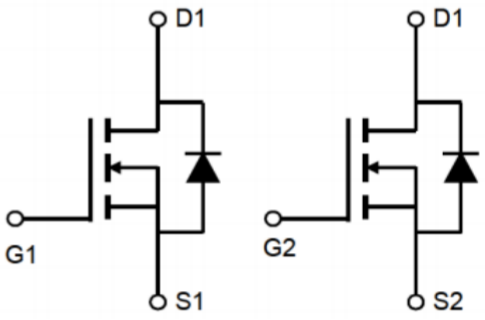
■ APPLICATIONS

- Power Management in Note Book
- Portable Equipment
- Battery Powered System

■ PIN CONFIGURATION







■ ABSOLUTE MAXIMUM RATINGS (T_A = 25℃ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		±12	V
I_D	Continuous Drain Current (T_A=25℃)	V_{GS}=10V	6.0	A
	Continuous Drain Current (T_A=75℃)		5.0	A
I_{DM}	Pulsed Drain Current		20	A
I_S	Continuous Source Current (Diode Conduction)		1	A
P_D	Power Dissipation	T_A=25℃	1.5	W
		T_A=75℃	1.0	
T_J	Operation Junction Temperature		150	℃
T_{STG}	Storage Temperature Range		-55~+150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

■ THERMAL DATA

Symbol	Parameter	Min	Typ	Max	Unit
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		62.5		℃/W

■ *ELECTRICAL CHARACTERISTICS(T_A=25℃ Unless otherwise noted)*

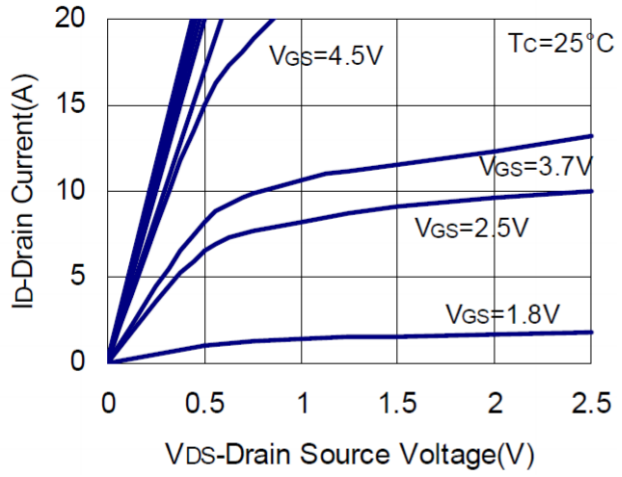
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	0.5	0.7	1.2	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=16V, V_{GS}=0			1	uA
		V_{DS}=16V, V_{GS}=0 T_J=55℃			5	
$I_{D(ON)}$	On=State Drain Current	V_{DS}≧5V, V_{GS}=4.5V	6			A
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=4.5V, I_D=6A		22	30	mΩ
		V_{GS}=2.5V, I_D=5.2A		30	40	
G_{fs}	Forward Transconductance	V_{DS}=5V, I_D=3.6A		10		S
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V		0.75	1.0	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}=10V V_{GS}=4.5V I_D=6.0A		17		nC
Q_{gs}	Gate-Source Charge			0.7		
Q_{gd}	Gate-Drain Charge			3.4		
C_{iss}	Input Capacitance	V_{DS}=10V V_{GS}=0V f=1MHz		850		pF
C_{oss}	Output Capacitance			142		
C_{rss}	Reverse Transfer Capacitance			112		
$T_{d(on)}$	Turn-On Time	V_{DS}=10V I_D=6.0A V_{GEN}=4.5V R_G=3.3Ω		6.5		nS
T_r				12		
$T_{d(off)}$	Turn-Off Time			32		
T_f				7.3		

Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%

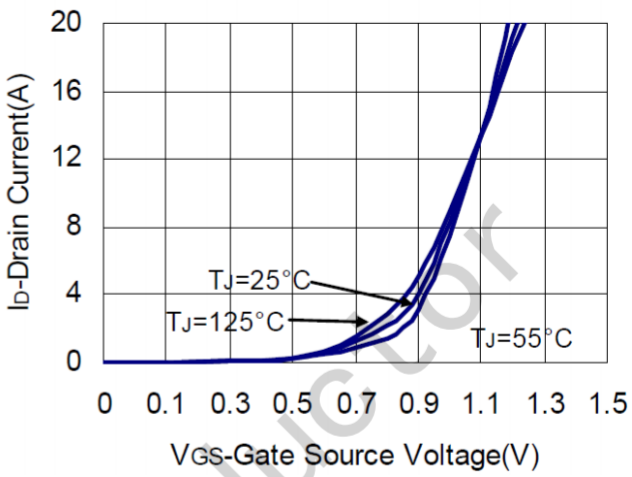
2.Static parameters are based on package level with recommended wire bonding

■ *TYPICAL CHARACTERISTICS (25℃ Unless Note)*

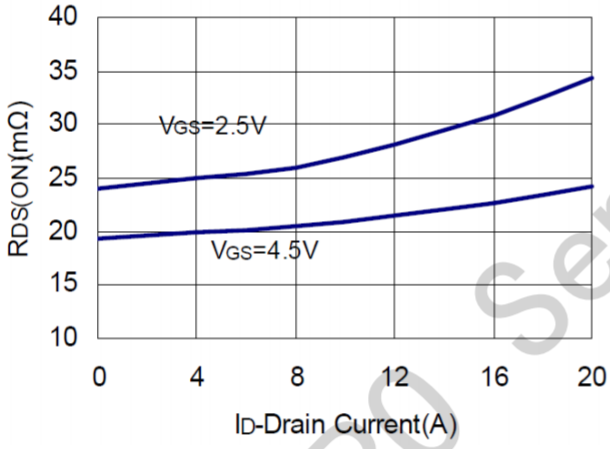
Output Characteristics



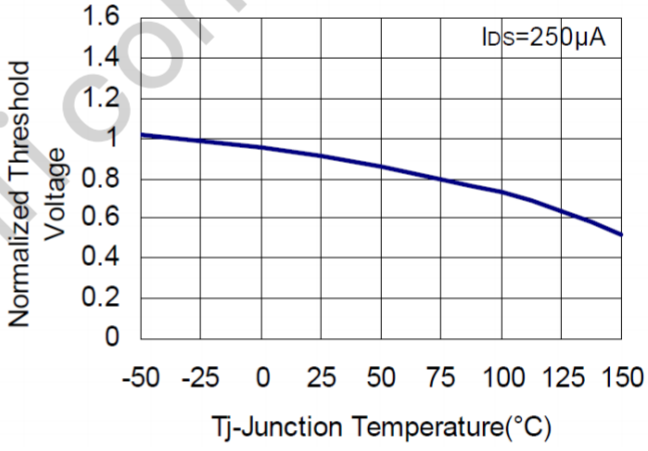
Drain-Source On Resistance



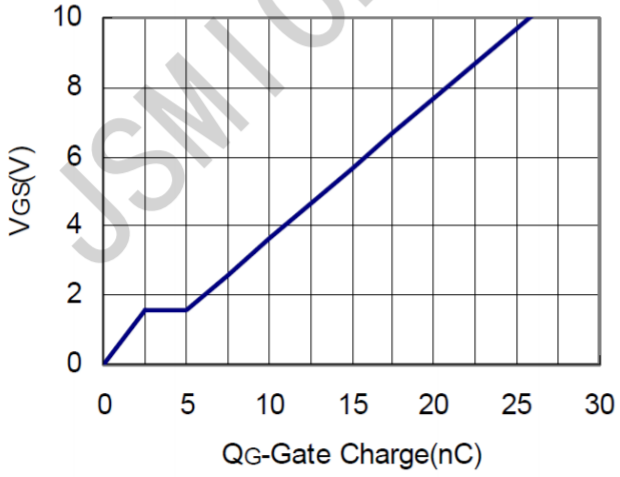
Transfer Characteristics



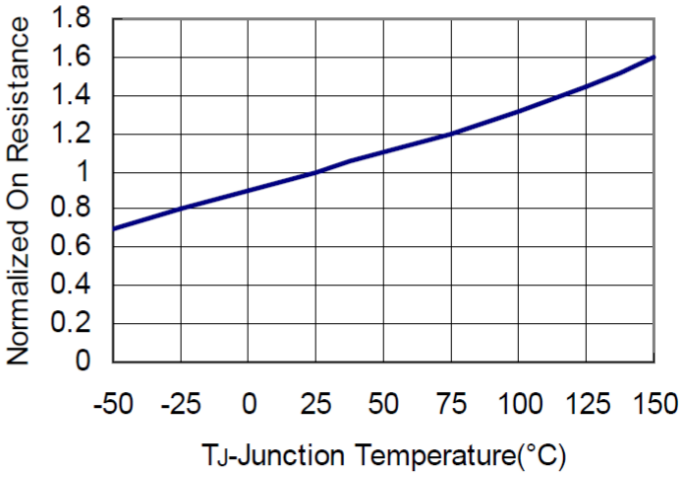
Gate Threshold Voltage



Gate Charge

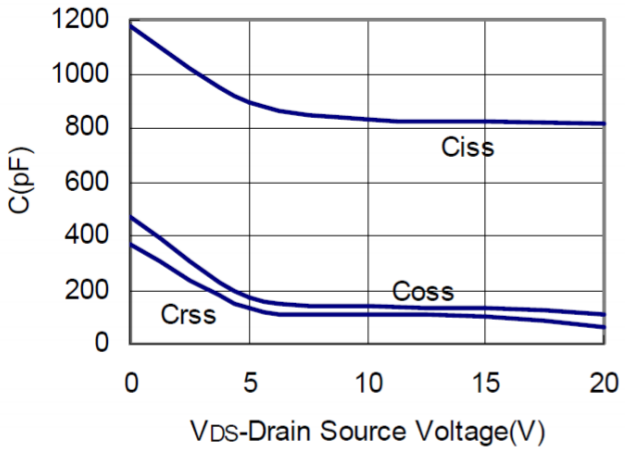


Drain Source On Resistance

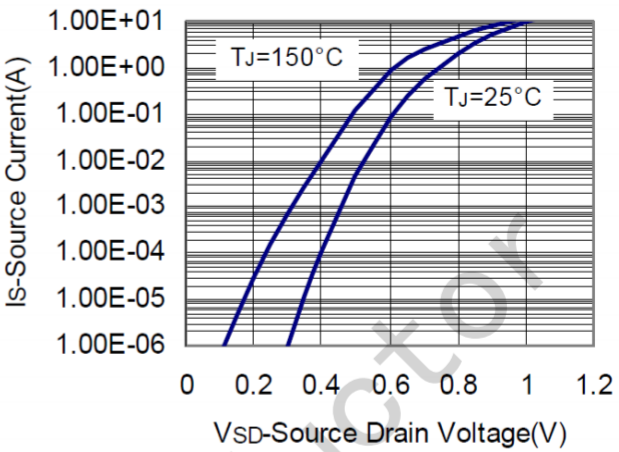


■ *TYPICAL CHARACTERISTICS (continuous)*

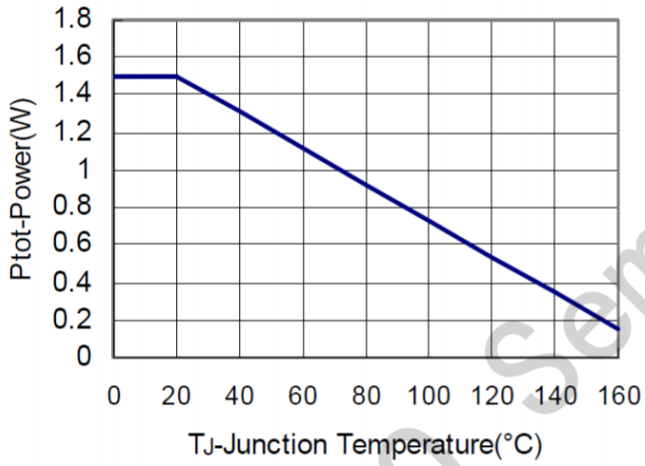
Capacitance



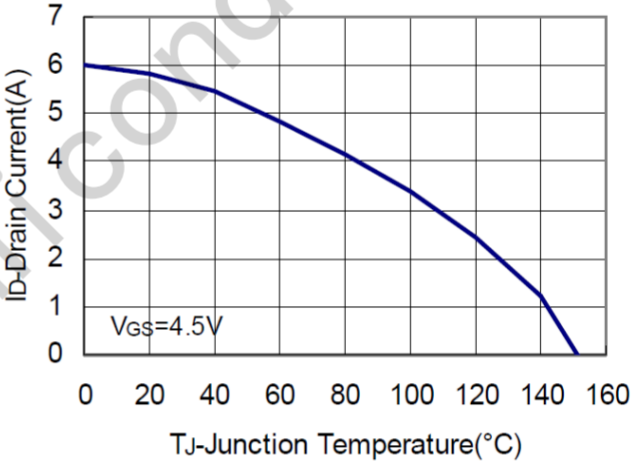
Source Drain Diode Forward



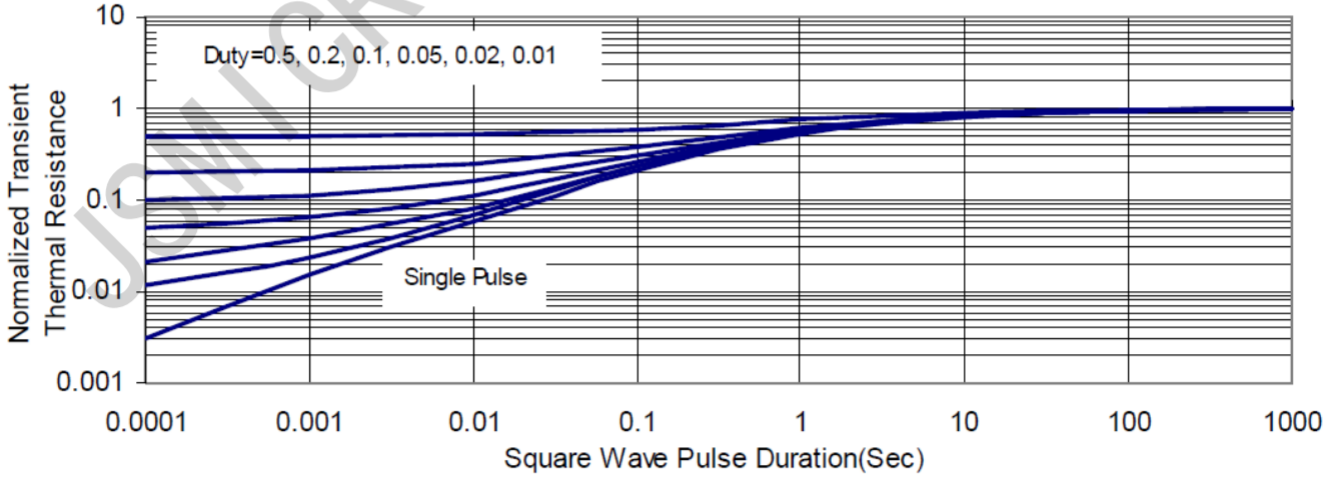
Power Dissipation



Drain Current

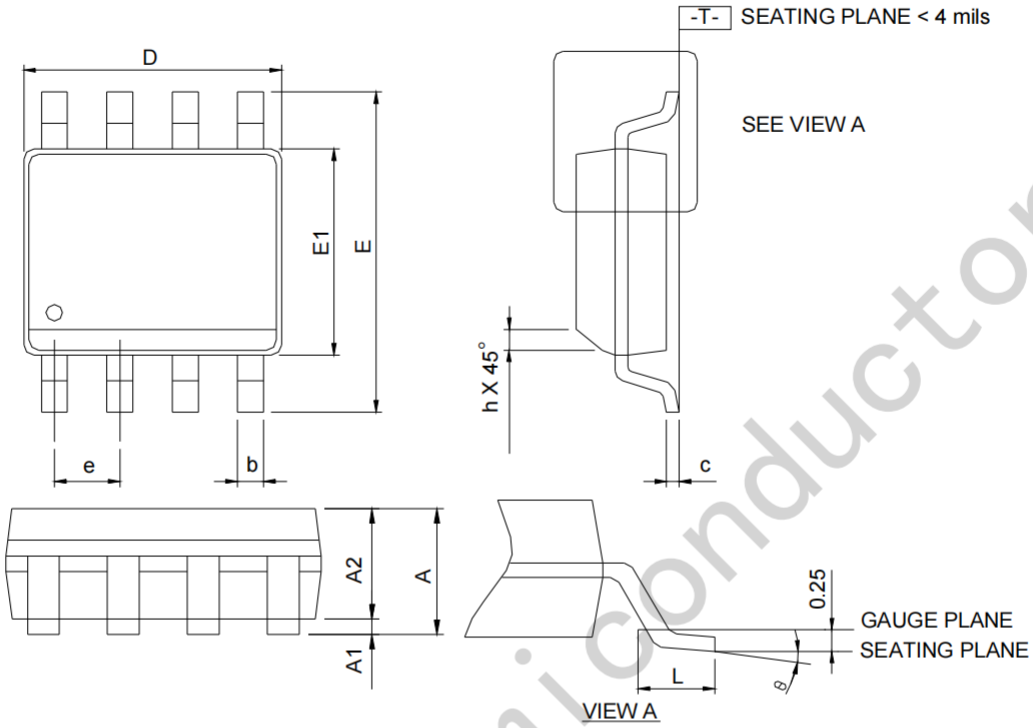


Thermal Transient Impedance



Package Information

SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN