UMW IRF7105TR

25V N-Channel MOSFET
-25V P-Channel MOSFET

1.Description

The SOP-8 has been modified through a customized eadframe "or enhanced therma characterstics and multiple-die capability making it ideal in a variety of power applications.

2.1Features

- Advanced Process Technology Ultra
- Low On-ResistanceSurface Mount
- Dynamic dv/dt Rating
- Fast SwitchingLead-Free

2.2Features(N-Ch)

- $V_{DS\ (V)}$=25V
- $R_{DS(ON)}$<100mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<160mΩ(V_{GS}=4.5V)

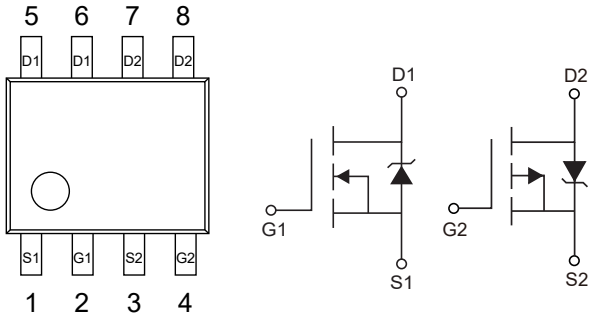
2.3Features(P-Ch)

- $V_{DS\ (V)}$=-25V
- $R_{DS(ON)}$<250mΩ(V_{GS}=-10V)
- $R_{DS(ON)}$<400mΩ(V_{GS}=-4.5V)

3.Pinning information

Pin	Symbol	Description
2,4	G	GATE
1,3	S	SOURCE
5,6,7,8	D	DRAIN

SOP-8



4.Absolute Maximum Ratings

Parameter		Symbol	N-Channel	P-Channel	Units
Continuous Drain Current, V_{GS}=10V	T_A= 25°C	I_D	3.5	-2.3	A
Continuous Drain Current, V_{GS}=10V	T_A=70°C		2.8	-1.8	A
Pulsed Drain Current ①		I_{DM}	14	-10	A
Power Dissipation	T_C= 25°C	P_D	2	2	W
Linear Derating Factor			0.016	0.016	W/°C
Gate-to-Source Voltage		V_{GS}	±20	±20	V
Peak Diode Recovery dv/dt ②		dv/dt	3	-3	V/ns
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	-55 to 150	°C

5.Thermal Characteristics

Parameter	Symbol	Max.	Units
Maximum Junction-to-Ambient ④	$R_{\theta JA}$	62.5	°C/W

6.Electrical Characteristics T_J=25°C

Parameter	Symbol		Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown VoltageBreakdown Voltage	$V_{(BR)DSS}$	N-Ch	I_D=250μA, V_{GS}=0V	25			V
		P-Ch	I_D=-250μA, V_{GS}=0V	-25			V
Breakdown Voltage Temp Coefficient Current	$\frac{\Delta V_{(BR)DSS}}{\Delta T_J}$	N-Ch	I_D=1mA,Reference to 25°C		0.03		V/°C
		P-Ch	I_D=-1mA,Reference to 25°C		-0.015		V/°C
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	N-Ch	V_{GS}=10V, I_D=1A ③		83	100	mΩ
		P-Ch	V_{GS}=4.5V, I_D=0.5A ③		140	160	mΩ
		N-Ch	V_{GS}=-10V, I_D=-1A ③		160	250	mΩ
		P-Ch	V_{GS}=-4.5V, I_D=-0.5A ③		300	400	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	N-Ch	V_{DS}=V_{GS}, I_D=250μA	1		3	V
		P-Ch	V_{DS}=V_{GS}, I_D=-250μA	-1		-3	V
Forward Transconductance	g_{fs}	N-Ch	V_{GS}=15V, I_D=3.5A ③		4.3		S
		P-Ch	V_{GS}=-15V, I_D=-3.5A ③		3.1		S
Drain-to-Source Leakage Current	I_{DSS}	N-Ch	V_{DS}=20V, V_{GS}=0V			2	μA
			V_{DS}=-20V, V_{GS}=0V			-2	μA
		P-Ch	V_{DS}=20V, V_{GS}=0V, T_J=55°C			25	μA
			V_{DS}=-20V, V_{GS}=0V, T_J=55°C			-25	μA
Gate-to-Source ForwardLeakage	I_{GSS}	N-P	V_{GS}=±20V			±100	
Total Gate Charge	Q_g	N-Ch	N-Ch: ③ I_D=2.3A, V_{DS}=12.5V, V_{GS}=10V P-Ch: I_D=-2.3A,V_{DS}=-12.5V,V_{GS}=-10V		9.4	27	nC
		P-Ch			10	25	nC
Gate-to-Source Charge	Q_{gs}	N-Ch				1.7	nC
		P-Ch			1.9		nC
Gate-to-Drain ("Miller") Charge	Q_{gd}	N-Ch				3.1	nC
		P-Ch				2.8	nC
Turn-On Delay Time	$t_{D(on)}$	N-Ch	N-Ch: ③ V_{DD}=25A, I_D=1A R_G=6Ω, R_D=25Ω		7	20	ns
		P-Ch			12	40	ns
Rise Time	t_r	N-Ch			9	20	ns
		P-Ch			13	40	ns

Tum-Off Delay Time	$t_{D(off)}$	N-Ch	P-Ch: ③ V_{DD}=-25A, I_D=-1A R_G=6Ω, R_D=25Ω		45	90	ns
		P-Ch			45	90	ns
Fall Time	t_f	N-Ch			25	50	ns
		N-P			4		ns
Internal Drain Inductace	L_S	P-Ch	Between lead ,6mm (0.25in)from		37	50	nH
Interna l Source Inductance	L_D	N-P	package and center of die contact		6		nH
Input Capacitance	C_{iss}	N-Ch	N-Ch: V_{GS}=0V, V_{DS}=15V, f=1MHz P-Ch: V_{GS}=0V, V_{DS}=-15V, f=1MHz		330		pF
		P-Ch			290		pF
Output Capacitance	C_{oss}	N-Ch			250		pF
		P-Ch			210		pF
ReverseTransferCapacitance	C_{rss}	N-Ch			61		pF
		P-Ch			67		pF
Continuous Source Current (Body Diode)	I_S	N-Ch				2	A
		P-Ch				-2	A
Pulsed Source Current (Body Diode) ①	I_{SM}	N-Ch				14	A
		P-Ch				-9.2	A
Diode Forward Voltage	V_{SD}	N-Ch	T_J=25°C, I_S=1.3A,V_{GS}=0V ③			1.2	V
		P-Ch	T_J=25°C, I_S=-1.3A,V_{GS}=0V ③			-1.2	V
Reverse Recovery Time	t_{rr}	N-Ch	N-Ch: T_J=25°C I_F=1.3A, d_{iF}/d_t=100A/μs P-Ch: T_J=25°C I_F=-1.3A, d_{iF}/d_t=100A/μs ③		36	54	ns
		P-Ch			69	100	ns
Reverse Recovery Charge	Q_{rr}	N-Ch			41	75	nC
		P-Ch			90	180	nC
Forward Turn-On Time	t_{on}	N-P	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited bymax.junction temperature.

② N-Channel I_{SD}≤3.5A, di/dt ≤ 90A/μs, V_{DD}≤$V_{(BR)DSS}$, T_J≤ 150°C.

P-Channel I_{SD}≤ -2.3A, di/dt ≤ 90Aμs, V_{DD}≤$V_{(BR)DSS}$, T_J≤ 150°C.

③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

④ Surface mounted on FR-4 board, t≤ 10sec.

7.1Typical Characterisitics (N-Channel)

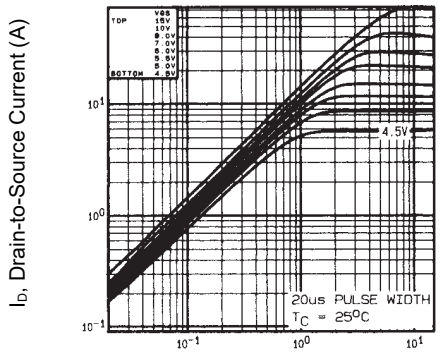


Figure 1: Typical Output Characteristics

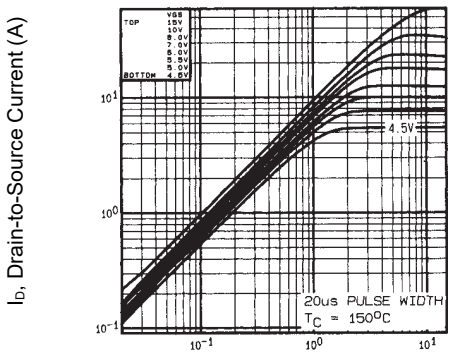


Figure 2: Typical Output Characteristics

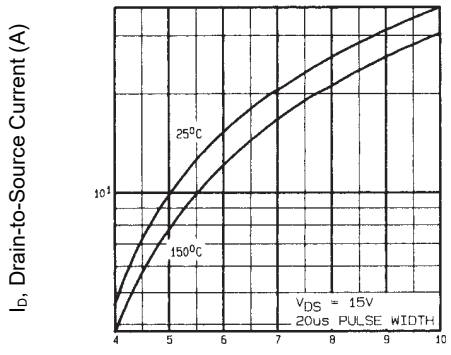


Figure 3: Typical Output Characteristics

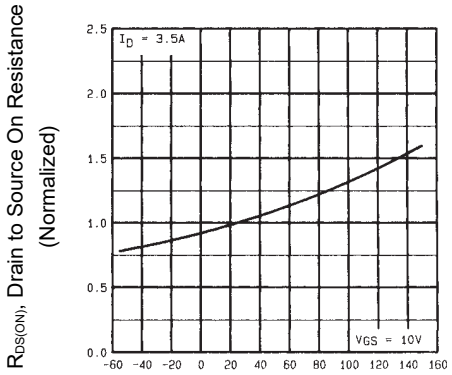


Figure 4: Normalized On-ResistanceVs. Temperature

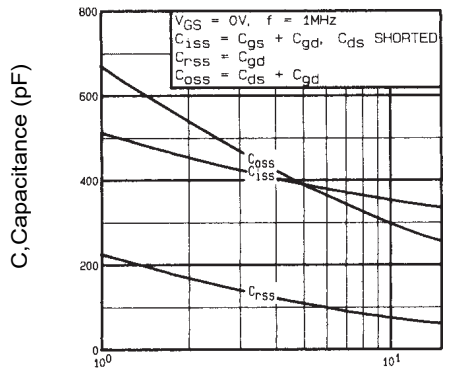


Figure 5: Typical Capacitance vs. Drain-to-Source Voltage

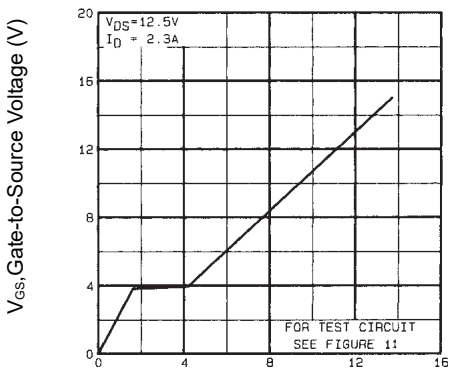


Figure 6: Typical Gate Charge Vs. Gate-to-Source Voltage

7.2Typical Characterisitics (N-Channel)

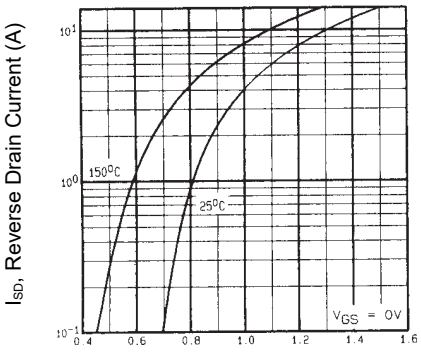


Figure 7: Typical Capacitance vs. Drain-to-Source Voltage

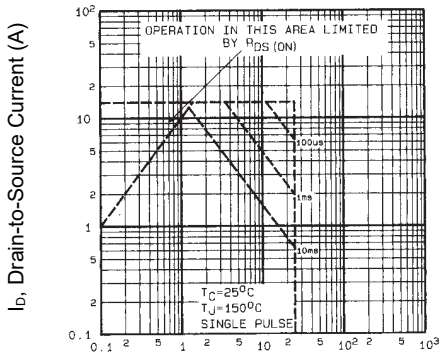


Figure 8: Maximum Safe Operating Area

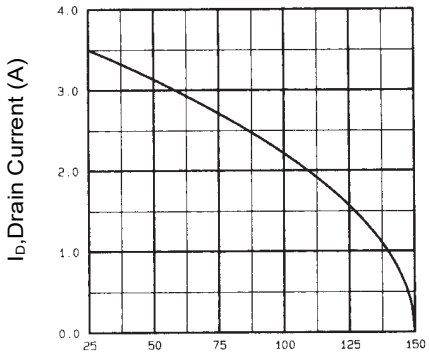


Figure 9: Maximum Drain Current Vs. Ambient Temperature

7.3Typical Characterisitics (N-Channel)

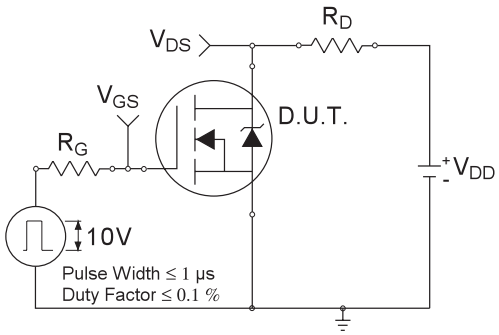


Figure 10a: Switching Time Test Circuit

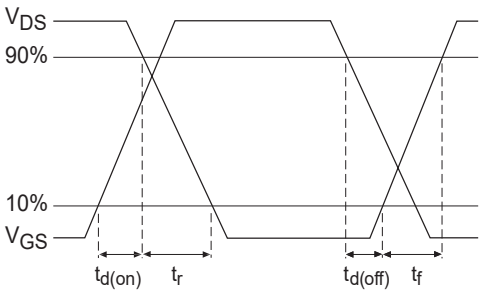


Figure 10b: Switching Time Waveforms

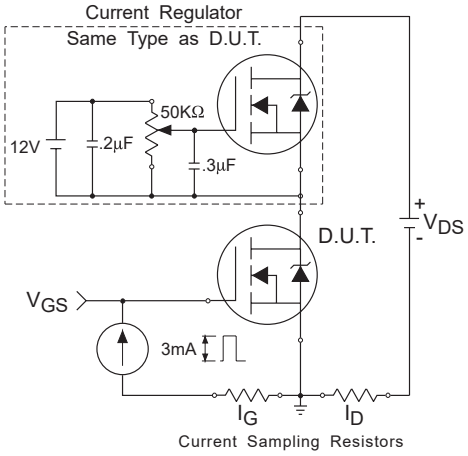


Figure 11a: Gate Charge Test Circuit

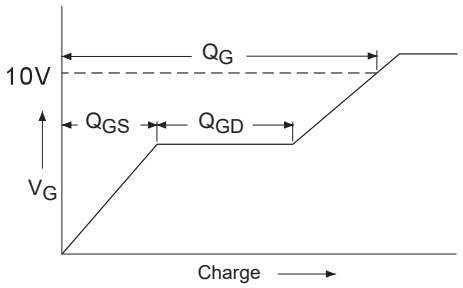


Figure 11b: Basic Gate Charge Wavefomm

7.4Typical Characterisitics (P-Channel)

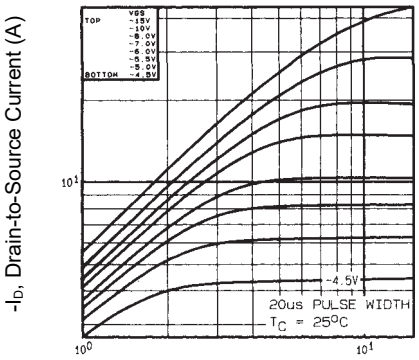


Figure 12: Typical Output Characteristics

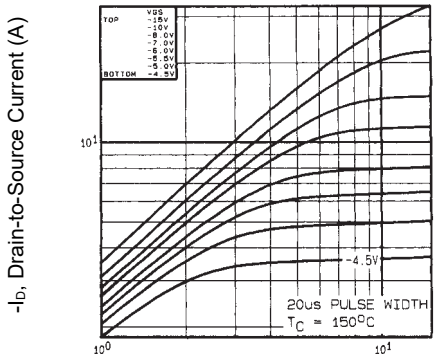


Figure 13: Typical Output Characteristics

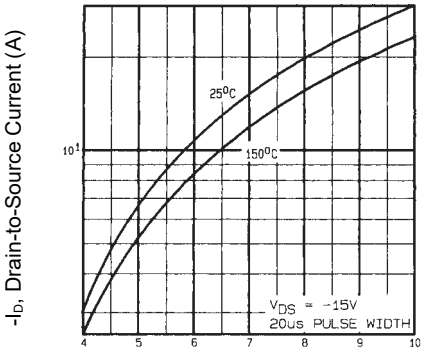


Figure 14: Typical Transfer Characteristics

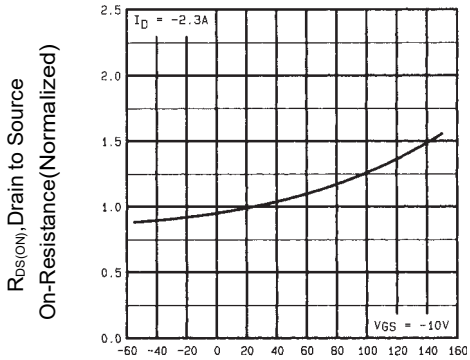


Figure 15: Normalized On-Resistance Vs. Temperature

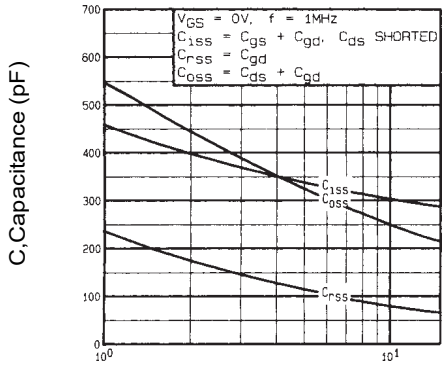


Figure 16: Typical Capacitance Vs. Drain-to-Source Voltage

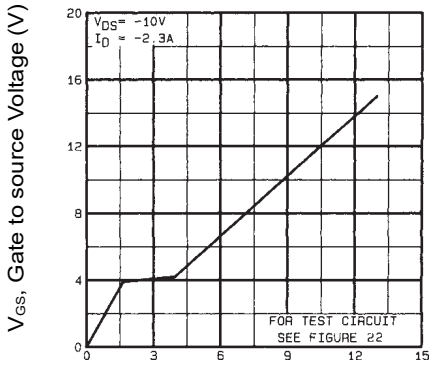


Figure 17: Typical Gate Charge Vs. Gate-to-Source Voltage

7.5Typical Characterisitics (P-Channel)

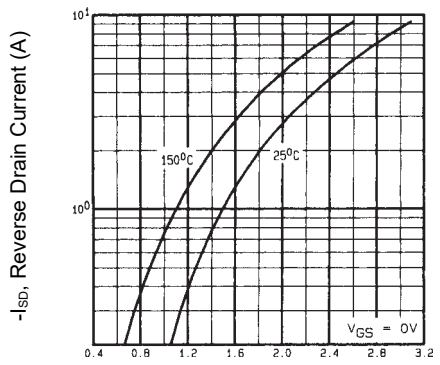


Figure 18: Typical Capacitance vs. Drain-to-Source Voltage

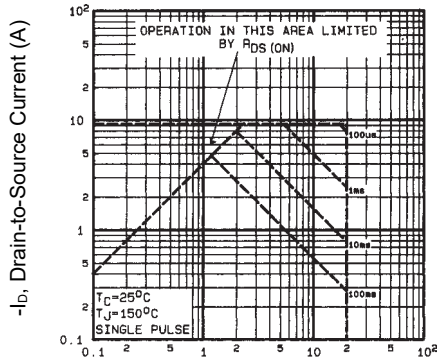


Figure 19: Maximum Safe Operating Area

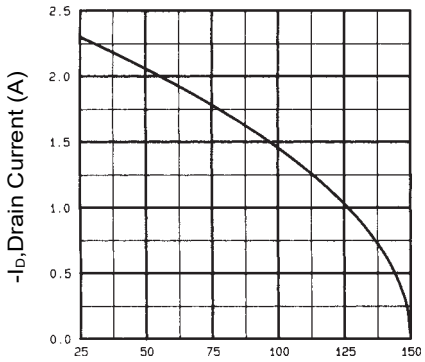


Figure 20: Maximum Drain Current Vs. Ambient Temperature

7.6Typical Characterisitics (P-Channel)

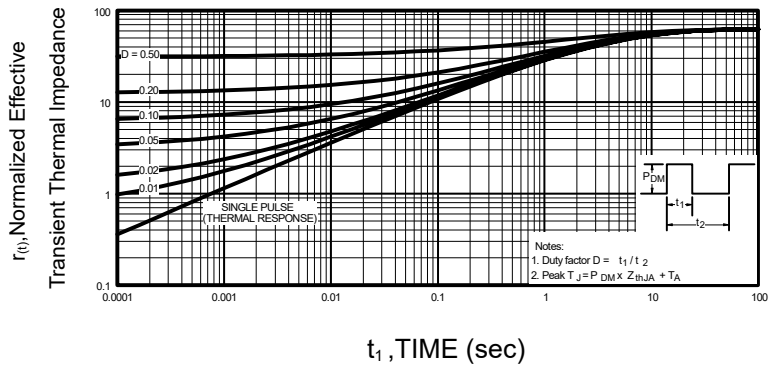


Figure 21: Transient Thermal Response Curve

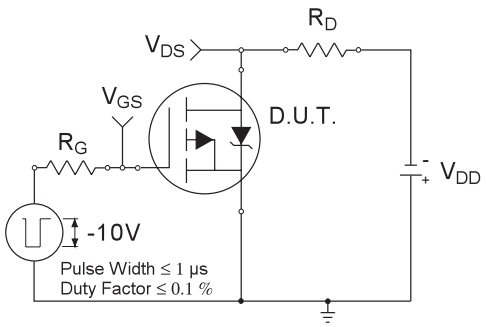


Figure 22a: Switching Time Test Circuit

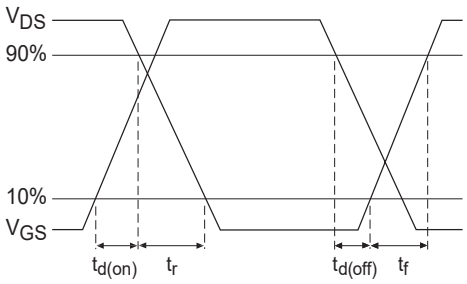


Figure 22b: Switching Time Waveforms

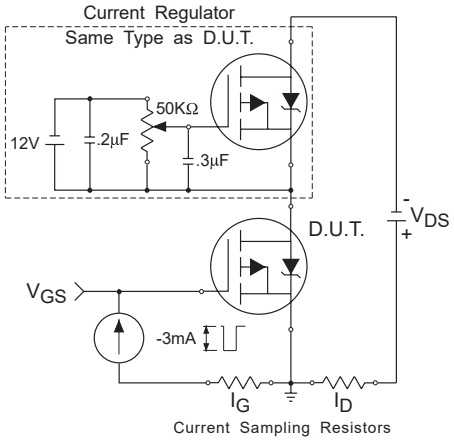


Figure 23a: Gate Charge Test Circuit

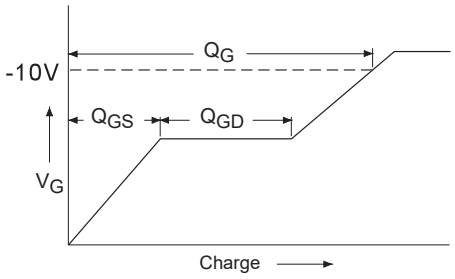
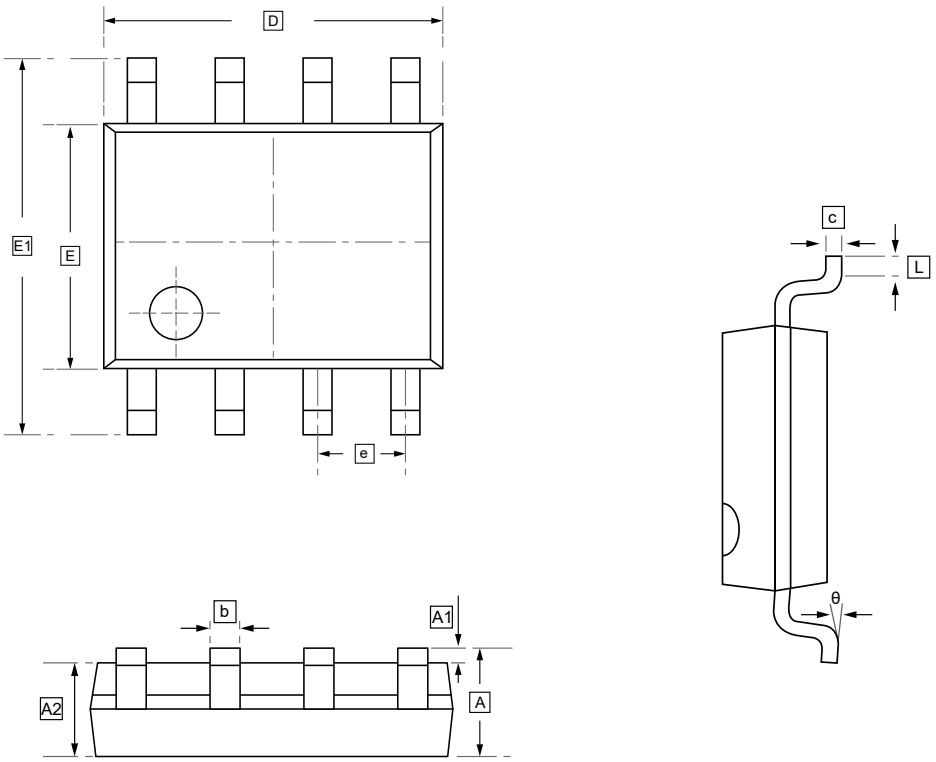


Figure 23b: Basic Gate Charge Wavefomm

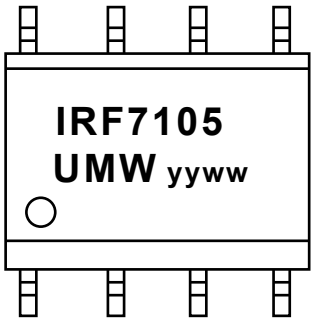
8.SOP-8 PACKAGE OUTLINE DIMENSIONS



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.100	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.250	1.550	0.510	0.250	5.100	4.000	6.200	(BSC)	1.270	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRF7105TR	SOP-8	3000	Tape and reel

10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.