

1.Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$, fast switching speed and extremely low $R_{DS(ON)}$ in a small package.

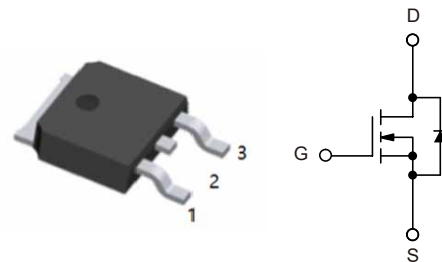
2.Features

- $V_{DS(V)}=30V$
- $R_{DS(ON)}=8m\Omega(V_{GS}=10V)$
- $R_{DS(ON)}=10m\Omega(V_{GS}=4.5V)$
- Low gate charge
- Fast Switching
- High performance trench technology for extremely low $R_{DS(ON)}$

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view



4.Absolute Maximum Ratings $T_A=25^{\circ}C$

Parameter			Symbol	Rating	Units
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	± 20	
Continuous Drain Current	@ $T_C=25^{\circ}C$	(Note 3)	I_D	66	A
	@ $T_A=25^{\circ}C$	(Note 1a)		15	
	Pulsed	(Note 1a)		100	
Power Dissipation	@ $T_C=25^{\circ}C$	(Note 3)	P_D	63	W
	@ $T_A=25^{\circ}C$	(Note 1a)		3.2	
	@ $T_A=25^{\circ}C$	(Note 1b)		1.3	
Storage Junction Temperature Range			T_J, T_{STG}	-55 to 175	$^{\circ}C$



5. Thermal Characteristics

Parameter		Symbol	Rating	Units
Thermal Resistance, Junction-to-Case	(Note 1)	$R_{\theta JC}$	2.4	°C/W
Thermal Resistance, Junction-to-Ambient	(Note 1a)	$R_{\theta JA}$	40	°C/W
Thermal Resistance, Junction-to-Ambient	(Note 1b)	$R_{\theta JA}$	96	°C/W



6. Electrical Characteristic ($T_A=25^\circ\text{C}$ unless otherwise noted)

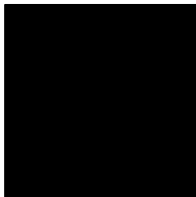
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Energy	E_{AS}	Single Pulse, $V_{DD}=15\text{V}$, $I_D=66\text{A}$			67	mJ
Drain-Source Avalanche Current	I_{AS}				66	A
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	30			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	$I_D=250\mu\text{A}$ Referenced to 25°C		26		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate-Body Leakage	I_{GSS}	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1	1.8	3	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	$I_D=250\mu\text{A}$ Referenced to 25°C		-5		mV/ $^\circ\text{C}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$, $I_D=15\text{A}$		6.3	8	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=13\text{A}$		7.9	10	m Ω
On-State Drain Current	$I_{D(on)}$	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	50			A
Forward Transconductance	g_{FS}	$V_{DS}=10\text{V}$, $I_D=15\text{A}$		60		S
Input Capacitance	C_{iss}	$V_{DS}=15\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$		1755		pF
Output Capacitance	C_{oss}			430		pF
Reverse Transfer Capacitance	C_{rss}			180		pF
Gate Resistance	R_g	$V_{OSC}=15\text{mV}$, $f=1\text{MHz}$		1.3		ns
Turn-On DelayTime	$t_{D(on)}$	$V_{DD}=15\text{V}$, $I_D=1\text{A}$ $V_{GS}=10\text{V}$, $R_{GEN}=6\Omega$		11	20	ns
Turn-On Rise Time	t_r			12	21	ns
Turn-Off DelayTime	$t_{D(off)}$			29	47	ns
Turn-Off Fall Time	t_f			19	34	ns
Total Gate Charge	Q_g	$V_{DS}=15\text{V}$, $I_D=15\text{A}$ $V_{GS}=5\text{V}$		16	22	nC
Gate-Source Charge	Q_{gs}			4.6		nC
Gate-Drain Charge	Q_{gd}			6.2		nC



Maximum Continuous Drain–Source Diode Forward Current	I_S				2.3	A
Drain–Source Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=2.3A$ (Note 2)		0.74	1.2	V
Diode Reverse Recovery Time	t_{rr}	$I_F=15A, dI_F/dt=100A/\mu s$		28		ns
Diode Reverse Recovery Charge	Q_{rr}			18		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.
- $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- a) $R_{\theta JA}=45^{\circ}C/W$ when mounted
■ on a 1in² pad of 2oz copper.



- b) $R_{\theta JA}= 96^{\circ}C/W$ when mounted
■ on a minimum pad.

Scale 1 : 1 on letter size paper.

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%.

3. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$

where P_D is maximum power dissipation at $T_C=25^{\circ}C$ and $R_{DS(ON)}$ is at $T_{J(max)}$ and $V_{GS}=10V$. Package current limitation is 21A.



7.1 Typical characteristic

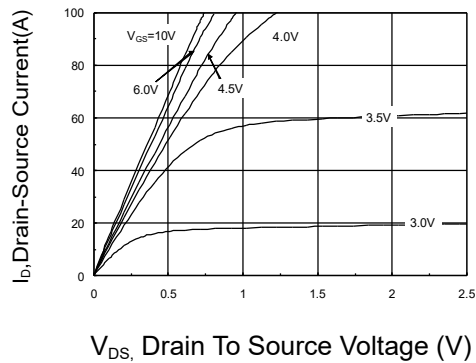


Figure 1: On-Region Characteristics

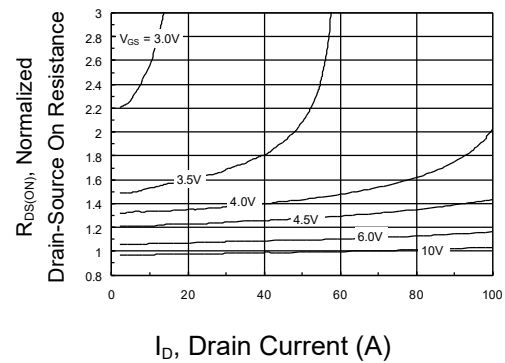


Figure 2: On-Resistance Variation with Drain Current and Gate Voltage

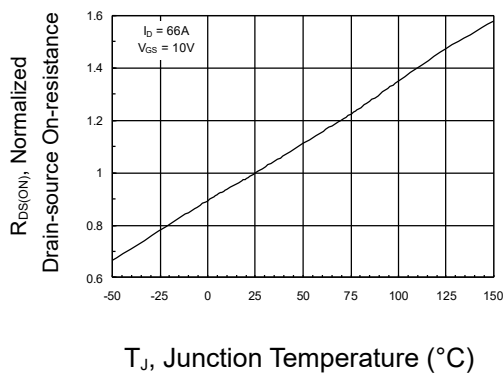


Figure 3: On-Resistance Variation with Temperature

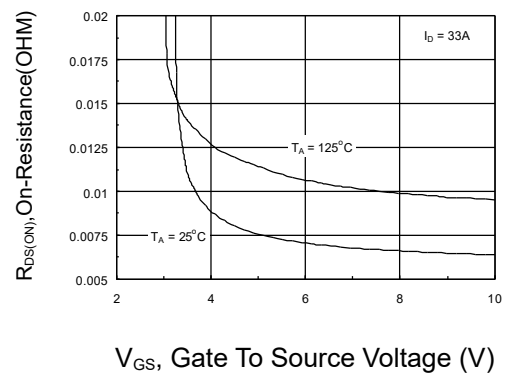


Figure 4: On-Resistance Variation with Gate-to-Source Voltage

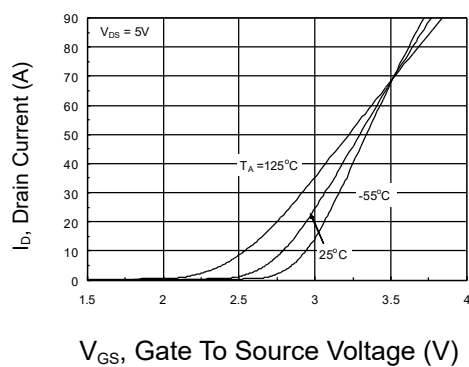


Figure 5: Transfer Characteristics

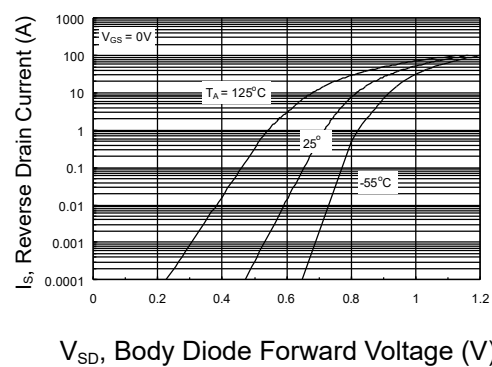


Figure 6: . Body Diode Forward Voltage Variation with Source Current and Temperature



7.2 Typical characteristic

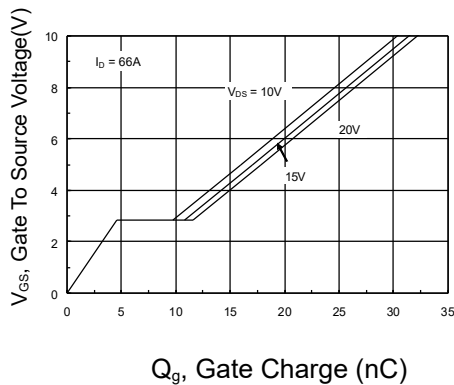


Figure 7: Gate Charge Characteristics

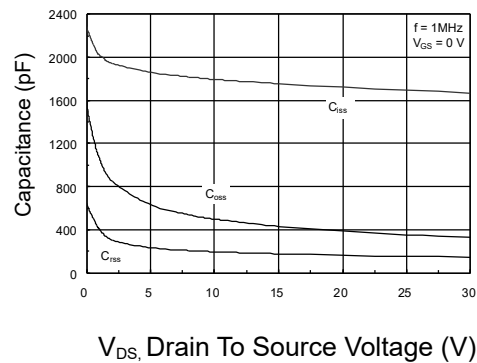


Figure 8: Capacitance Characteristics

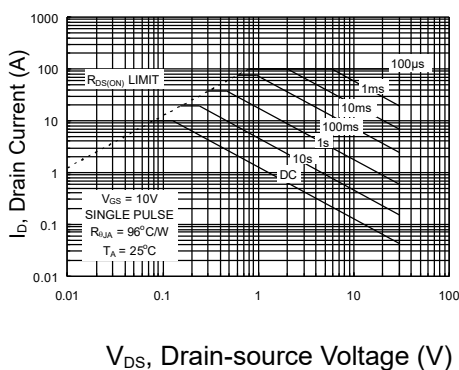


Figure 9: Maximum Safe Operating Area

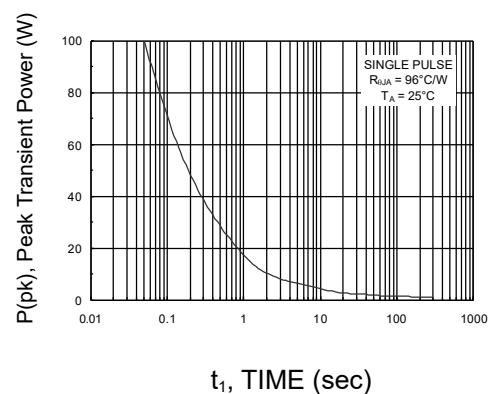


Figure 10: Single Pulse Maximum Power Dissipation

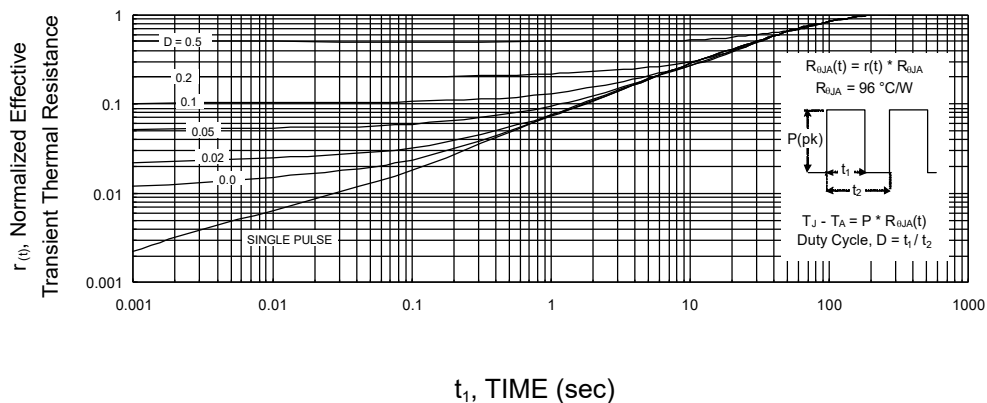
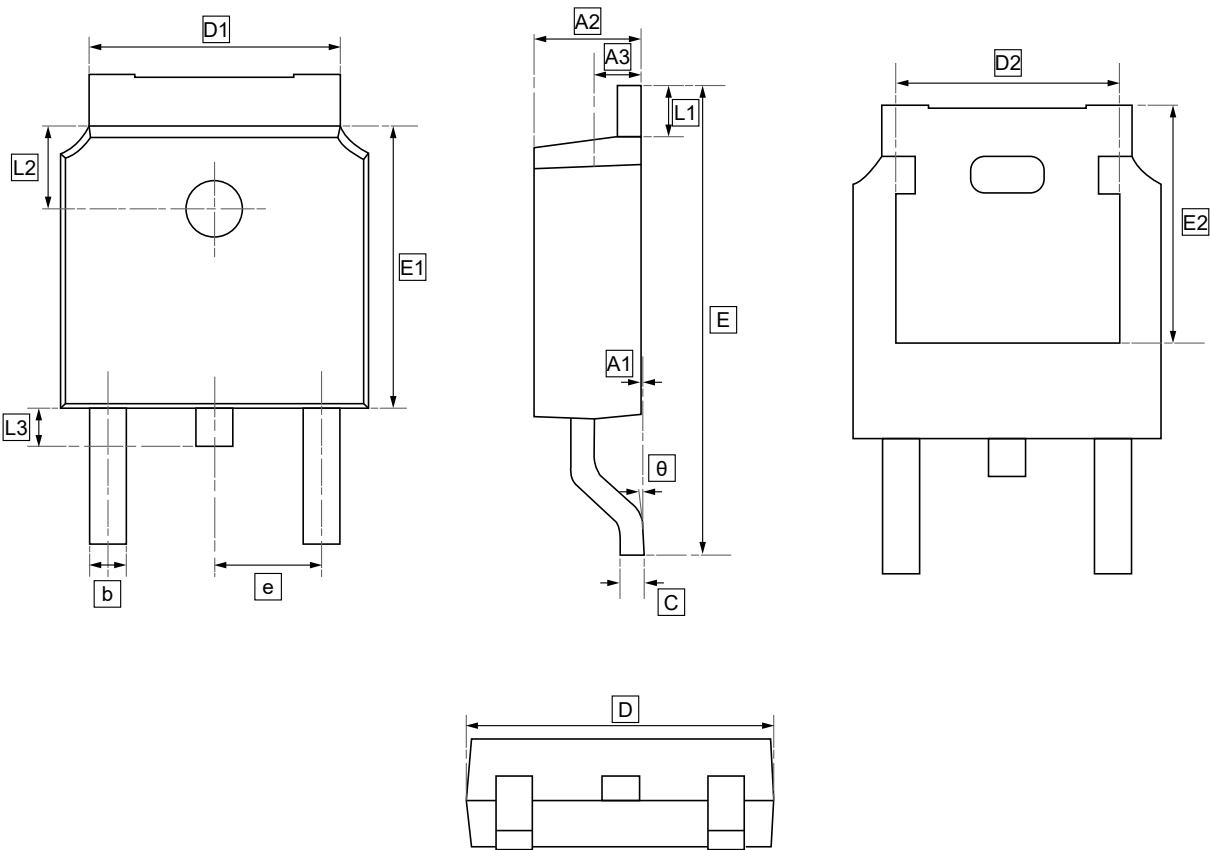


Figure 11: Transient Thermal Response Curve



8.TO-252 Package Outline Dimensions

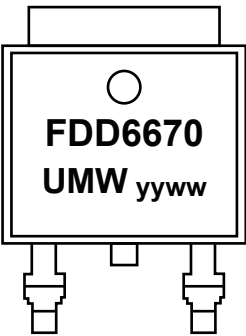


DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286 BSC	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38		1.27	1.90	1.00	8.00



9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDD6670A	TO-252	2500	Tape and reel



10.Disclaimer

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