UMW FDV304P

P-Channel Enhancement MOSFET

1.Description

This P-Channel enhancement mode field effect transistors is produced using Fairchild's proprietary, high cell density, DMOStechnology. This very high density process is tailored to minimizeon-state resistance at low gate drive conditions.

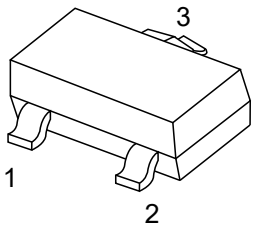
2.Features

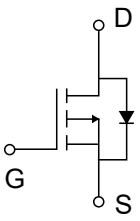
- $V_{DS\ (V)}$=-30V
- I_D=-4.2A(V_{GS}=-10V)
- $R_{DS(ON)}$<65mΩ(V_{GS}=-4.5V)
- $R_{DS(ON)}$<120mΩ(V_{GS}=-2.5V)

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	S	SOURCE
3	D	DRAIN

SOT-23





4.Absolute Maximum Ratings T_A= 25°C

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current	T_A=25°C	I_D	-4.2	A
	T_A=70°C		-3.5	
Pulsed Drain Current		I_{DM}	-30	
Power Dissipation	T_A=25°C	P_D	1.4	W
	T_A=70°C		1	
Thermal Resistance.Junction- to-Ambient t ≤ 10s		R_{thJA}	90	°C/W
Thermal Resistance.Junction- to-Ambient			125	
Thermal Resistance.Junction- to-Case		R_{thJC}	60	
Junction Temperature		T_J	150	°C
Junction and Storage Temperature Range		T_{STG}	-55 to 150	

5.Electrical Characteristics T_A= 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	V_{DSS}	I_D=250μA, V_{GS}=0V	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V, V_{GS}=0V			-1	μA
		V_{DS}=-24V,V_{GS}=0V,T_J=55°C			-5	
Gate-Body leakage current	I_{GSS}	V_{DS}=0V, V_{GS}=±12V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-0.4		-1.3	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-4A			65	mΩ
		V_{GS}=-2.5V, I_D=-1A			120	
On state drain current	$I_{D(ON)}$	V_{GS}=-4.5V, V_{DS}=-5V	-25			A
Forward Transconductance	g_{FS}	V_{DS}=-5V, I_D=-5A	7	11		S
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-15V, f=1MHz		954		pF
Output Capacitance	C_{oss}			115		
Reverse Transfer Capacitance	C_{rss}			77		
Gate resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz		6		Ω
Total Gate Charge	Q_g	V_{GS}=-4.5V, V_{DS}=-15V I_D=-4A		9.4		nC
Gate Source Charge	Q_{gs}			2		
Gate Drain Charge	Q_{gd}			3		
Turn-On DelayTime	$t_{D(on)}$	V_{GS}=-10V, V_{DS}=-15V R_L=3.6Ω, R_{GEN}=6Ω		6.3		ns
Turn-On Rise Time	t_r			3.2		
Turn-Off DelayTime	$t_{D(off)}$			38.3		
Turn-Off Fall Time	t_f			12		
Body Diode Reverse Recovery Time	t_{rr}	I_F=-4A, dI/dt=100A/μs		20.2		
Body Diode Reverse Recovery Charge	Q_{rr}	I_F=-5A, dI/dt=100A/μs		11.2		nC
Maximum Body-Diode Continuous Current	I_S				-2.2	A
Diode Forward Voltage	V_{SD}	I_S=-1A, V_{GS}=0V		-0.75	-1	V

6.1Typical Characterisitics

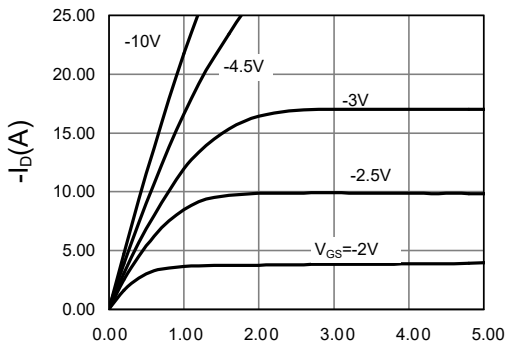


Fig 1: On-Region Characteristics

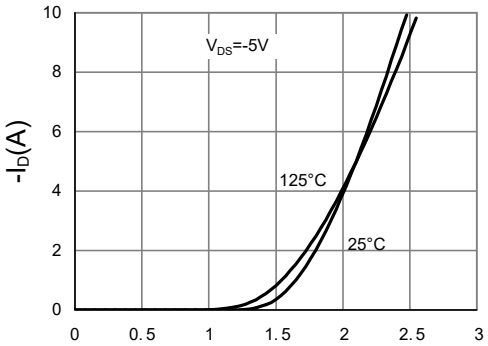


Figure 2: Transfer Characteristics

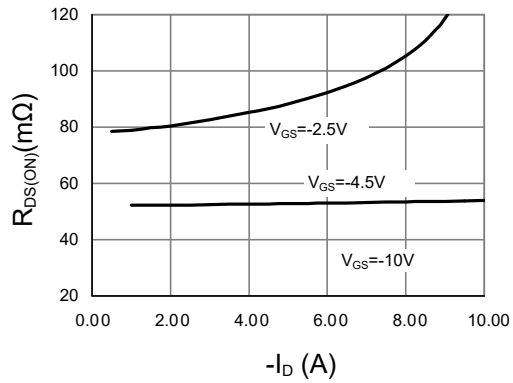


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

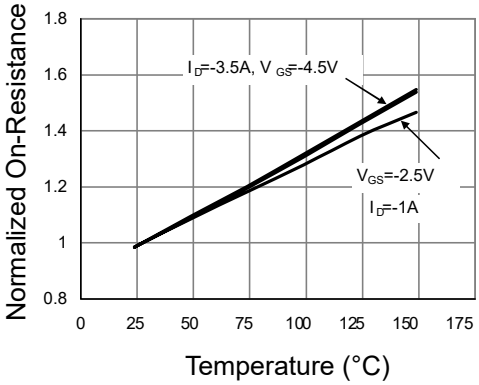


Figure 4: On-Resistance vs. Junction Temperature

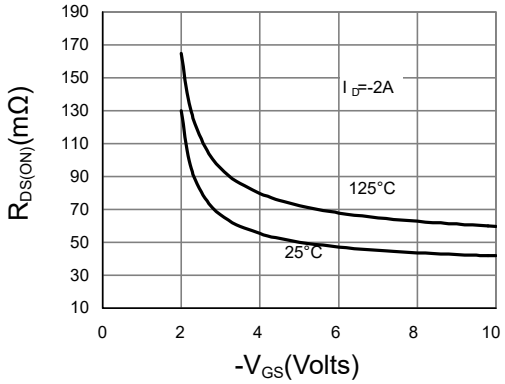


Figure 5: On-Resistance vs. Gate-Source Voltage

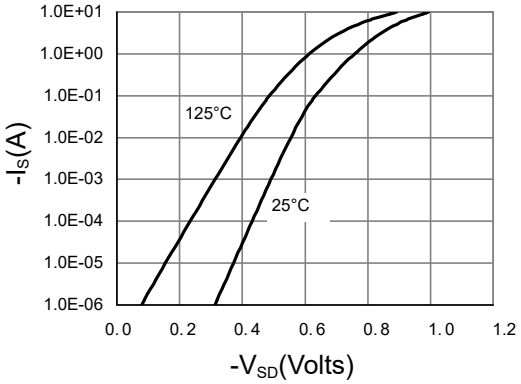


Figure 6: Body-Diode Characteristics

6.2Typical Characterisitics

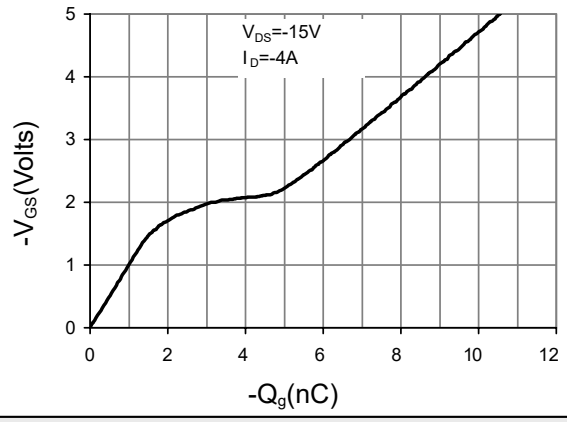


Figure 7: Gate-Charge Characteristics

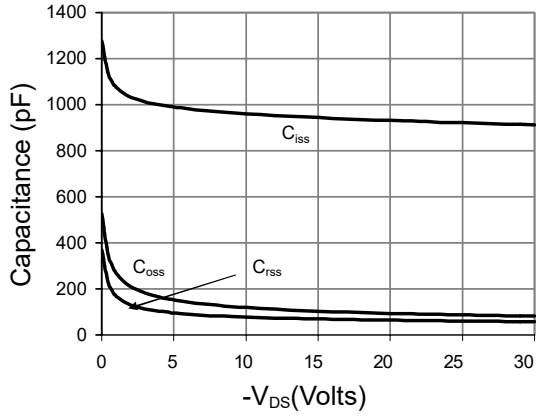


Figure 8: Capacitance Characteristics

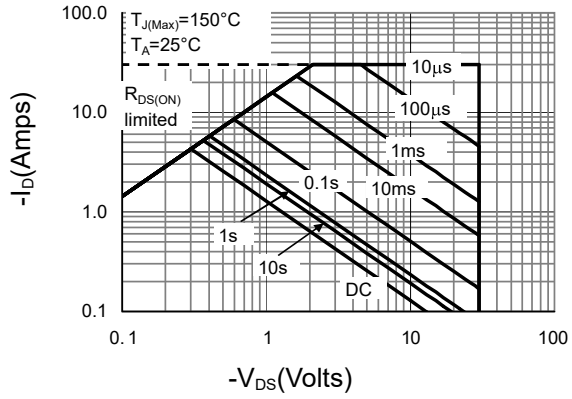


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

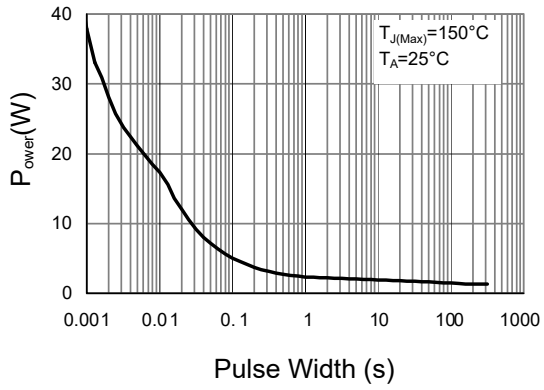


Figure 10: Single Pulse Power Rating Junction-to -Ambient (Note E)

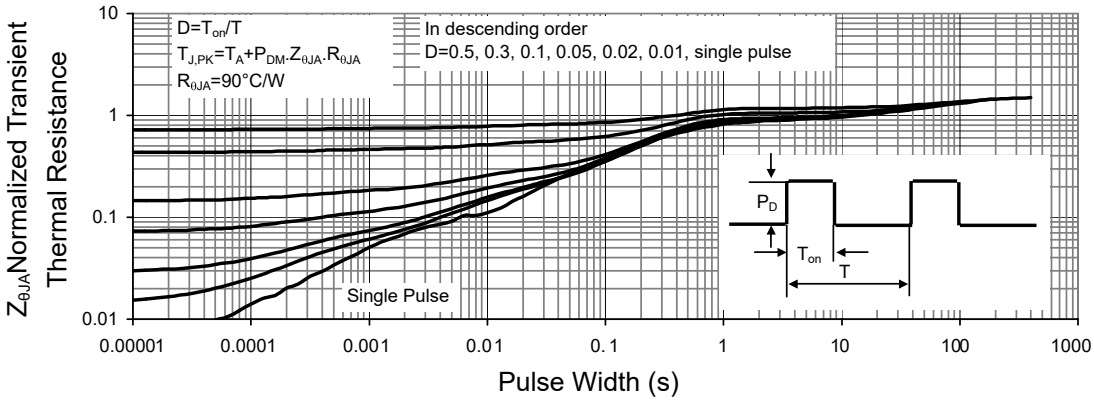
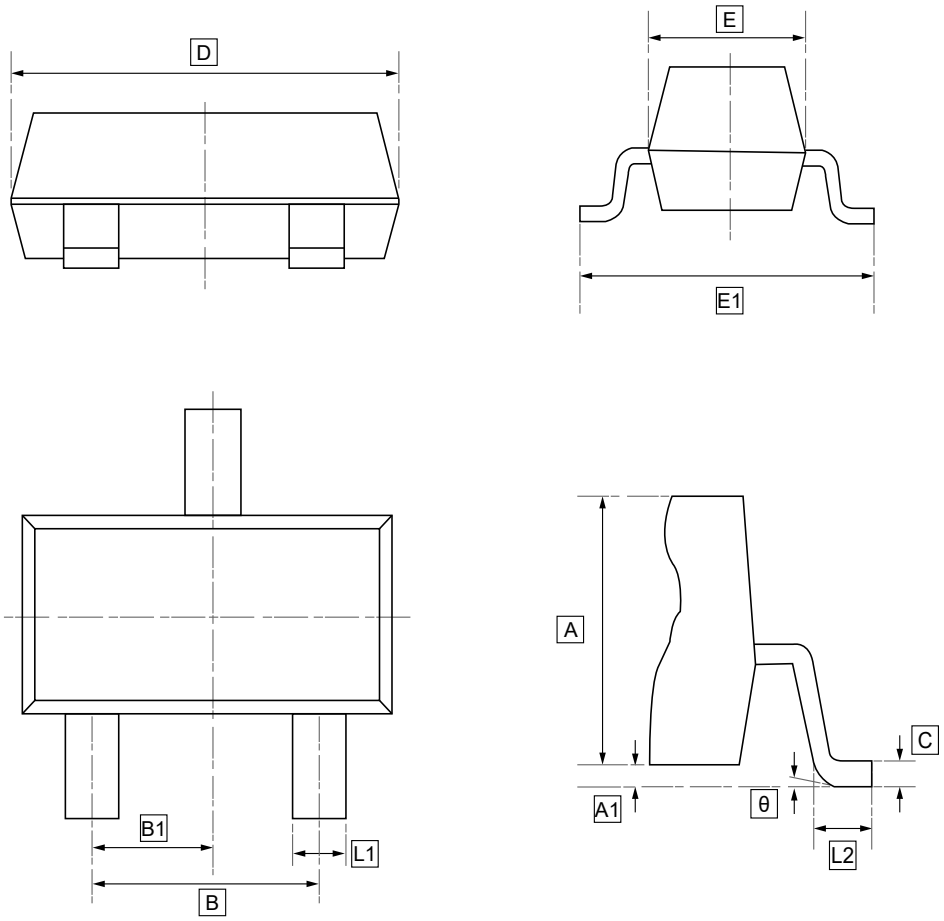


Figure 11: Normalized Maximum Transient Thermal Impedance

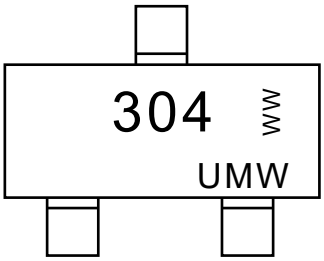
7.SOT-23 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	L1	L2	C	D	E	E1	B	B1	θ
Min	1.050	0.000	0.300	0.350	0.100	2.820	1.500	2.700	1.800	0.950	0°
Max	1.150	0.100	0.500	0.550	0.200	3.020	1.700	2.900	2.000	TYP	8°

8.Ordering information



WW: Batch Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDV304P	SOT-23	3000	Tape and reel

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