UMW IRLR3915TR

55V N-Channel MOSFET

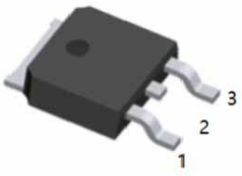
1.Features

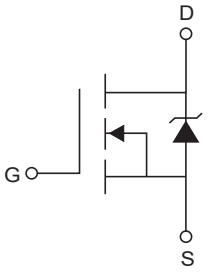
- $V_{DS\ (V)}$=55V
- I_D=30A(V_{GS}=10V)
- $R_{DS(ON)}$<14mΩ(V_{GS}=10V)
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching

2.Pinning information

Pin	Symbol	Description
1	G	GATE
3	S	SOURCE
2	D	DRAIN

TO-252(DPAK)
top view





3.Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Continuous Drain Current, VGS @ 10V (Silicon limited)	T_C=25°C	I_D	61	A
Continuous Drain Current, VGS @ 10V (See Fig.9)	T_C=100°C		43	A
Continuous Drain Current, VGS @ 10V (Package limited)	T_C=25°C		30	A
Pulsed Drain Current ①		I_{DM}	240	A
Power Dissipation	T_C=25°C	P_D	120	W
Linear Derating Factor			0.77	W/°C
Gate-to-Source Voltage		V_{GS}	±16	V
Single Pulse Avalanche Energy ②		E_{AS}	200	mJ
Single Pulse Avalanche Energy Tested Value⑦		E_{AS} (6 sigma)	600	mJ
Avalanche Current①		I_{AR}	See Fig.12a	A
Repetitive Avalanche Energy⑥		E_{AR}	12b, 15, 16	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C
Soldering Temperature, for 10 seconds			300 (1.6mm from case)	°C

4.Thermal resist ance rating

Parameter	Symbol	Typ	Max	Units
Junction-to-Case	$R_{\theta JC}$		1.3	°C/W
Junction-to-Ambient (PCB Mount) ⑧	$R_{\theta JA}$		50	°C/W
Junction-to-Ambient	$R_{\theta JA}$	110		°C/W

5.Electrical Characteristics T_J=25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=250μA, V_{GS}=0V	55			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/T_J$	I_D=1mA,Reference to 25°C		0.057		V/°C
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=30A ④		12	14	mΩ
		V_{GS}=5V, I_D=26A ④		14	17	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=10V, I_D=250μA	1	1.6	3	V
Forward Transconductance	g_{FS}	V_{DS}=25V, I_D=30A	42			S
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=55V, V_{GS}=0V			20	μA
		V_{DS}=55V,V_{GS}=0V,T_J=125°C			250	
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS}=16V			200	nA
Gate-to-Source Reverse Leakage		V_{GS}=-16V			-200	
Total Gate Charge	Q_g	I_D=30A		61	92	nC
Gate-to-Source Charge	Q_{gs}	V_{DS}=44V		9	14	
Gate-to-Drain ("Miller") Charge	Q_{gd}	V_{GS}=10V ④		17	25	
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=28V, I_D=30A R_G=8.5Ω, V_{GS}=10V ④		7.4		ns
Rise Time	t_r			51		ns
Turn-Off Delay Time	$t_{D(off)}$			83		ns
Fall Time	t_f			100		ns
Internal Drain inductance	L_D	Between lead, 6mm (0.25in.)		4.5		nH
Internal Source inductance	L_S	from package and center of die contact		7.5		
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V		1870		pF
Output Capacitance	C_{oss}			390		pF
Reverse Transfer Capacitance	C_{rss}	f=1.0MHz, See Fig. 5		74		pF
Output Capacitance	C_{oss}	V_{GS}=0V, V_{DS}=1V, f=1MHz		2380		pF
Output Capacitance	C_{oss}	V_{GS}=0V, V_{DS}=44V, f=1MHz		290		pF
Effective Output Capacitance ⑤	C_{oss}eff.	V_{GS}=0V, V_{DS}=0V to 44V		540		pF

Source-Drain Ratings and Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			61	A
Pulsed Source Current (Body Diode) ①	I_{SM}				240	A
Diode Forward Voltage	V_{SD}	T_J=25°C, I_S=30A, V_{GS}=0V ④			1.3	V
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=30A, V_{DD}=25xjkl V dI/dt=100A/μs ④		62	93	ns
Reverse Recovery Charge	Q_{rr}			110	170	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

6.1Typical Characterisitics

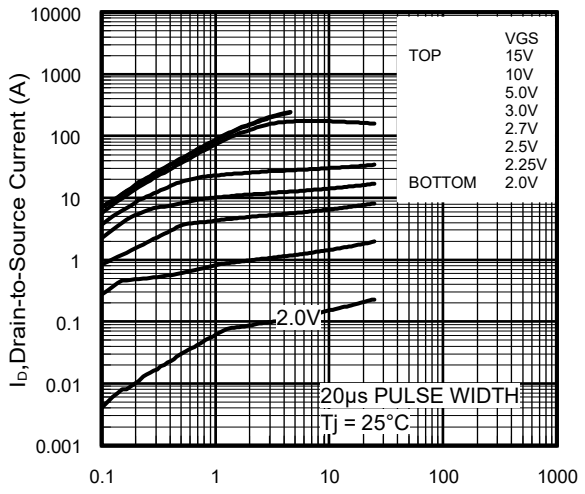


Figure 1: Typical Output Characteristics

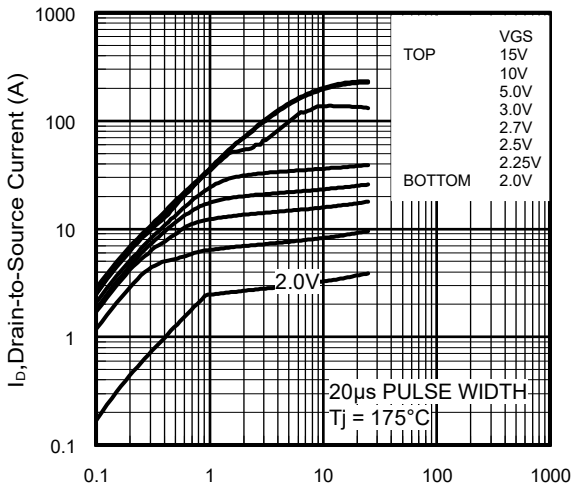


Figure 2: Typical Output Characteristics

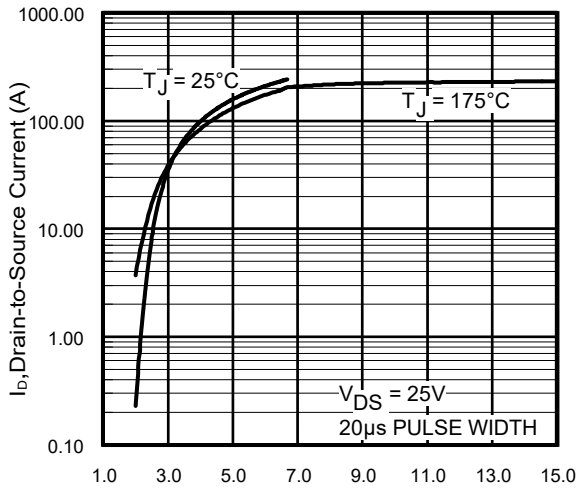


Figure 3: Typical Transfer Characteristics

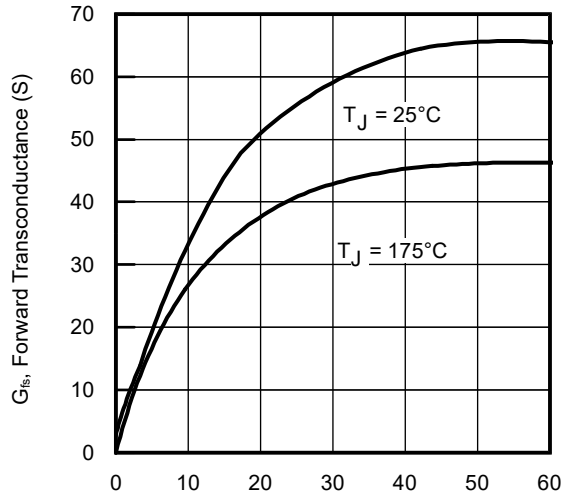
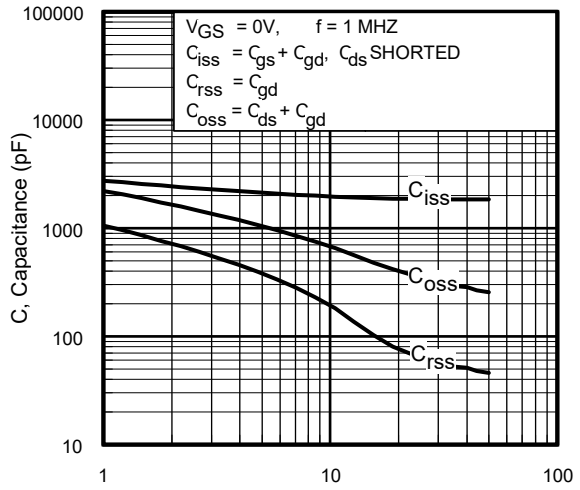


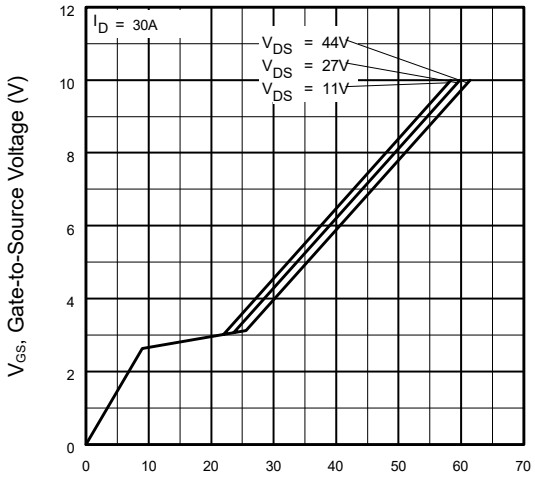
Figure 4: Typical Forward Transconductance vs. Drain Current

6.2Typical Characterisitics



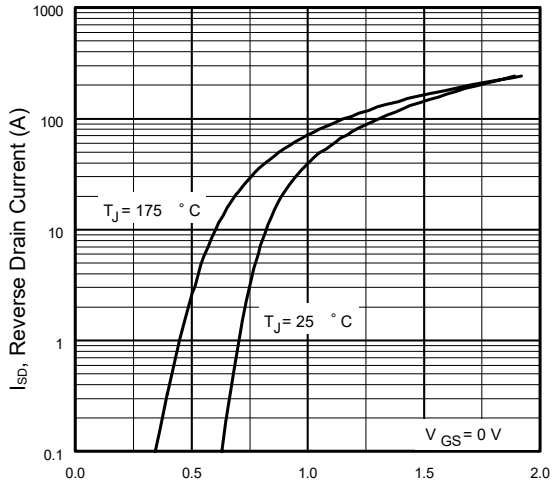
V_{DS} ,Drain-to-Source Voltage (V)

Figure 5: Typical Capacitance Vs. Drain-to-Source Voltage



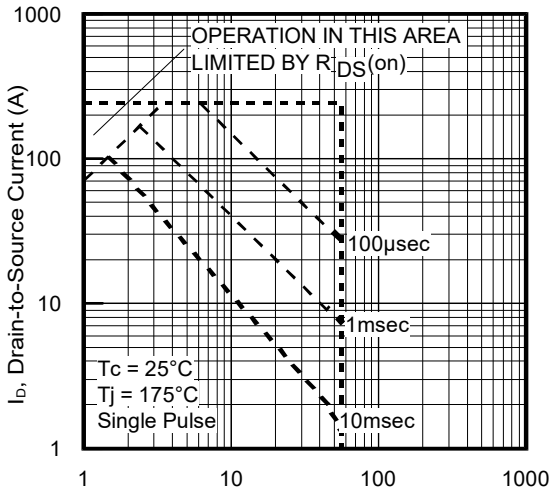
Q_G, Total Gate Charge (nC)

Figure 6: Typical Gate Charge Vs. Gate-to-Source Voltage



V_{SD}, Source-to-Drain Voltage (V)

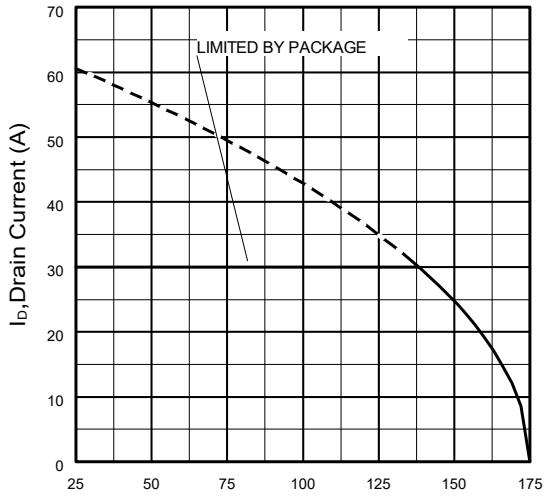
Figure 7: Typical Source-Drain Diode Forward Voltage



V_{DS}, Drain-to-Source Voltage (V)

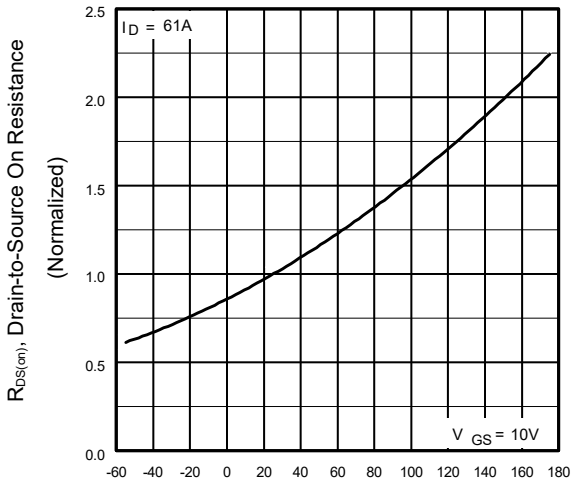
Figure 8: Maximum Safe Operating Area

6.3Typical Characterisitics



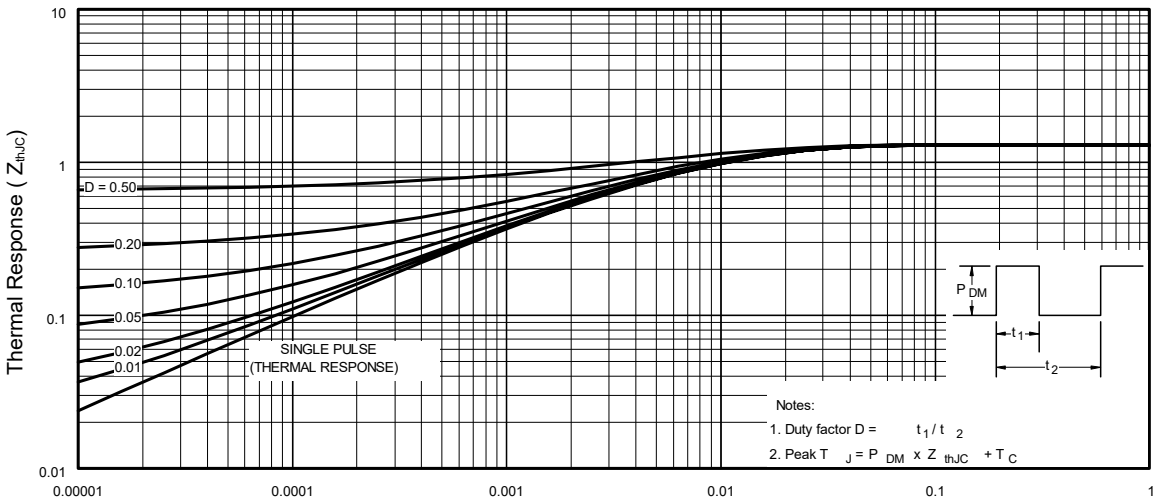
T_C, Case Temperature (°C)

Figure 9: Maximum Drain Current vs. Case Temperature



T_J, Junction Temperature (°C)

Figure 10: Normalized On-Resistance vs. Temperature



t_1 , Rectangular Pulse Duration (sec)

Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

6.4Typical Characterisitics

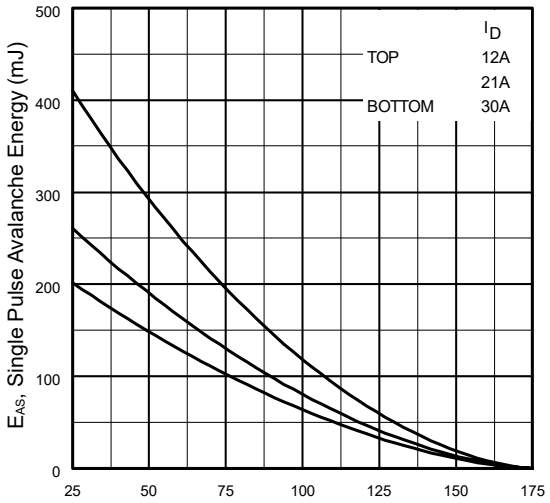


Figure 12: Maximum Avalanche Energy vs. Drain Current

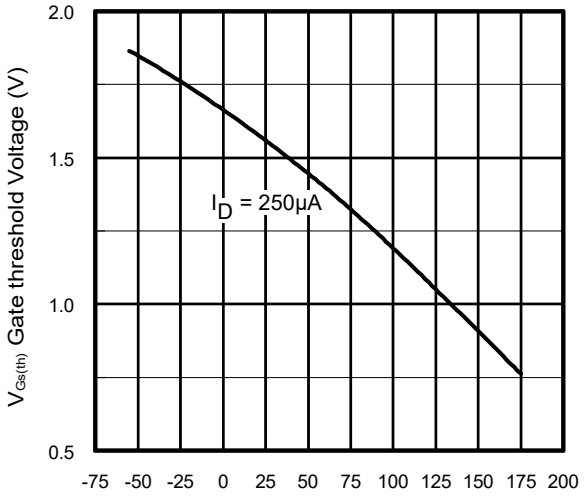


Figure 13: Threshold Voltage vs. Temperature

6.5Typical Characterisitics

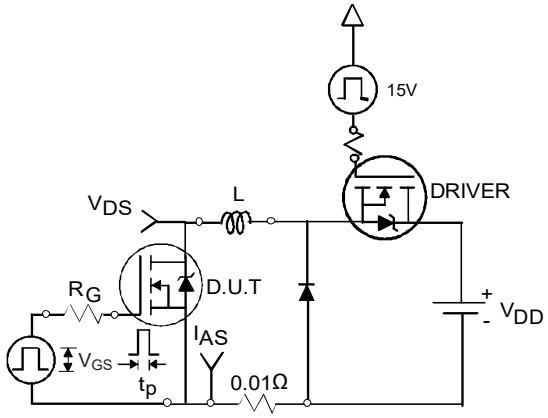


Figure 14a: Unclamped Inductive Test Circuit

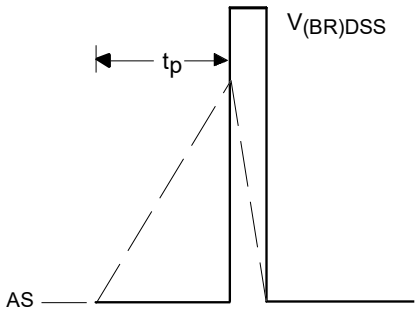


Figure 14b: Unclamped Inductive Waveforms

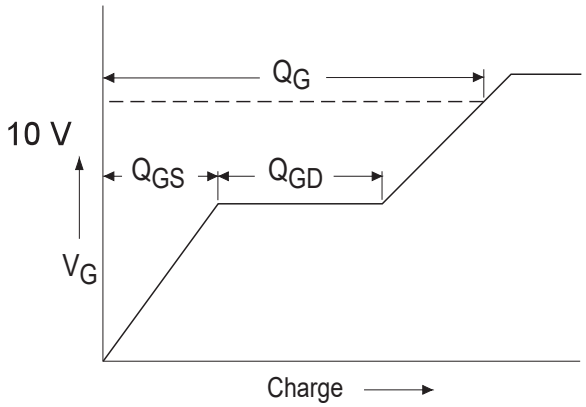


Figure 15a: Basic Gate Charge Waveform

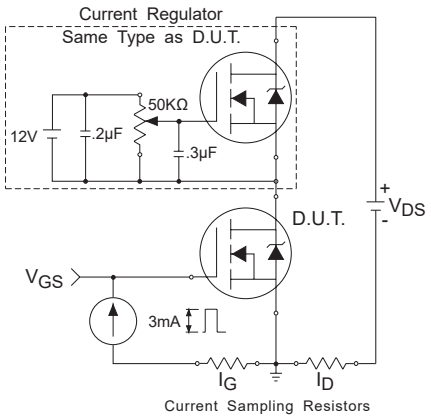


Figure 15b: Gate Charge Test Circuit

6.6Typical Characterisitics

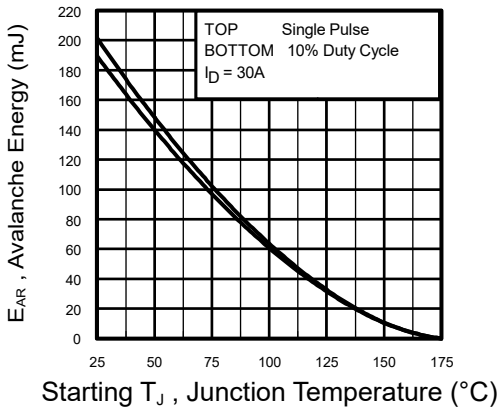


Figure 13: Maximum Avalanche Energy Vs. Temperature

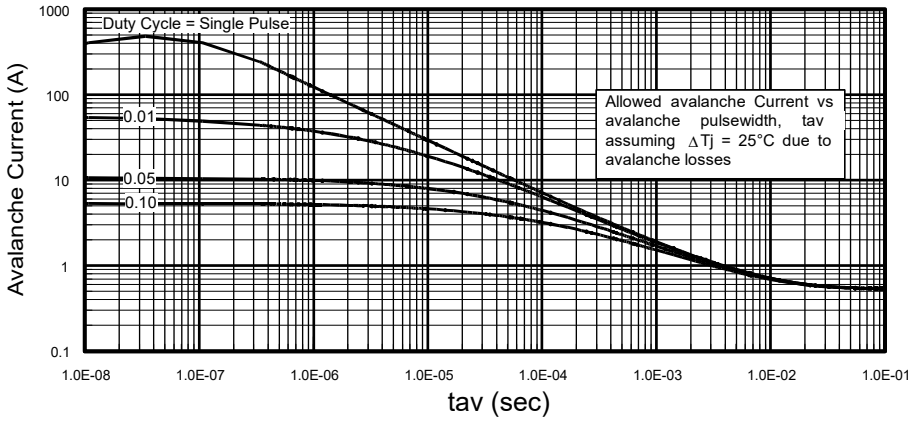


Figure 14: Typical Avalanche Current Vs.Pulsewidth

Notes on Repetitive Avalanche Curves , Figures 13, 14:

1. Avalanche failures assumption:

Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.

2. Safe operation in Avalanche is allowed as long asTjmax is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 14a, 14b.

4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. I_{av} = Allowable avalanche current.

7. ΔT = Allowable rise in junction temperature, not to exceed

T_{jmax} (assumed as 25°C in Figure 13, 14).

tav = Average time in avalanche.

D = Duty cycle in avalanche = tav ·f

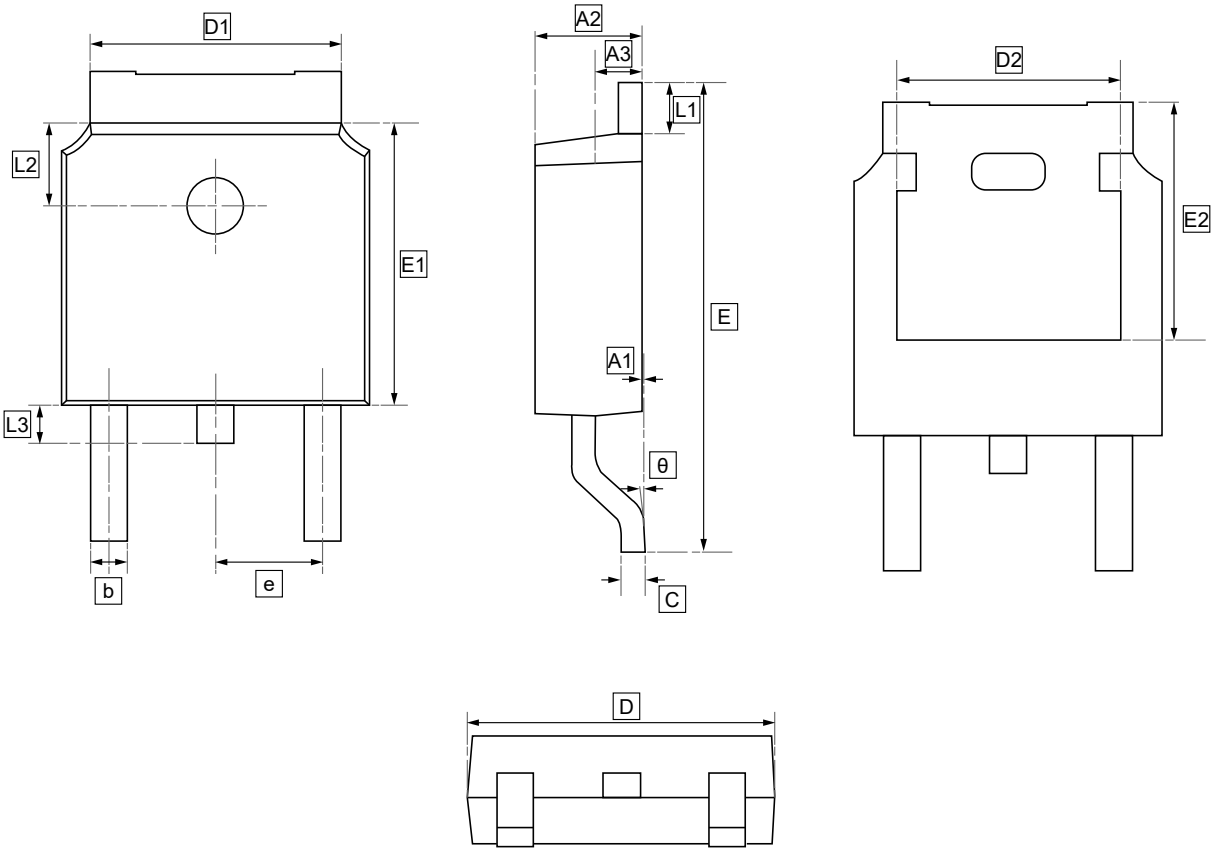
$Z_{thJC(D,\ tav)}$ = Transient thermal resistance, see figure 11.

$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$

$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$

$E_{AS\ (AR)} = PD_{\ (ave)} \cdot t_{av}$

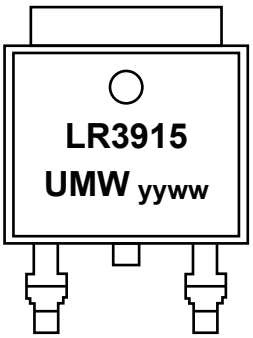
7.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

8.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRLR3915TR	TO-252	2500	Tape and reel

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