

1. Description

The SOP-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.

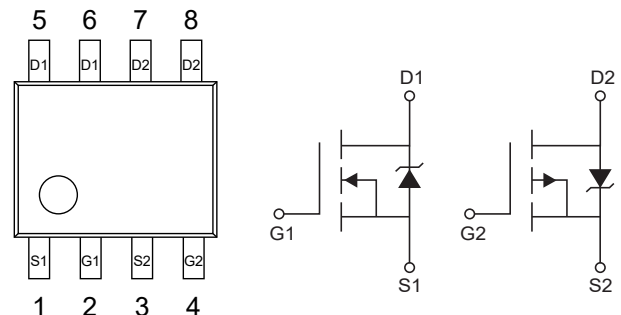
2.2 Features

- Generation V Technology Ultra
- Low On-Resistance
- Dual N and P Channel Mosfet
- Surface Mount

3. Pinning information

Pin	Symbol	Description
2,4	G	GATE
1,3	S	SOURCE
5,6,7,8	D	DRAIN

SOP-8



2.1 Features

N-Ch:

- $V_{DS(V)} = 20V$
- $R_{DS(ON)} < 53m\Omega (V_{GS} = 4.5)$
- $R_{DS(ON)} < 70m\Omega (V_{GS} = 2.7V)$

P-Ch:

- $V_{DS(V)} = -20V$
- $R_{DS(ON)} < 100m\Omega (V_{GS} = -4.5)$
- $R_{DS(ON)} < 140m\Omega (V_{GS} = -2.7V)$

- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free



4. Absolute Maximum Ratings $T_A = 25^\circ\text{C}$

Parameter		Symbol	Max n-channel	Max p-channel	Units
10 Sec. Pulse Drain Current, $V_{GS}=4.5\text{V}$	$T_A=25^\circ\text{C}$	I_D	5.7	-4.7	A
Continuous Drain Current, $V_{GS}=4.5\text{V}$	$T_A=25^\circ\text{C}$		5.2	-4.3	A
Continuous Drain Current, $V_{GS}=4.5\text{V}$	$T_A=70^\circ\text{C}$		4.1	-3.4	A
Pulsed Drain Current ①		I_{DM}	21	-17	A
Power Dissipation	$T_A=25^\circ\text{C}$	P_D	2		W
Linear Derating Factor			0.016		W/ $^\circ\text{C}$
Gate-to-Source Voltage		V_{GS}	± 12		V
Peak Diode Recovery dv/dt ②		dv/dt	5	-5	V/ns
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		$^\circ\text{C}$

5. Thermal resistance rating

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ④	$R_{\theta JA}$		62.5	$^\circ\text{C/W}$



6. Electrical Characteristics $T_J=25^\circ\text{C}$

Parameter	Symbol		Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	N-Ch	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	-20			V
		P-Ch	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	20			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/T_J$	N-Ch	$I_D=1\text{mA}$, Reference to 25°C		0.044		V/ $^\circ\text{C}$
		P-Ch	$I_D=-1\text{mA}$, Reference to 25°C		-0.012		V/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	N-Ch	$V_{GS}=4.5\text{V}$, $I_D=2.6\text{A}$ ③			53	m Ω
			$V_{GS}=2.7\text{V}$, $I_D=2.2\text{A}$ ③			70	m Ω
		P-Ch	$V_{GS}=-4.5\text{V}$, $I_D=-2.2\text{A}$ ③			100	m Ω
			$V_{GS}=-2.7\text{V}$, $I_D=-1.8\text{A}$ ③			140	m Ω
Gate Threshold Voltage	$V_{GS(th)}$	N-Ch	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	0.7			V
		P-Ch	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-0.7			V
Forward Transconductance	g_{FS}	N-Ch	$V_{DS}=15\text{V}$, $I_D=2.6\text{A}$ ③	8.3			S
		P-Ch	$V_{DS}=-15\text{V}$, $I_D=-2.2\text{A}$ ③	4			S
Drain-to-Source Leakage Current	I_{DSS}	N-Ch	$V_{DS}=16\text{V}$, $V_{GS}=0\text{V}$			1	μA
		P-Ch	$V_{DS}=-16\text{V}$, $V_{GS}=0\text{V}$			-1	μA
		N-Ch	$V_{DS}=16\text{V}$, $V_{GS}=0\text{V}$, $T_J=125^\circ\text{C}$			25	μA
		P-Ch	$V_{DS}=-16\text{V}$, $V_{GS}=0\text{V}$, $T_J=125^\circ\text{C}$			-25	μA
Gate-to-Source Forward Leakage	I_{GSS}	N-P	$V_{GS}=\pm 12\text{V}$			± 100	
Total Gate Charge	Q_g	N-Ch	N-Channel			20	nC
		P-Ch	$I_D=2.6\text{A}$, $V_{DS}=16\text{V}$			22	nC
Gate-to-Source Charge	Q_{gs}	N-Ch	$V_{GS}=4.5\text{V}$			2.2	nC
		P-Ch	P-Channel			3.3	nC
Gate-to-Drain ("Miller") Charge	Q_{gd}	N-Ch	$I_D=-2.2\text{A}$			8	nC
		P-Ch	$V_{DS}=-16\text{V}$, $V_{GS}=-4.5\text{V}$			9	nC
Turn-On Delay Time	$t_{D(on)}$	N-Ch	N-Channel		9		ns
		P-Ch	$V_{DD}=10\text{V}$, $I_D=2.6\text{A}$		8.4		ns
Rise Time	t_r	N-Ch	$R_G=6\Omega$, $R_D=3.8\Omega$		42		ns
		P-Ch			26		ns



20V N-Channel MOSFET
-20V P-Channel MOSFET

Turn-Off Delay Time	$t_{D(off)}$	N-Ch	P-Channel $V_{DD}=-10V, I_D=-2.2A$ $R_G=6\Omega, R_D=4.5\Omega$		32		ns	
		P-Ch			51		ns	
Fall Time	t_f	N-Ch			51		ns	
		P-Ch			33		ns	
Internal Drain inductance	L_D	N-Ch	Between lead tip and center of die contact		4		nH	
Internal Source inductance	L_S	P-Ch			6		nH	
Input Capacitance	C_{iss}	N-Ch	N-Channel $V_{GS}=0V, V_{DS}=15V, f=1.0MHz$		660		pF	
		P-Ch			610		pF	
Output Capacitance	C_{oss}	N-Ch			280		pF	
		P-Ch			310		pF	
Reverse Transfer Capacitance	C_{rss}	N-Ch	P-Channel		140		pF	
		P-Ch	$V_{GS}=0V, V_{DS}=-15V, f=1.0MHz$		170			
Source-Drain Ratings and Characteristics								
Continuous Source Current (Body Diode)	I_S	N-Ch				2.5	A	
		P-Ch				-2.5		
Pulsed Source Current (Body Diode) ①	I_{SM}	N-Ch				21		
		P-Ch				-17		
Diode Forward Voltage	V_{SD}	N-Ch	$T_J=25^{\circ}C, I_S=1.8A, V_{GS}=0V$ ③			1	V	
		P-Ch	$T_J=25^{\circ}C, I_S=-1.8A, V_{GS}=0V$ ③			-1	V	
Reverse Recovery Time	t_{rr}	N-Ch	N-Channel: $T_J=25^{\circ}C$ $I_F=2.6A, dI/dt=100A/\mu s$		29	44	ns	
		P-Ch			56	84	ns	
Reverse Recovery Charge	Q_{rr}	N-Ch		P-Channel: $T_J=25^{\circ}C$ ③ $I_F=-2.2A, dI/dt=100A/\mu s$		22	33	nC
		P-Ch				71	110	nC
Forward Turn-On Time	t_{on}	N-Ch	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)					
		P-Ch						

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 23)

② N-Channel $I_{SD} \leq 2.6A, di/dt \leq 100A/\mu s, V_{DD} \leq V_{BR(DSS)}, T_J \leq 150^\circ C$.

P-Channel $I_{SD} \leq -2.2A, di/dt \leq 50A/\mu s, V_{DD} \leq V_{BR(DSS)}, T_J \leq 150^\circ C$.

③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

④ Surface mounted on FR-4 board, $t_s \leq 10sec$.



20V N-Channel MOSFET
-20V P-Channel MOSFET

7.1 Typical Characteristics

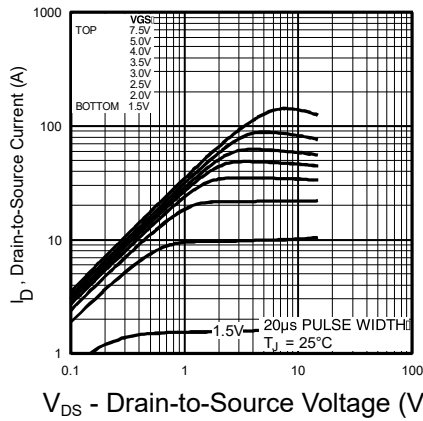


Fig 1. Typical Output Characteristics

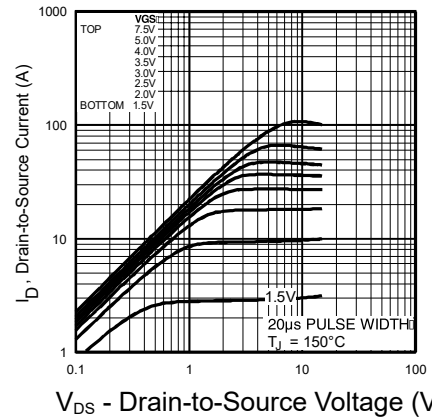


Fig 2. Typical Output Characteristics

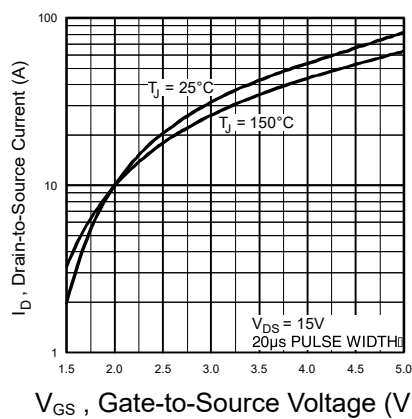


Fig 3. Typical Transfer Characteristics

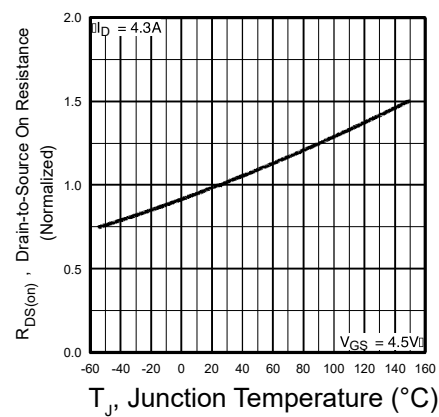
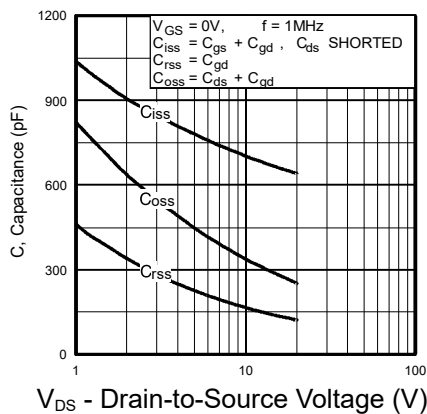
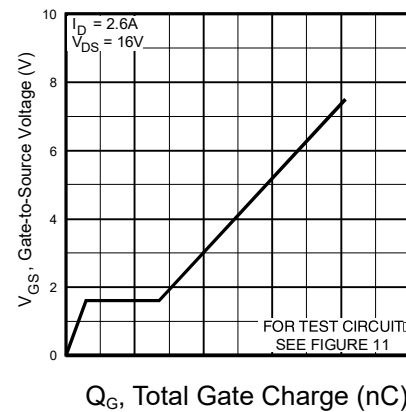


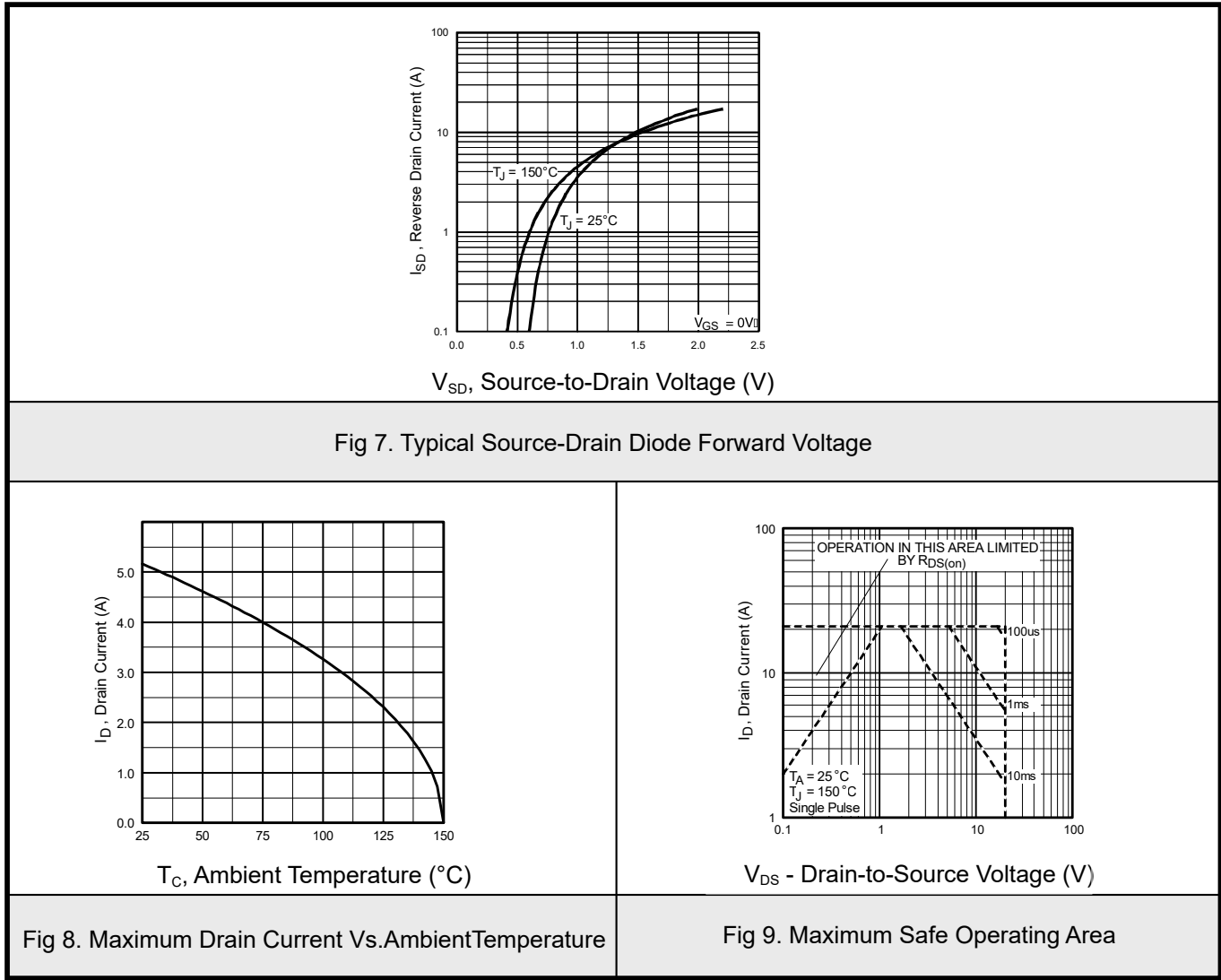
Fig 4. Normalized On-Resistance Vs. Temperature

Fig 5. Typical Capacitance Vs.
Drain-to-Source VoltageFig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage



20V N-Channel MOSFET
-20V P-Channel MOSFET

7.2Typical Characterisitics





20V N-Channel MOSFET
-20V P-Channel MOSFET

7.3 Typical Characteristics

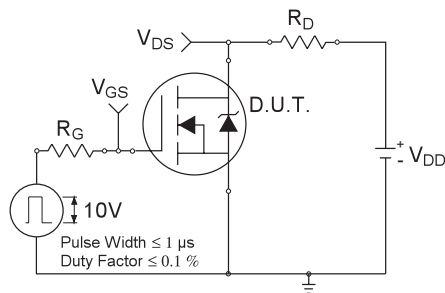


Fig 10a. Switching Time Test Circuit

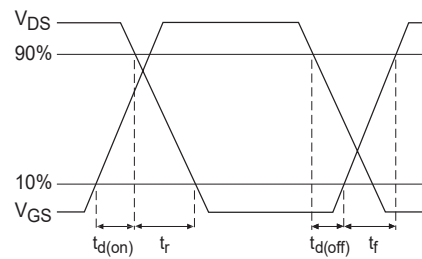


Fig 10b. Switching Time Waveforms

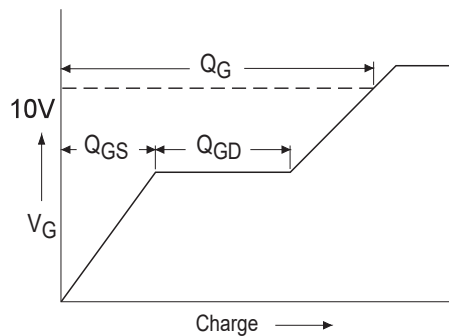


Fig 11a. Basic Gate Charge Waveform

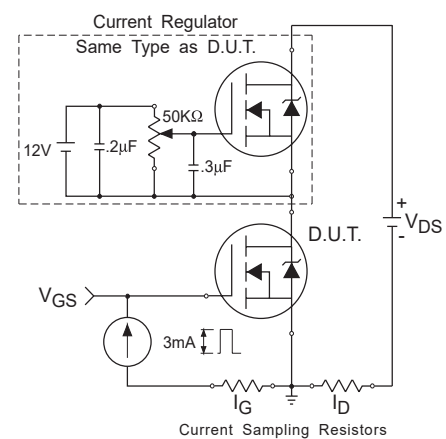


Fig 11b. Gate Charge Test Circuit



20V N-Channel MOSFET
-20V P-Channel MOSFET

7.4 Typical Characteristics

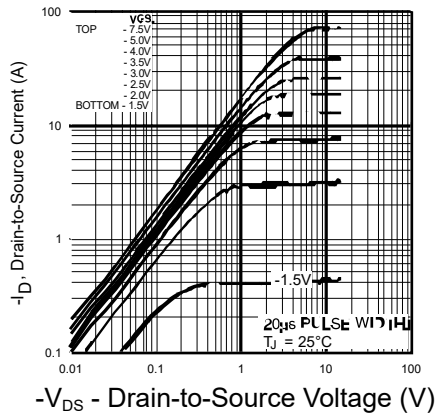


Fig 12. Typical Output Characteristics

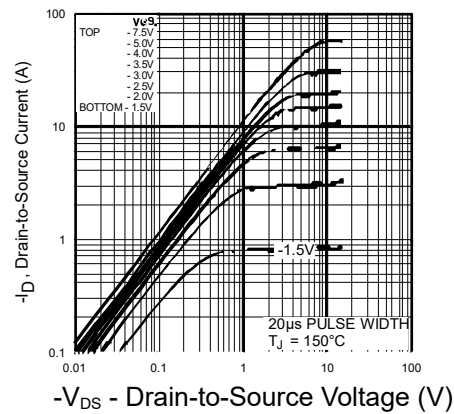


Fig 13. Typical Output Characteristics

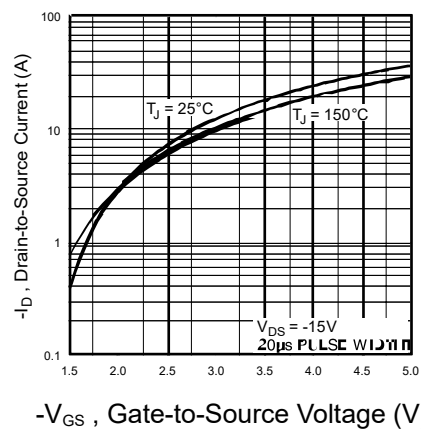


Fig 14. Typical Transfer Characteristics

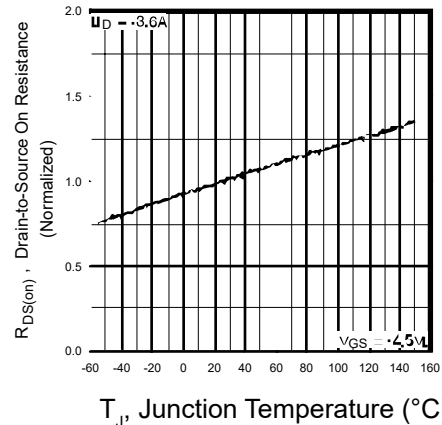
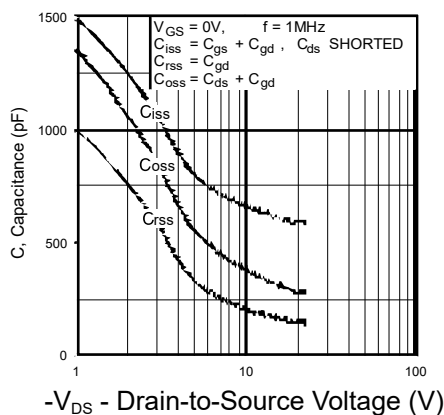
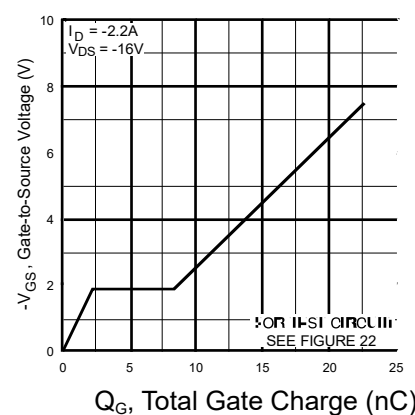


Fig 15. Normalized On-Resistance Vs. Temperature

Fig 16. Typical Capacitance Vs.
Drain-to-Source VoltageFig 17. Typical Gate Charge Vs.
Gate-to-Source Voltage



20V N-Channel MOSFET
-20V P-Channel MOSFET

7.5Typical Characterisitics

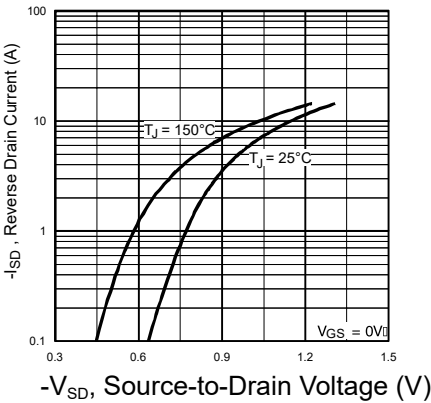


Fig 18. Typical Source-Drain Diode Forward Voltage

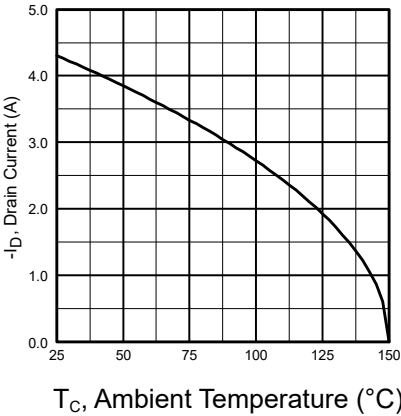


Fig 19. Maximum Drain Current Vs.AmbientTemperature

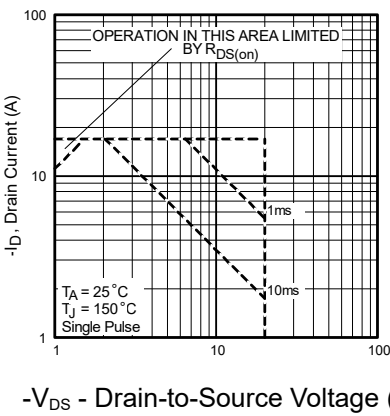


Fig 20. Maximum Safe Operating Area



20V N-Channel MOSFET
-20V P-Channel MOSFET

7.6 Typical Characteristics

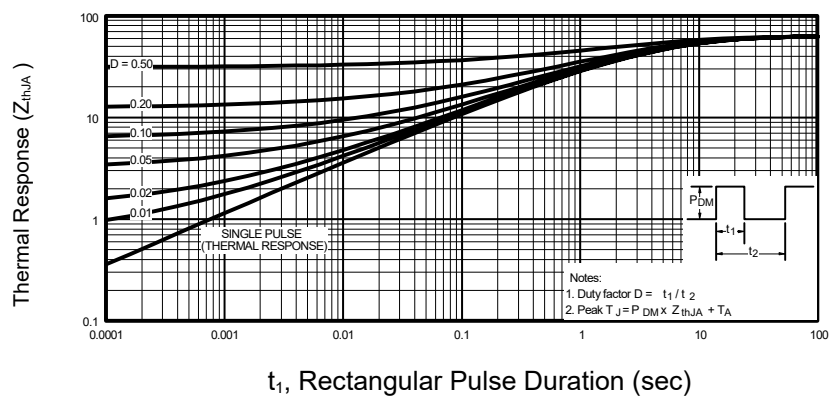


Fig 23. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



20V N-Channel MOSFET
-20V P-Channel MOSFET

7.7 Typical Characteristics

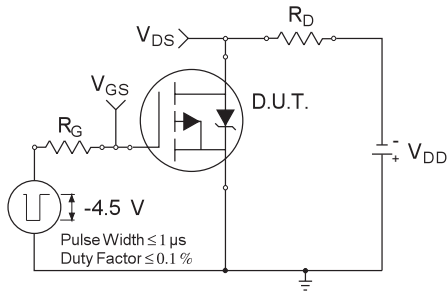


Fig 21a. Switching Time Test Circuit

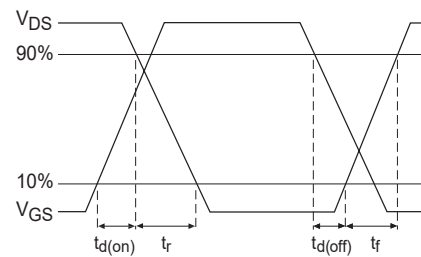


Fig 21b. Switching Time Waveforms

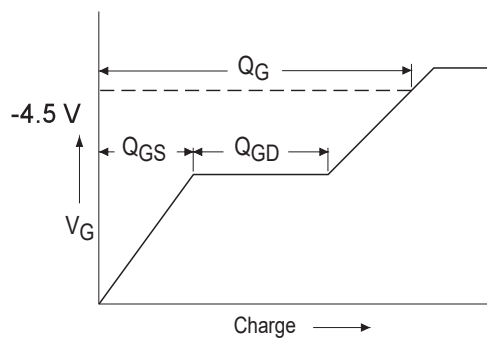


Fig 22a. Basic Gate Charge Waveform

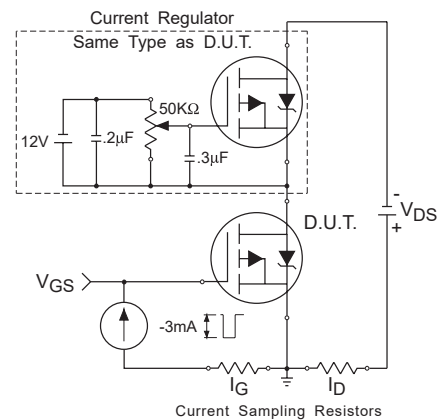
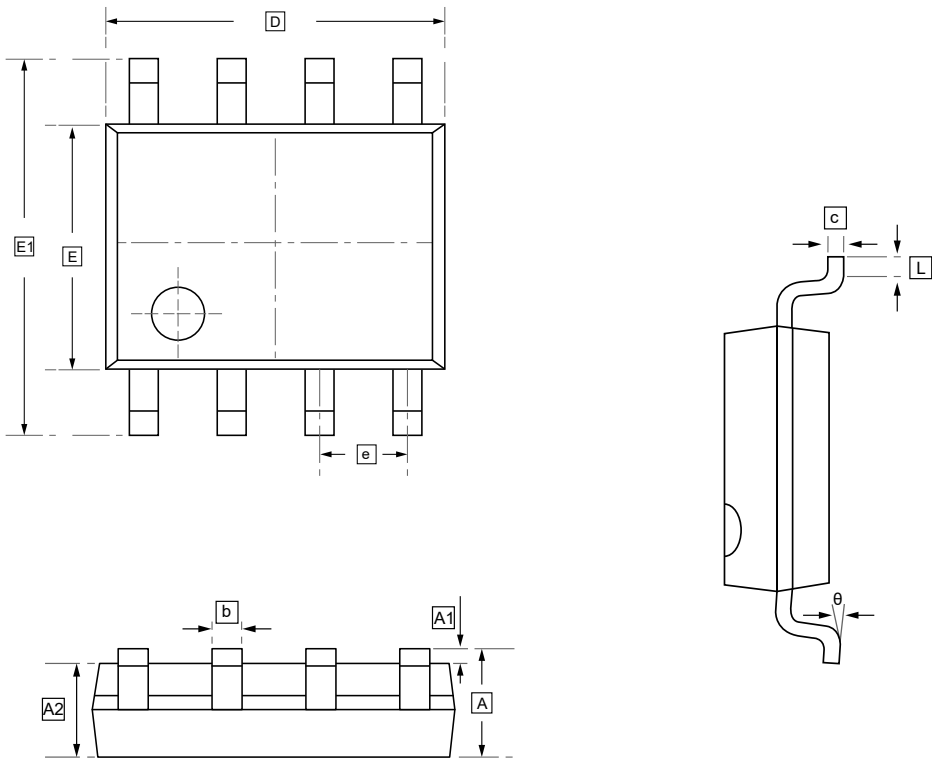


Fig 22b. Gate Charge Test Circuit



8.SOP-8 Package Outline Dimensions



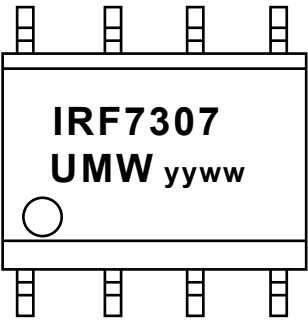
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°



20V N-Channel MOSFET
-20V P-Channel MOSFET

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRF7307TR	SOP-8	3000	Tape and reel



10.Disclaimer

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