

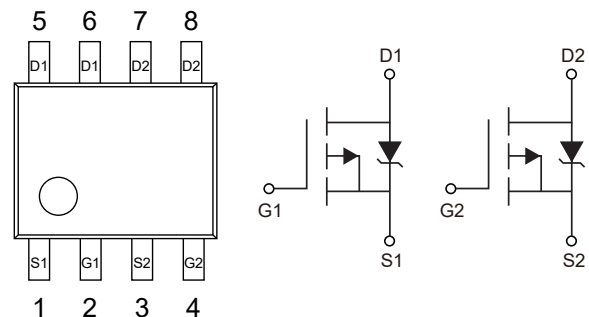
1.Features

- $V_{DS(V)} = -20V$
- $R_{DS(ON)} < 18m\Omega (V_{GS} = -4.5V)$
- $R_{DS(ON)} < 26m\Omega (V_{GS} = -2.5V)$
- Trench Technology
- Ultra Low On-Resistance
- Low Profile ($< 1.1mm$)
- Available in Tape & Reel
- 2.5V Rated
- Lead-Free

2.Pinning information

Pin	Symbol	Description
2,4	G	GATE
1,3	S	SOURCE
5,6,7,8	D	DRAIN

SOP-8



3.Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	-20	V
Continuous Drain Current, $V_{GS} = -4.5V$	I_D	-9	A
Continuous Drain Current, $V_{GS} = -4.5V$		-7.1	A
Pulsed Drain Current ①	I_{DM}	-71	A
Maximum Power Dissipation ③	P_D	2	W
Maximum Power Dissipation ③		1.3	W
Linear Derating Factor		16	mW/°C
Gate-to-Source Voltage	V_{GS}	± 12	V
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

5.Thermal resist ance rating

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ③	$R_{\theta JA}$		62.5	°C/W



6. Electrical Characteristics $T_J=25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-20			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/T_J$	$I_D=-1\text{mA}$, Reference to 25°C		-0.02		V/ $^{\circ}\text{C}$
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=-4.5\text{V}$, $I_D=-9\text{A}$ ②			18	m Ω
		$V_{GS}=-2.5\text{V}$, $I_D=-7.7\text{A}$ ②			26	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-0.45		-1	V
Forward Transconductance	g_{FS}	$V_{DS}=-10\text{V}$, $I_D=-9\text{A}$	19			S
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS}=-16\text{V}$, $V_{GS}=0\text{V}$			-1	μA
		$V_{DS}=-16\text{V}$, $V_{GS}=0\text{V}$, $T_J=125^{\circ}\text{C}$			-25	
Gate-to-Source Forward Leakage	I_{GSS}	$V_{GS}=-12\text{V}$			-100	nA
Gate-to-Source Reverse Leakage		$V_{GS}=12\text{V}$			100	
Total Gate Charge	Q_g	$I_D=-9\text{A}$		42	63	nC
Gate-to-Source Charge	Q_{gs}	$V_{DS}=-16\text{V}$		7.1	11	
Gate-to-Drain ("Miller") Charge	Q_{gd}	$V_{GS}=-5\text{V}$		12	18	
Turn-On Delay Time	$t_{D(on)}$	$V_{DD}=-10\text{V}$		17		ns
Rise Time	t_r	$I_D=-1\text{A}$		36		ns
Turn-Off Delay Time	$t_{D(off)}$	$R_G=6\Omega$		170		ns
Fall Time	t_f	$R_D=10\Omega$ ②		190		ns
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}$		2940		pF
Output Capacitance	C_{oss}	$V_{DS}=-15\text{V}$		630		pF
Reverse Transfer Capacitance	C_{rss}	$f=1.0\text{MHz}$		420		pF



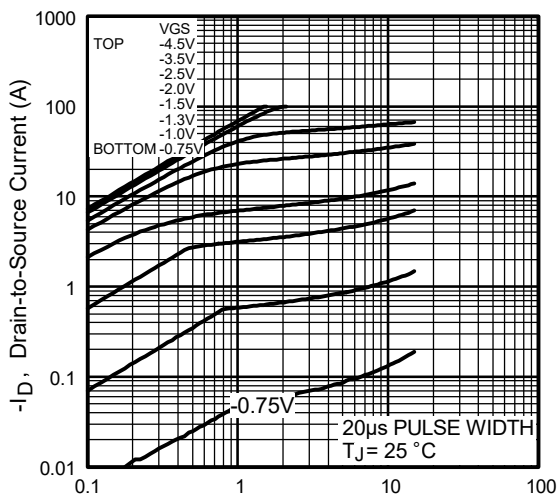
Source-Drain Ratings and Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			-2	A
Pulsed Source Current (Body Diode) ①	I_{SM}				-71	
Diode Forward Voltage	V_{SD}	$T_J=25^{\circ}\text{C}, I_S=-2\text{A}, V_{GS}=0\text{V}$ ②			-1.2	V
Reverse Recovery Time	t_{rr}	$T_J=25^{\circ}\text{C}, I_F=-2\text{A}$		180	270	ns
Reverse Recovery Charge	Q_{rr}	$di/dt=-100\text{A}/\mu\text{s}$ ②		300	450	nC

Notes:

- ① Repetitive rating; pulse width limited by max.junction temperature.
- ② Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ③ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.

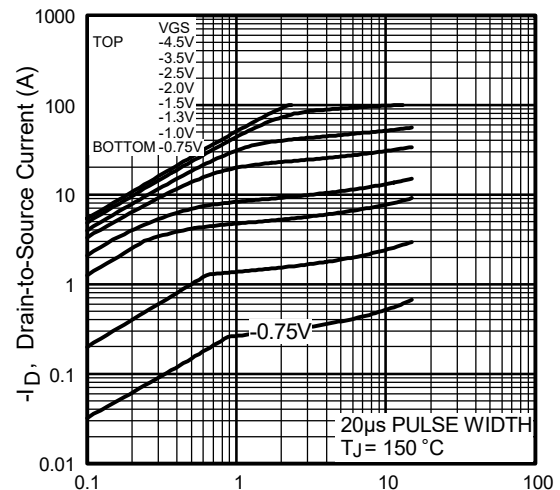


7.1 Typical Characteristics



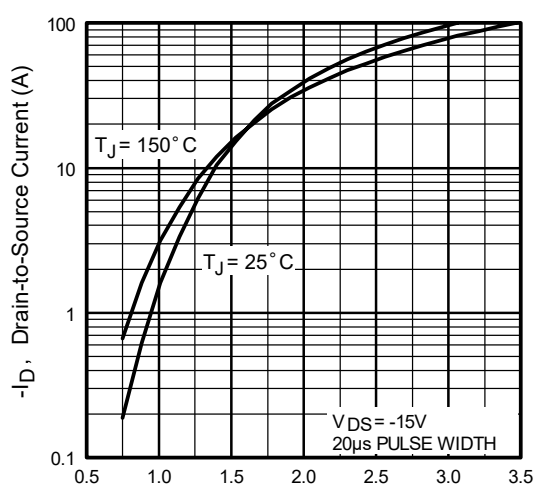
$-V_{DS}$ - Drain-to-Source Voltage (V)

Fig 1. Typical Output Characteristics



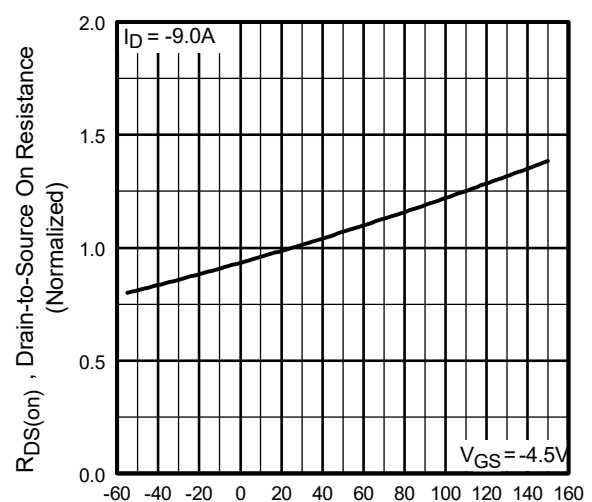
$-V_{DS}$ - Drain-to-Source Voltage (V)

Fig 2. Typical Output Characteristics



$-V_{GS}$, Gate-to-Source Voltage (V)

Fig 3. Typical Transfer Characteristics

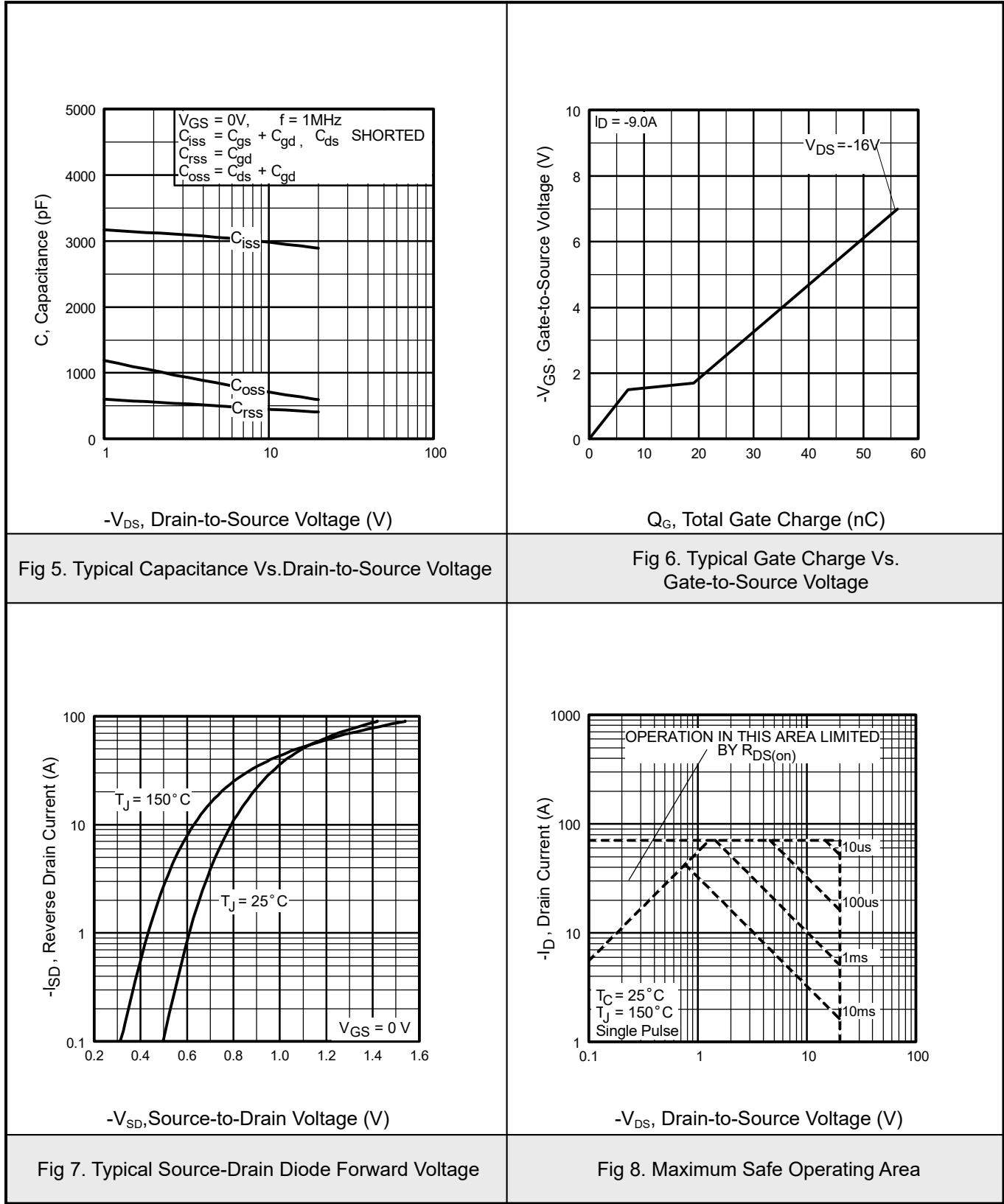


T_J , Junction Temperature(°C)

Fig 4. Normalized On-Resistance Vs. Temperature



7.2Typical Characterisitics





7.3 Typical Characteristics

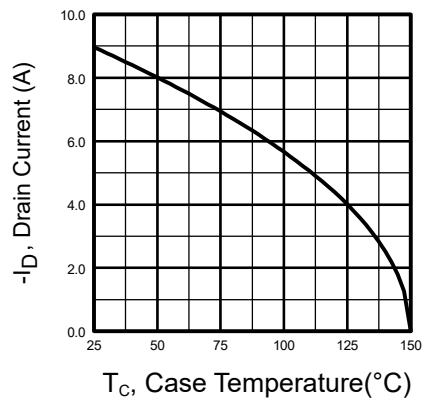


Fig 9. Maximum Drain Current Vs. Case Temperature

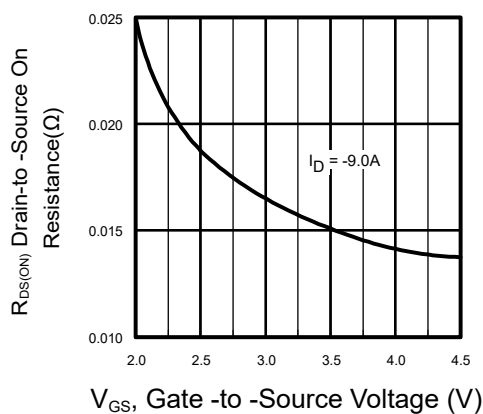


Fig 10. Typical On-Resistance Vs. Gate Voltage

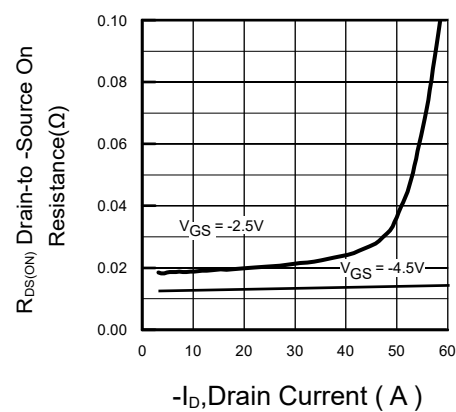


Fig 11. Typical On-Resistance Vs. Drain Current

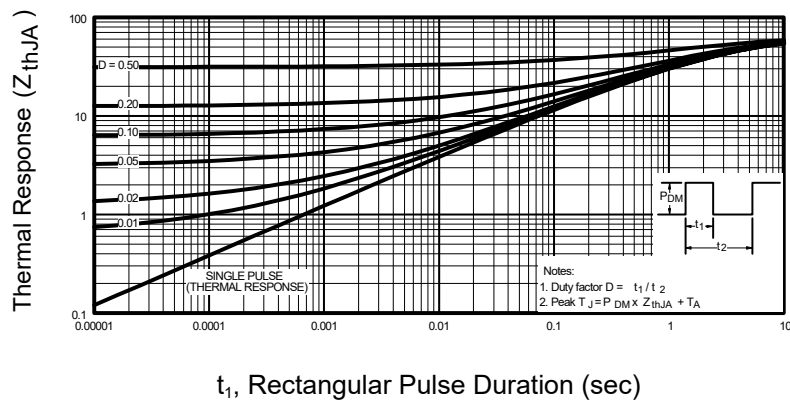


Fig 12. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



7.3Typical Characterisitics

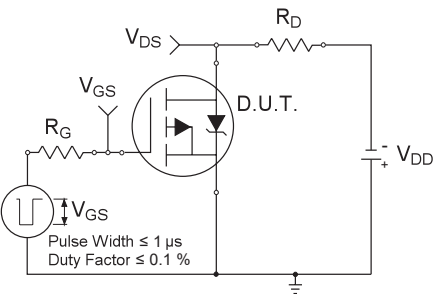


Fig 13a. Switching Time Test Circuit

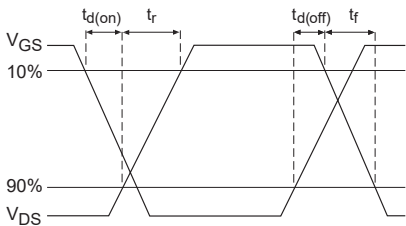


Fig 13b. Switching Time Waveforms

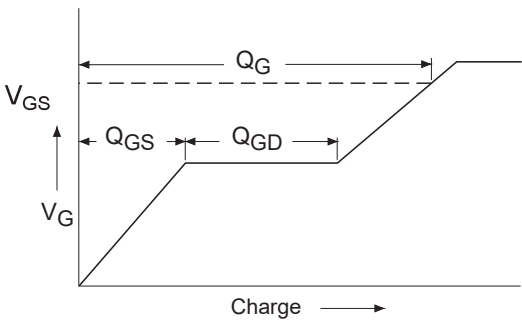


Fig 14a. Basic Gate Charge Waveform

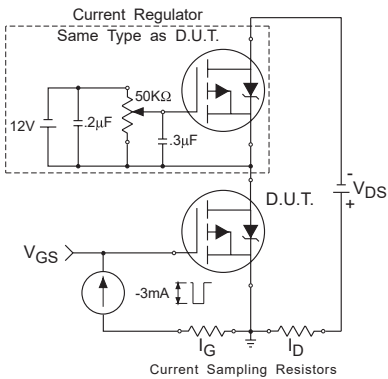
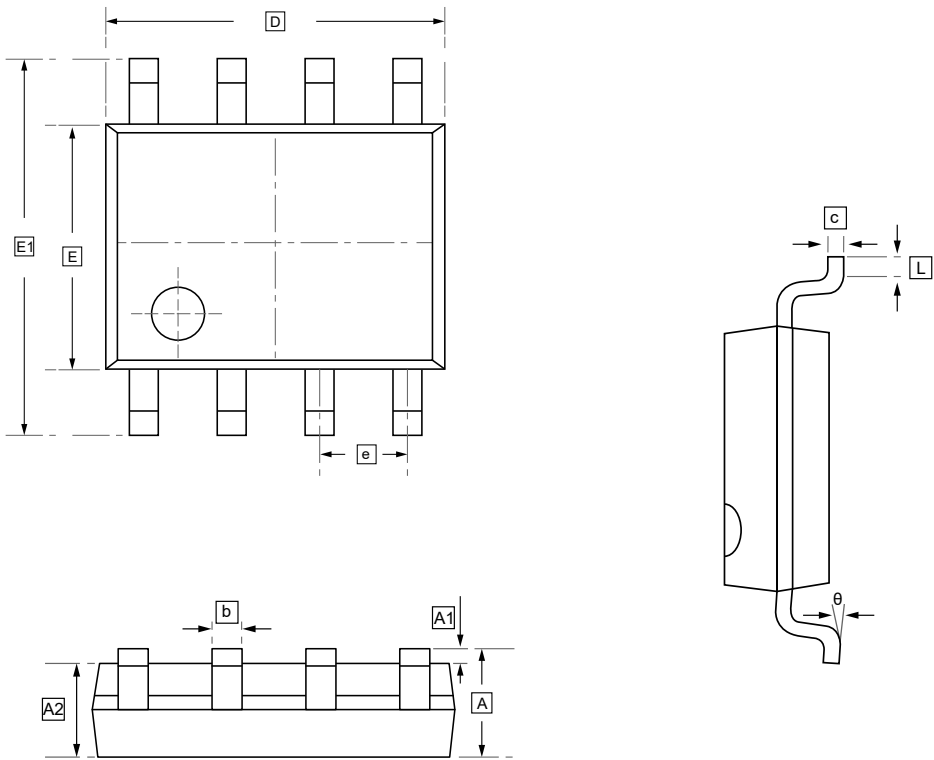


Fig 14b. Gate Charge Test Circuit



8.SOP-8 Package Outline Dimensions

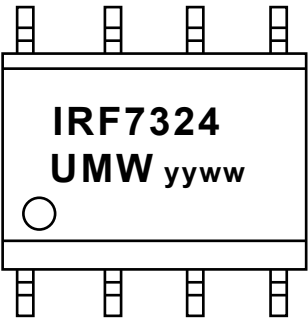


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°



9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRF7324TR	SOP-8	3000	Tape and reel



10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

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