

1.Description

The SOP-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications.

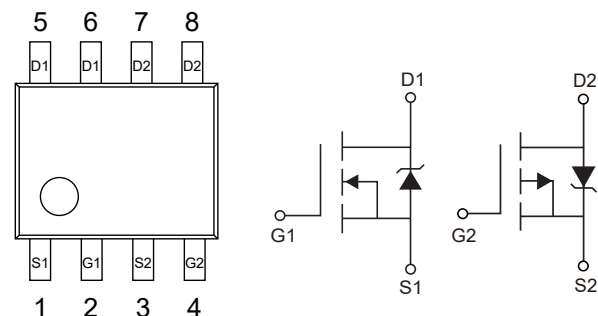
2.2Features(N-Ch)

- $V_{DS(V)}=30V$
- $R_{DS(ON)}=0.029\Omega$

3.Pinning information

Pin	Symbol	Description
2,4	G	GATE
1,3	S	SOURCE
5,6,7,8	D	DRAIN

SOP-8



4.Absolute Maximum Ratings

Parameter		Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	± 20	± 20	V
Continuous Drain Current ⑤	$T_A=25^{\circ}C$	I_D	6.5	-4.9	A
	$T_A=70^{\circ}C$		5.2	-3.9	A
Pulsed Drain Current		I_{DM}	30	-30	A
Continuous Source Current (Diode Conduction)		I_S	2.5	-2.5	A



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Maximum Power Dissipation ⑤	$T_A = 25^{\circ}\text{C}$	P_D	2	2	W
	$T_A = 70^{\circ}\text{C}$		1.3	1.3	W
Single Pulse Avalanche Energy		E_{AS}	82	140	mJ
Avalanche Current		I_{AR}	4	-2.8	A
Repetitive Avalanche Energy		E_{AR}	0.2	0.2	mJ
Peak Diode Recovery dv/dt ②		dv/dt	5	-5	V/ns
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	-55 to 150	$^{\circ}\text{C}$

5. Thermal Characteristics

Parameter	Symbol	Max.	Units
Maximum Junction-to-Ambient ⑤	$R_{\theta JA}$	62.5	$^{\circ}\text{C/W}$



6. Electrical Characteristics $T_J=25^{\circ}\text{C}$

Parameter	Symbol		Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	N-Ch	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
		P-Ch	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-30			V
Breakdown Voltage Temp Coefficient	$\frac{\Delta V_{(BR)DSS}}{\Delta T_J}$	N-Ch	$I_D=1\text{mA}$, Reference to 25°C		0.022		$\text{V}/^{\circ}\text{C}$
		P-Ch	$I_D=-1\text{mA}$, Reference to 25°C		0.022		$\text{V}/^{\circ}\text{C}$
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	N-Ch	$V_{GS}=10\text{V}$, $I_D=5.8\text{A}$ ④		23	31	$\text{m}\Omega$
		P-Ch	$V_{GS}=4.5\text{V}$, $I_D=4.7\text{A}$ ④		32	48	$\text{m}\Omega$
		N-Ch	$V_{GS}=-10\text{V}$, $I_D=-4.9\text{A}$ ④		42	60	$\text{m}\Omega$
		P-Ch	$V_{GS}=-4.5\text{V}$, $I_D=-3.6\text{A}$ ④		76	100	$\text{m}\Omega$
Gate Threshold Voltage	$V_{GS(th)}$	N-Ch	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1			V
		P-Ch	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1			V
Forward Transconductance	g_{fs}	N-Ch	$V_{GS}=15\text{V}$, $I_D=5.8\text{A}$ ④		14		S
		P-Ch	$V_{GS}=-15\text{V}$, $I_D=-4.9\text{A}$ ④		7.7		S
Drain-to-Source Leakage Current	I_{DSS}	N-Ch	$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$			1	μA
			$V_{DS}=-24\text{V}$, $V_{GS}=0\text{V}$			-1	μA
		P-Ch	$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$, $T_J=55^{\circ}\text{C}$			25	μA
			$V_{DS}=-24\text{V}$, $V_{GS}=0\text{V}$, $T_J=55^{\circ}\text{C}$			-25	μA
Gate-to-Source Forward Leakage	I_{GSS}	N-P	$V_{GS}=\pm 20\text{V}$			± 100	
Total Gate Charge	Q_g	N-Ch	N-Ch: ④		22	33	nC
		P-Ch			23	34	nC
Gate-to-Source Charge	Q_{gs}	N-Ch	$I_D=5.8\text{A}$, $V_{DS}=15\text{V}$, $V_{GS}=10\text{V}$		2.6	3.9	nC
		P-Ch	P-Ch:		3.8	5.7	nC
Gate-to-Drain ("Miller") Charge	Q_{gd}	N-Ch	$I_D=-4.9\text{A}$, $V_{DS}=-15\text{V}$, $V_{GS}=-10\text{V}$		6.4	9.6	nC
		P-Ch			5.9	8.9	nC
Turn-On Delay Time	$t_{D(on)}$	N-Ch	N-Ch: ④		8.1	12	ns
		P-Ch			13	19	ns
Rise Time	t_r	N-Ch	$V_{DD}=15\text{A}$, $I_D=1\text{A}$		8.9	13	ns
		P-Ch	$R_G=6\Omega$, $R_D=15\Omega$		13	20	ns



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Turn-Off Delay Time	$t_{D(off)}$	N-Ch	P-Ch: ④ $V_{DD}=-15A, I_D=-1A$ $R_G=6\Omega, R_D=15\Omega$		26	39	ns
		P-Ch			34	51	ns
Fall Time	t_f	N-Ch			17	26	ns
		P-Ch			32	48	ns
Input Capacitance	C_{iss}	N-P	N-Ch: $V_{GS}=0V, V_{DS}=25V, f=1MHz$ P-Ch: $V_{GS}=0V, V_{DS}=-25V, f=1MHz$		650		pF
		N-P			710		pF
Output Capacitance	C_{oss}	N-Ch			320		pF
		P-Ch			380		pF
Reverse Transfer Capacitance	C_{rss}	N-Ch			130		pF
		P-Ch			180		pF
Continuous Source Current (Body Diode)	I_S	N-Ch				2.5	A
		P-Ch				-2.5	A
Pulsed Source Current (Body Diode) ①	I_{SM}	N-Ch				30	A
		P-Ch				-30	A
Diode Forward Voltage	V_{SD}	N-Ch	$T_J=25^\circ C, I_S=1.7A, V_{GS}=0V$ ③		0.78	1	V
		P-Ch	$T_J=25^\circ C, I_S=-1.7A, V_{GS}=0V$ ③		-0.78	-1	V
Reverse Recovery Time	t_{rr}	N-Ch	N-Ch: $T_J=25^\circ C$ $I_F=1.7A, di/dt=100A/\mu s$ P-Ch: $T_J=25^\circ C$ $I_F=-1.7A, di/dt=100A/\mu s$ ④		45	68	ns
		P-Ch			44	66	ns
Reverse Recovery Charge	Q_{rr}	N-Ch			58	87	nC
		P-Ch			42	63	nC

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 22)
- ② N-Channel $I_{SD} \leq 4A, di/dt \leq 74A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ C$.
P-Channel $I_{SD} \leq -2.8A, di/dt \leq 150A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ C$.
- ③ N-Channel Starting $T_J=25^\circ C, L=10mH, R_G=25\Omega, I_{AS}=4.0A$. (See Figure 12)
P-Channel Starting $T_J=25^\circ C, L=35mH, R_G=25\Omega, I_{AS}=-2.8A$.
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Surface mounted on FR-4 board, $t_s \leq 10sec$.



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7.1Typical Characterisitics (N-Channel)

Figure 1: Typical Output Characteristics	Figure 2: Typical Output Characteristics
Figure 3: Typical Output Characteristics	Figure 4: Typical Source-Drain Diode Forward Voltage
Figure 5: Normalized On-Resistance VS. Temperature	Figure 6: Typical On-Resistance Vs. DrainCurrent



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7.2 Typical Characteristics (N-Channel)

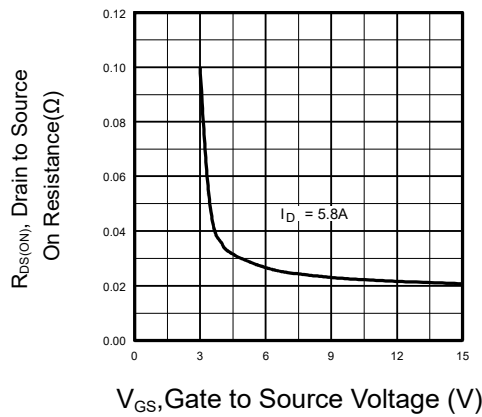


Figure 7: Typical On-Resistance Vs. Gate Voltage

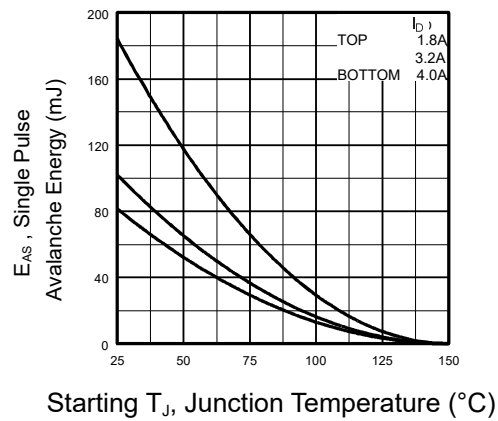


Figure 8: Maximum Avalanche Energy Vs. Drain Current

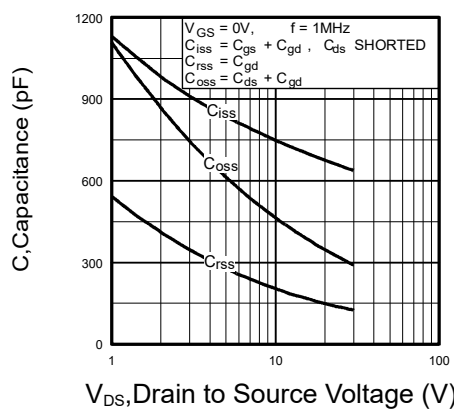


Figure 9: Typical Capacitance Vs. Drain-to-Source Voltage

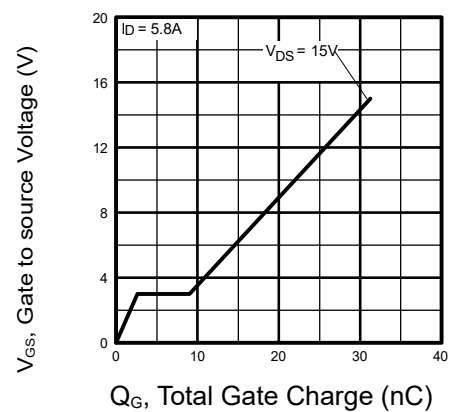


Figure 10: Typical Gate Charge Vs. Gate-to-Source Voltage

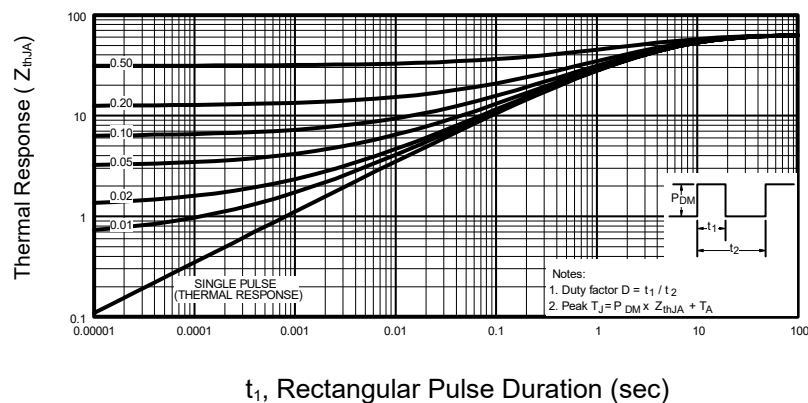


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



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7.3 Typical Characteristics (P-Channel)

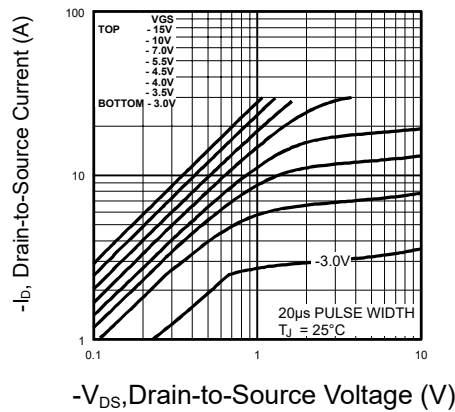


Figure 12: Typical Output Characteristics

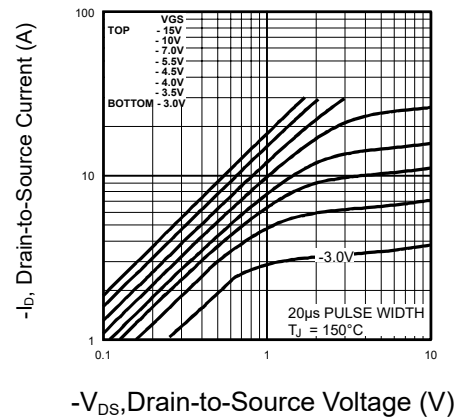


Figure 13: Typical Output Characteristics

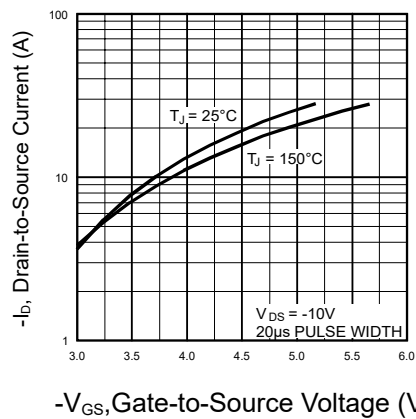


Figure 14: Typical Output Characteristics

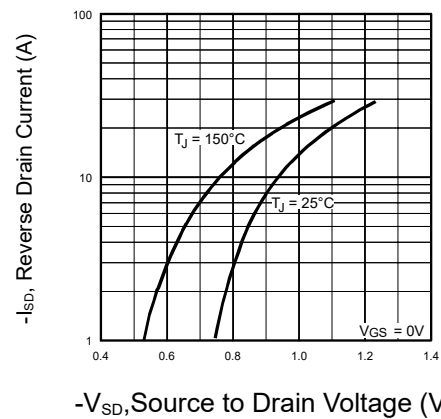


Figure 15: Typical Source-Drain Diode Forward Voltage

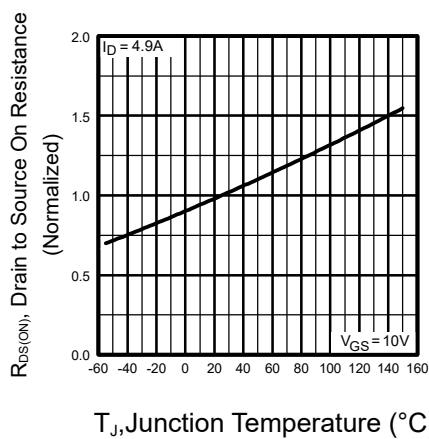


Figure 16: Normalized On-Resistance VS. Temperature

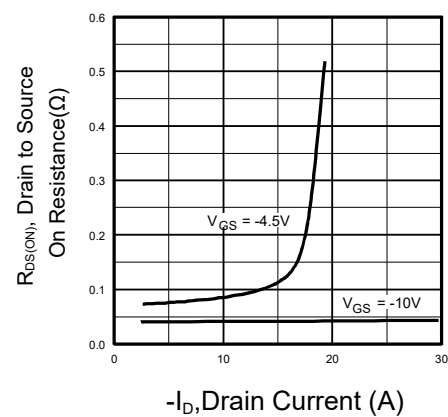


Figure 17: Typical On-Resistance Vs. Drain Current



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7.4 Typical Characteristics (P-Channel)

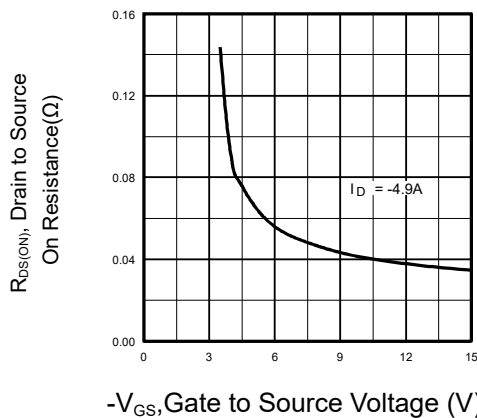


Figure 18: Typical On-Resistance Vs. Gate Voltage

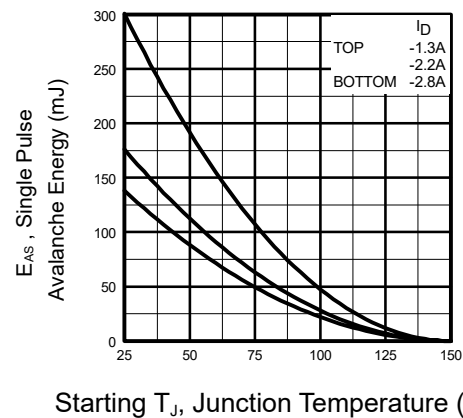


Figure 19: Maximum Avalanche Energy Vs. Drain Current

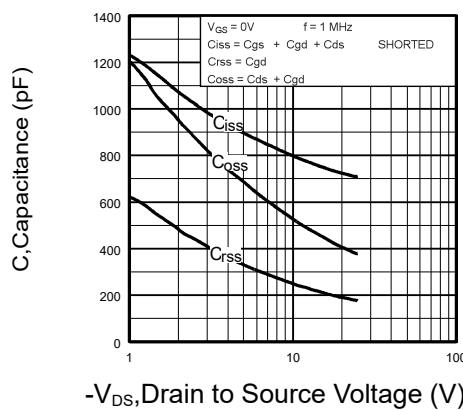


Figure 20: Typical Capacitance Vs. Drain-to-Source Voltage

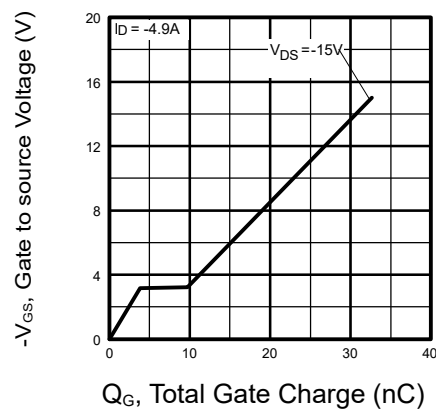


Figure 21: Typical Gate Charge Vs. Gate-to-Source Voltage

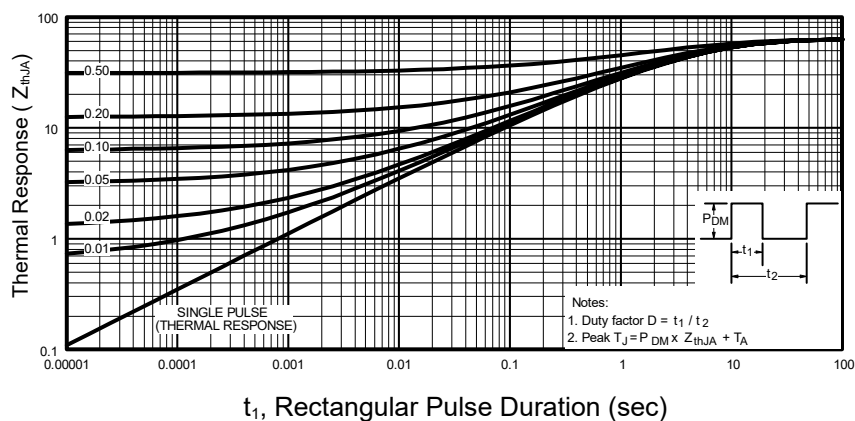
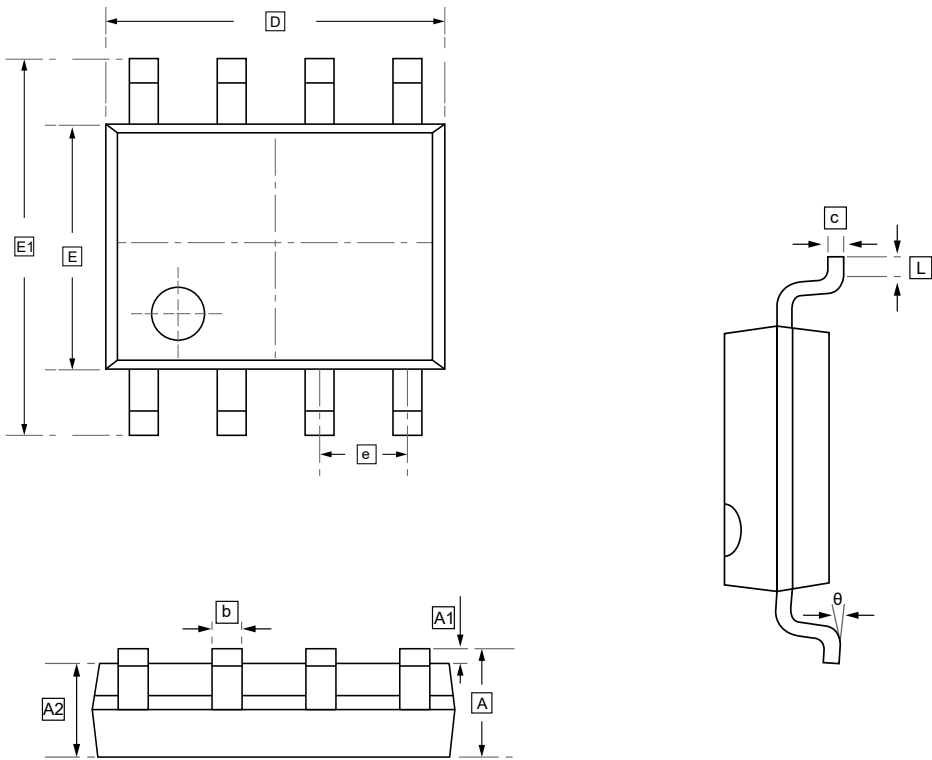


Figure 22: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



8.SOP-8 Package Outline Dimensions



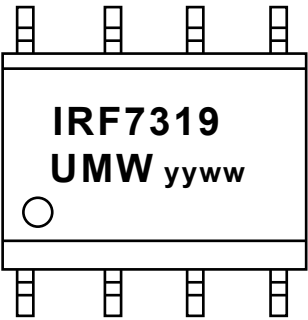
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°



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-30V P-Channel MOSFET

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRF7319TR	SOP-8	3000	Tape and reel



10.Disclaimer

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