

1. Description

The ADA4692-2 are dual and the ADA4692-4 are the quad rail-to-rail output, single-supply amplifiers featuring low power, wide bandwidth, and low noise.

The ADA4692-4 is a quad version without shutdown.

These amplifiers are ideal for a wide variety of applications. Audio, filters, photodiode amplifiers, and charge amplifiers, all benefit from this combination of performance and features. Additional applications for these amplifiers include portable consumer audio players with low noise and low distortion that provide high gain and slew rate response over the audio band at low power. Industrial applications with high impedance sensors, such as pyroelectric and IR sensors, benefit from the high impedance and low 0.5 pA input bias, low offset drift, and enough bandwidth and response for low gain applications.

3. Applications

- Photodiode amplifiers
- Sensor amplifiers
- Portable medical and instrumentation
- Portable audio: MP3s, PDAs, and smartphones
- Communications

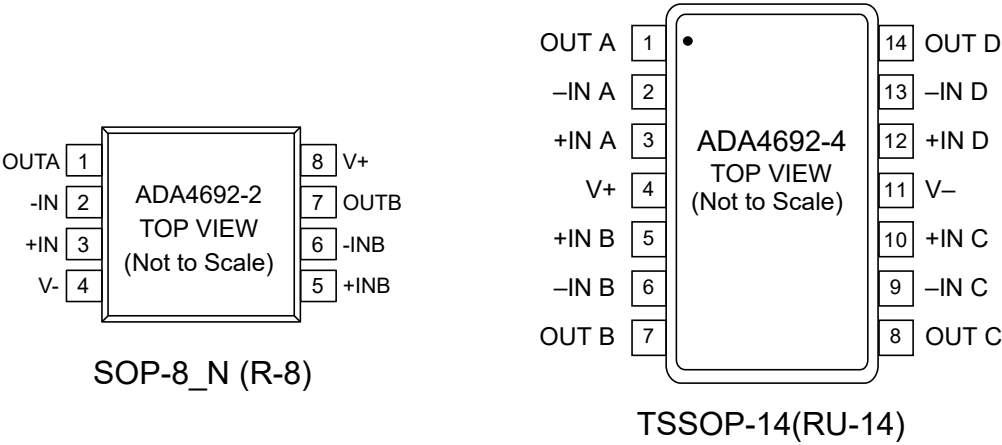
2. Features

- Low power: 180 μ A typical
- Very low input bias currents: 0.5 pA typical
- Low noise: 16 nV/ $\sqrt{\text{Hz}}$ typical
- 3.6 MHz bandwidth
- Offset voltage: 500 μ V typical
- Low offset voltage drift: 4 μ V/ $^{\circ}\text{C}$ maximum
- Low distortion: 0.003% THD + N
- 2.7 V to 5 V single supply or ± 1.35 V to ± 2.5 V dual supply

- Low-side current sense
- ADC drivers
- Active filters
- Sample-and-hold



4.Pinning Information





5. Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Description	Rating
Supply Voltage	6 V
Input Voltage	$V_{SS} - 0.3 \text{ V}$ to $V_O + 0.3 \text{ V}$
Input Current ¹	$\pm 10 \text{ mA}$
Shutdown Pin Rise/Fall Times	50 μs maximum
Differential input Voltage ²	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Temperature	-65°C to $+150^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-40°C to $+125^\circ\text{C}$
Junction Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C

¹ Input pins have clamp diodes to the supply pins. Limit input current to 10 mA or less whenever the input signal exceeds the power supply rail by 0.3V.

² Differential input voltage is limited to 6V or the supply voltage, whichever is less.



6.1 Electrical Characteristics

Supply voltage (V_{SY})=2.7V, common-mode voltage (V_{CM})= $V_{SY}/2$, $T_A=25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Offset Voltage	V _{OS}	V _{CM} =−0.3V to +1.6V		0.5	2.5	mV
Dual (ADA469x -2)		V _{CM} =−0.1V to 1.6V, −40°C<T _A <125°C			3.5	mV
Quad (ADA469x -4)		V _{CM} =−0.1V to 1.6V, −40°C<T _A <125°C			4	mV
Offset Voltage Drift	ΔV _{OS} /ΔT	−40°C <T _A <125°C		1	4	μV/°C
Input Bias Current	I _B			0.5	5	pA
Input Offset Current	I _{OS}	−40°C <T _A <125°C			360	pA
				1	8	pA
Input Voltage Range		−40°C <T _A <125°C			225	pA
−40°C <T _A <125°C		−0.3		1.6	V	
Common -Mode Rejection Ratio	CMRR	V _{CM} =−0.3V to +1.6V	70	90		dB
Large Signal Voltage Gain	A _{VO}	V _{CM} =−0.1V to 1.6V, −40°C<T _A <125°C	62			dB
		Load resistance (R _L)=2kΩ, output voltage (V _{OUT}) = 0.5V to 2.2V	90	100		dB
		−40°C <T _A <85°C	80			dB
		−40°C <T _A <125°C	63			dB
		R _L =600Ω, V _{OUT} =0.5V to 2.2V	85	95		dB
Input Capacitance	C _{IN}					
Differentia I Mode	C _{INDM}			2.5		pF
Common Mode	C _{INCM}			7		pF
Logic High Voltage (Enabled)	V _{IH}	−40°C<T _A <125°C	1.6			V
Logic Low Voltage (Power -Down)	V _{IL}	−40°C<T _A <125°C			0.5	V
Logic input Current (Per Pin)	I _{IN}	−40°C<T _A <125°C, 0V≤ shutdown voltage (V _{SD})≤ 2.7V			1	μA
Output Voltage High	V _{OH}	R _L =2kΩ to V _{CM}	2.65	2.67		V
		−40°C<T _A <125°C	2.6			V
		R _L =600Ω to V _{CM}	2.55	2.59		V
		−40°C<T _A <125°C	2.5			V



Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage Low	V_{OL}	$R_L=2k\Omega$ to V_{CM}		24	33	mV
		$-40^{\circ}\text{C}<T_A<125^{\circ}\text{C}$			43	mV
		$R_L=600\Omega$ to V_{CM}		78	103	mV
		$-40^{\circ}\text{C}<T_A<125^{\circ}\text{C}$			138	mV
Short-Circuit Current	I_{SC}	$V_{OUT}=V_{SY}$ or GND		± 15		mA
Closed-Loop Output Impedance	Z_{OUT}	Frequency (f)=1MHz voltage gain (A_V)=-100		372		Ω
Output Pin Leakage Current		$-40^{\circ}\text{C}<T_A<125^{\circ}\text{C}$, shutdown active V_{SD} =negative supply voltage (V_{SS})		10		nA
Power Supply Rejection Ratio	PSRR	$V_{SY}=2.7\text{V}$ to 5.5V	80	90		dB
		$-40^{\circ}\text{C}<T_A<125^{\circ}\text{C}$	75			dB
Supply Current Per Amplifier	I_{SY}	$V_{OUT}=V_{SY}/2$		165	200	μA
		$-40^{\circ}\text{C}<T_A<125^{\circ}\text{C}$			240	μA
Supply Current Shutdown Mode	I_{SD}	All amplifiers shut down, $V_{SD}=V_{SS}$		10		nA
		$-40^{\circ}\text{C}<T_A<125^{\circ}\text{C}$			2	μA
Slew Rate	SR	$R_L=600\Omega$, load capacitance (C_L)=20pF, $A_V=+1$		1.1		V/ μs
		$R_L=2k\Omega$, $C_L=20\text{pF}$, $A_V=+1$		1.4		V/ μs
Settling Time to 0.1%	t_s	Step=0.5V, $R_L=2k\Omega$, 600 Ω		1		μs
Gain Bandwidth Product	GBP	$R_L=1M\Omega$, $C_L=35\text{pF}$, $A_V=+1$		3.6		MHz
Phase Margin	Φ_M	$R_L=1M\Omega$, $C_L=35\text{pF}$, $A_V=+1$		49		Degrees
Turn-On/Turn-Off Time		$R_L=600\Omega$		1		μs



Parameter	Symbol	Conditions	Min	Typ	Max	Units
Distortion	THD+ N	$A_V = -1$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, input voltage (V_{IN}) $rms = 0.15V_{rms}$		0.009		%
		$A_V = -1$, $R_L = 600\Omega$, $f = 1\text{ kHz}$ $V_{IN}rms = 0.15V_{rms}$		0.01		%
		$A_V = +1$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$ $V_{IN}rms = 0.15V_{rms}$		0.006		%
		$A_V = +1$, $R_L = 600\Omega$, $f = 1\text{ kHz}$ $V_{IN}rms = 0.15V_{rms}$		0.009		%
Voltage Noise	e_{np-p}	$f = 0.1\text{ Hz to } 10\text{ Hz}$		3.1		μV_{p-p}
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		16		$nV/\sqrt{Hz}$
		$f = 10\text{ kHz}$		13		$nV/\sqrt{Hz}$



6.2 Electrical Characteristics

$V_{SY}=5V$, $V_{CM}=V_{SY}/2$, $T_A=25^{\circ}C$, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Offset Voltage	V _{OS}	V _{CM} =−0.3V to +3.9V		0.5	2.5	mV
Dual (ADA4692-2)		V _{CM} =−0.1V to 3.9V, −40°C<T _A <125°C			3.5	mV
Quad (ADA4692-4)		V _{CM} =−0.1V to 3.9V, −40°C<T _A <125°C			4	mV
Offset Voltage Drift	ΔV _{OS} /ΔT	−40°C <T _A <125°C		1	4	μV/°C
Input Bias Current	I _B			0.5	5	pA
Input Offset Current	I _{OS}	−40°C <T _A <125°C			360	pA
				1	8	pA
Input Voltage Range		−40°C <T _A <125°C			260	pA
		−40°C <T _A <125°C	-0.3		±3.9	V
Common -Mode Rejection Ratio	CMRR	V _{CM} =−0.3V to +3.9V	75	98		dB
		V _{CM} =−0.1V to 3.9V, −40°C<T _A <125°C	68			dB
Large Signal Voltage Gain	A _{VO}	R _L =2kΩ, V _{OUT} =0.5V to 4.5V V _{CM} =0 V	95	110		dB
		−40°C <T _A <85°C	80			dB
		−40°C <T _A <125°C	70			dB
		R _L =600Ω, V _{OUT} =0.5V to 2.2V, V _{CM} =0V	90	100		dB
Differentia I Mode	C _{INDM}			2.5		pF
Common Mode	C _{INCM}			7		pF
Logic High Voltage (Enabled)	V _{IH}	−40°C<T _A <125°C	2			V
Logic Low Voltage (Power -Down)	V _{IL}	−40°C<T _A <125°C			0.8	V
Logic input Current (Per Pin)	I _{IN}	−40°C<T _A <125°C, 0V≤V _{SD} ≤2.7V			1	μA
Output Voltage High	V _{OH}	R _L =2kΩ to V _{CM}	4.95	4.97		V
		−40°C<T _A <125°C	4.9			V
		R _L =600Ω to V _{CM}	4.85	4.88		V
		−40°C<T _A <125°C	4.8			V



Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage Low	V_{OL}	$R_L=2k\Omega$ to V_{CM}		30	40	mV
		$-40^{\circ}\text{C}<T_A<125^{\circ}\text{C}$			55	mV
		$R_L=600\Omega$ to V_{CM}		100	128	mV
		$-40^{\circ}\text{C}<T_A<125^{\circ}\text{C}$			173	mV
Short-Circuit Current	I_{SC}	$V_{OUT}=V_{SY}$ or GND		± 55		mA
Closed-Loop Output Impedance	Z_{OUT}	ADA4691 -2, $f=1\text{MHz}$, $A_V=-100$		364		Ω
		ADA4691 -2, $f=1\text{MHz}$, $A_V=-100$		246		
Output Pin Leakage Current		$-40^{\circ}\text{C}<T_A<125^{\circ}\text{C}$, shutdown active $V_{SD}=V_{SS}$		10		nA
Power Supply Rejection Ratio	PSRR	$V_{SY}=2.7\text{V}$ to 5.5V	80	90		dB
		$-40^{\circ}\text{C}<T_A<125^{\circ}\text{C}$	75			dB
Supply Current Per Amplifier	I_{SY}	$V_{OUT}=V_{SY}/2$		180	225	μA
		$-40^{\circ}\text{C}<T_A<125^{\circ}\text{C}$			275	μA
Supply Current Shutdown Mode	I_{SD}	All amplifiers shut down, $V_{SD}=V_{SS}$		10		nA
		$-40^{\circ}\text{C}<T_A<125^{\circ}\text{C}$			2	μA
Slew Rate	SR	$R_L=2k\Omega$, 600Ω , $C_L=20\text{pF}$, $A_V=+1$		1.3		$\text{V}/\mu\text{s}$
Settling Time to 0.1%	t_s	$V_{IN}=2\text{V}$ step, $R_L=2k\Omega$ or 600Ω		1.5		μs
Gain Bandwidth Product	GBP	$R_L=1\text{M}\Omega$, $C_L=35\text{pF}$, $A_V=+1$		3.6		MHz
Phase Margin	Φ_M	$R_L=1\text{M}\Omega$, $C_L=35\text{pF}$, $A_V=+1$		52		Degrees
Turn-On/Turn-Off Time		$R_L=600\Omega$		1		μs



Parameter	Symbol	Conditions	Min	Typ	Max	Units
Distortion	THD+ N	$A_V=-1, R_L=2k\Omega, f=1kHz$ $V_{INrms}=0.8Vrms$		0.006		%
		$A_V=-1, R_L=600\Omega, f=1kHz$ $V_{INrms}=0.8Vrms$		0.008		%
		$A_V=-1, R_L=2k\Omega, f=1kHz$ $V_{INrms}=0.8Vrms$		0.001		%
		$A_V=-1, R_L=600\Omega, f=1kHz$ $V_{INrms}=0.8Vrms$		0.003		%
Voltage Noise	e_{np-p}	$f=0.1Hz$ to $10Hz$		3.2		μV_{p-p}
Voltage Noise Density	e_n	$f=1kHz$		16		$nV/\sqrt{Hz}$
		$f=10kHz$		13		$nV/\sqrt{Hz}$



7.1 Typical Characteristic

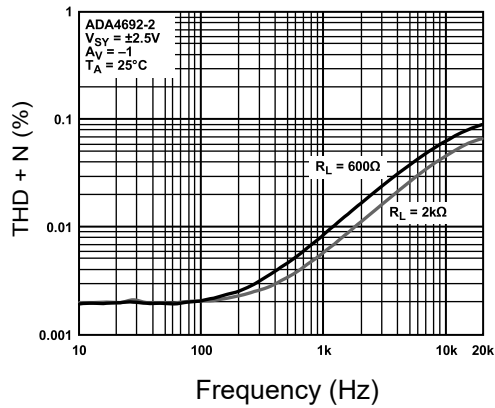


Figure 1: THD + Noise vs. Frequency

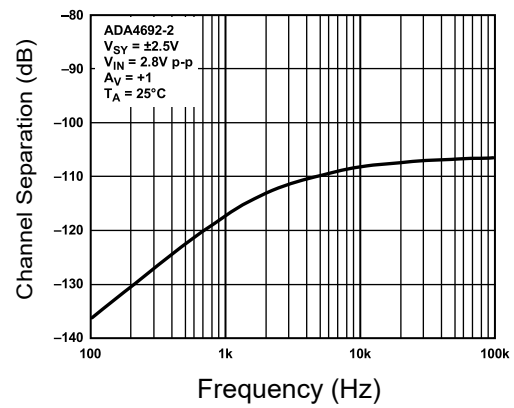


Figure 2: Channel Separation vs. Frequency

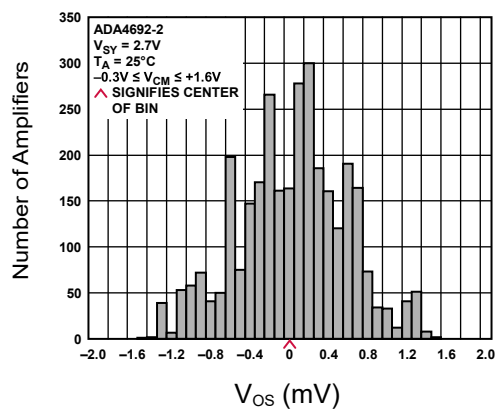


Figure 3: Input Offset Voltage Distribution

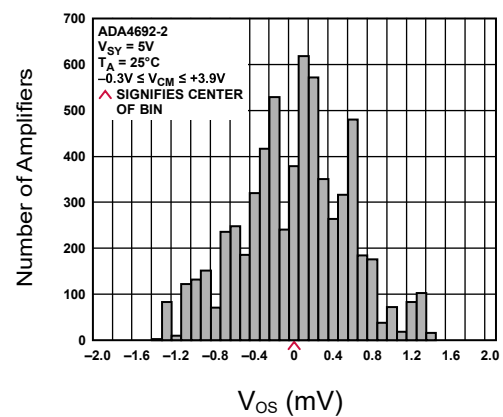


Figure 4: Input Offset Voltage Distribution

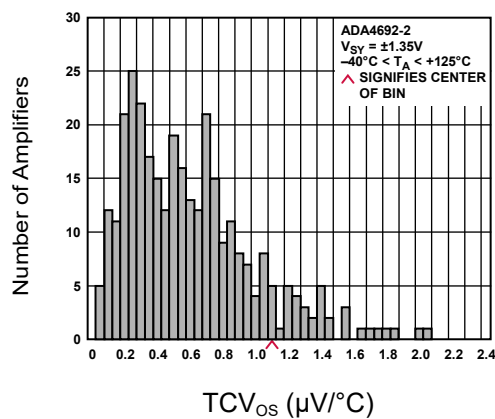


Figure 5: Input Offset Voltage Drift Distribution

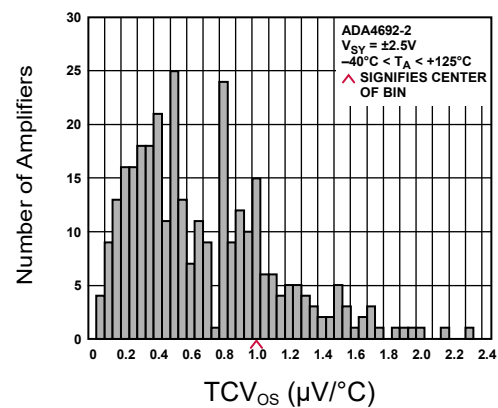


Figure 6: Input Offset Voltage Drift Distribution



7.2 Typical Characteristic

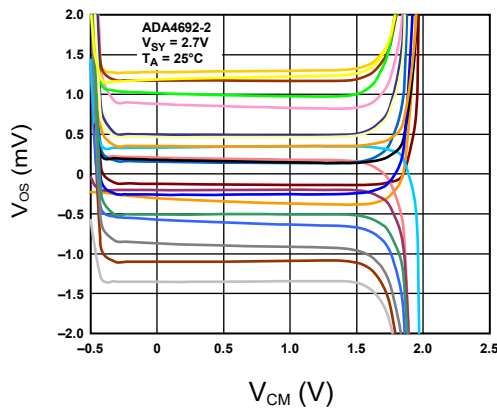


Figure 7: Input Offset Voltage vs. Common-Mode Voltage

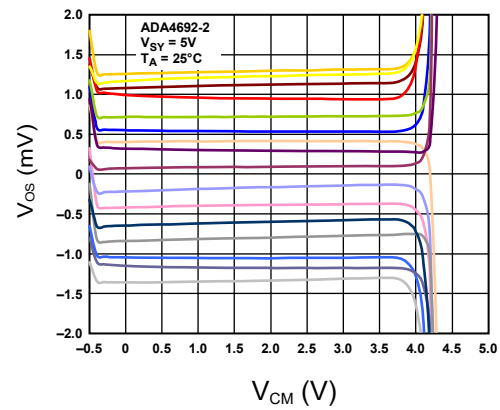


Figure 8: Input Offset Voltage vs. Common-Mode Voltage

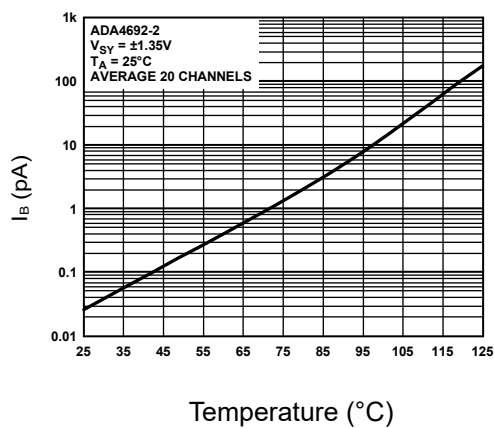


Figure 9: Input Bias Current vs. Temperature

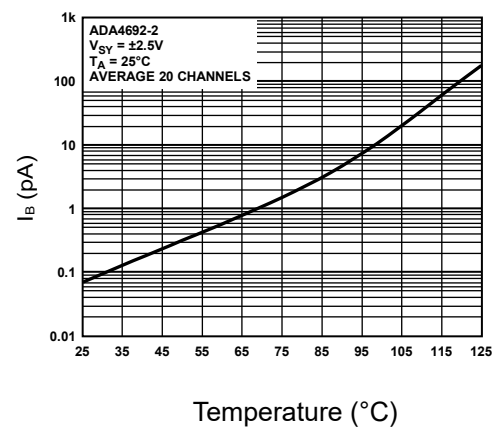


Figure 10: Input Bias Current vs. Temperature

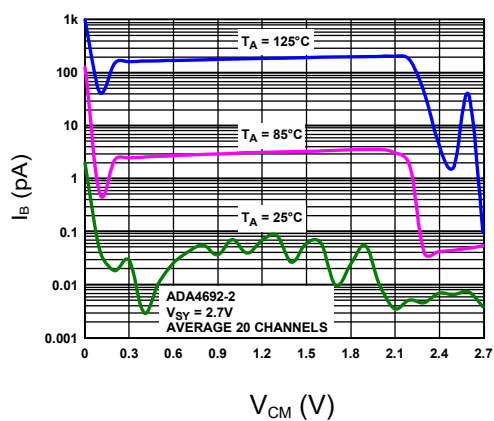


Figure 11: Input Bias Current vs. Common-Mode Voltage

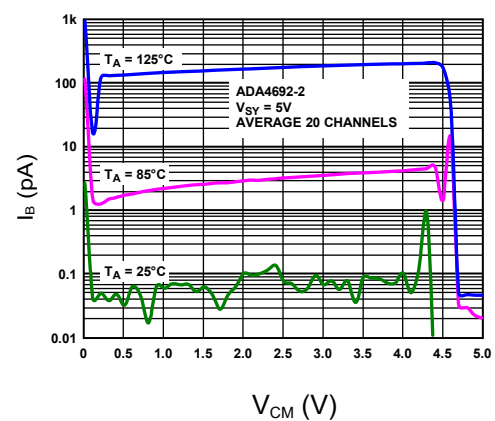


Figure 12: Input Bias Current vs. Common-Mode Voltage



7.3 Typical Characteristic

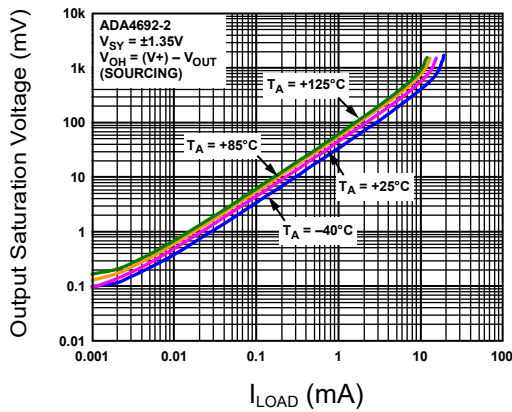


Figure 13: Output Voltage (V_{OH}) to Supply Rail vs. Load Current

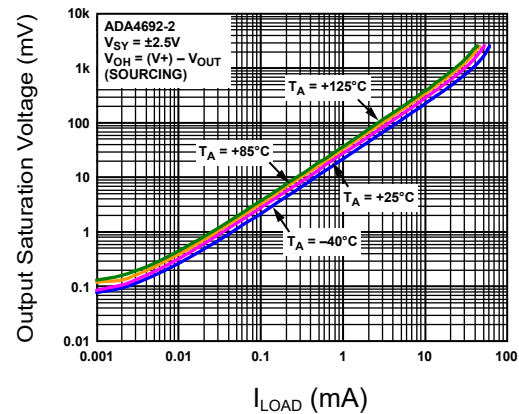


Figure 14: Output Voltage (V_{OL}) to Supply Rail vs. Load Current

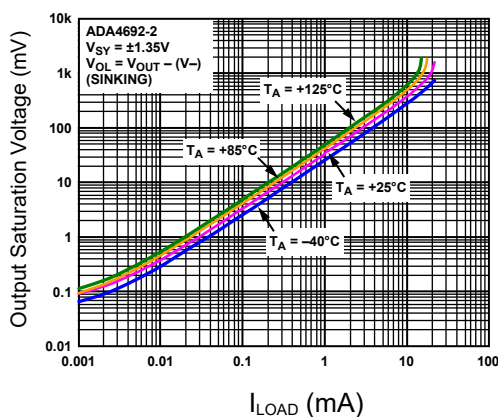


Figure 15: Output Voltage (V_{OL}) to Supply Rail vs. Load Current

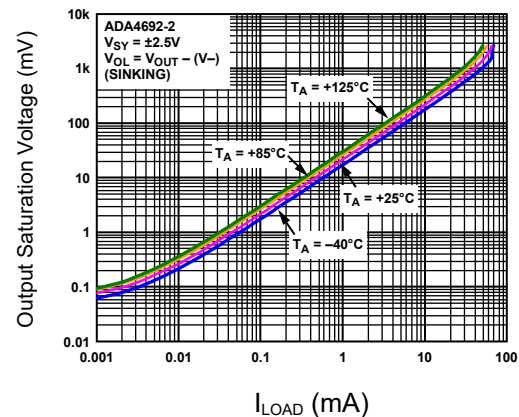


Figure 16: Output Voltage (V_{OL}) to Supply Rail vs. Load Current

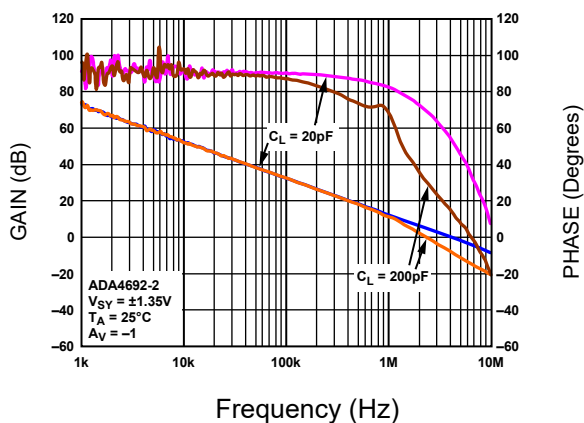


Figure 17: Open-Loop Gain and Phase vs. Frequency

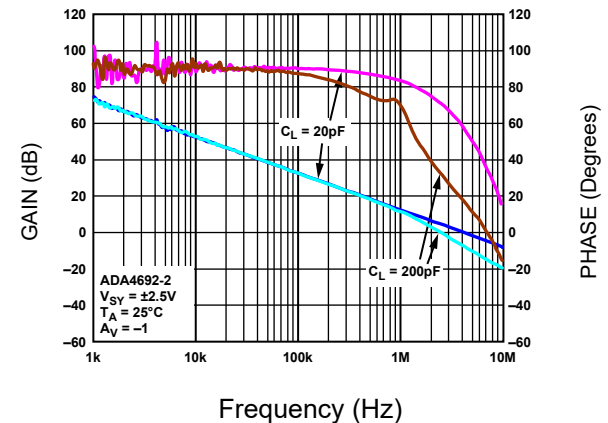


Figure 18: Open-Loop Gain and Phase vs. Frequency



7.4 Typical Characteristic

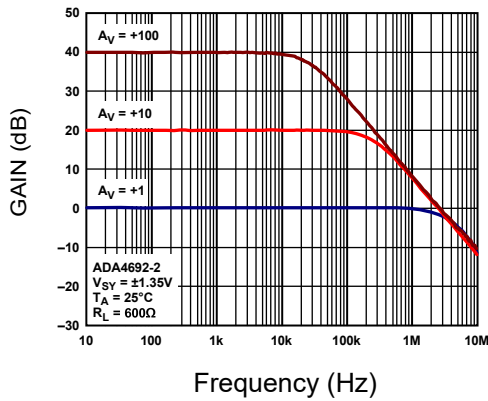


Figure 19: Closed-Loop Gain vs. Frequency

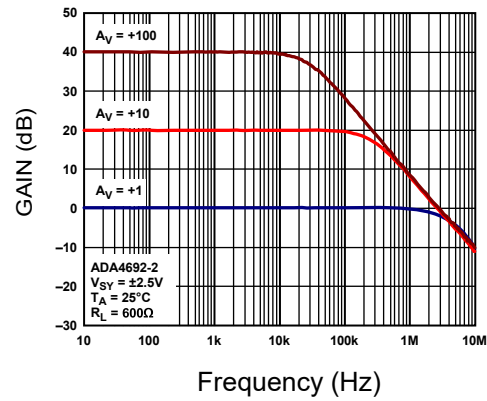


Figure 20: Closed-Loop Gain vs. Frequency

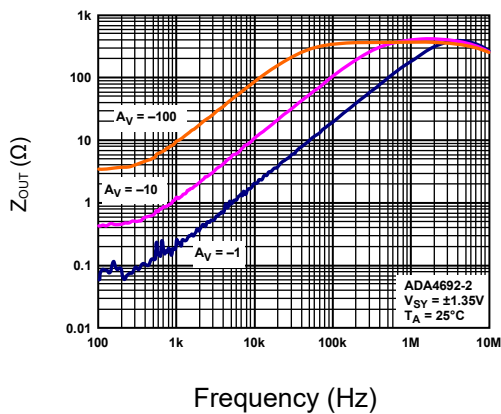


Figure 21: Output Impedance vs. Frequency

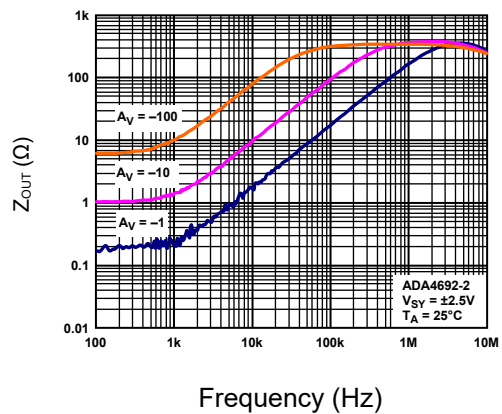


Figure 22: Output Impedance vs. Frequency

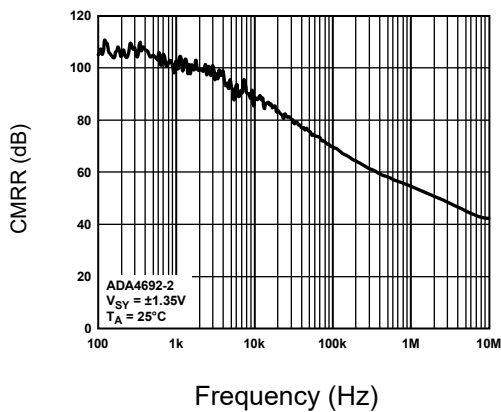


Figure 23: CMRR vs. Frequency

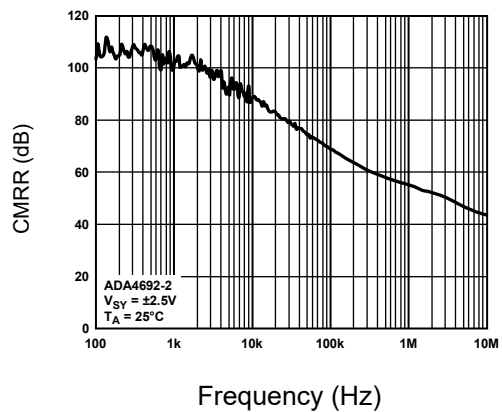
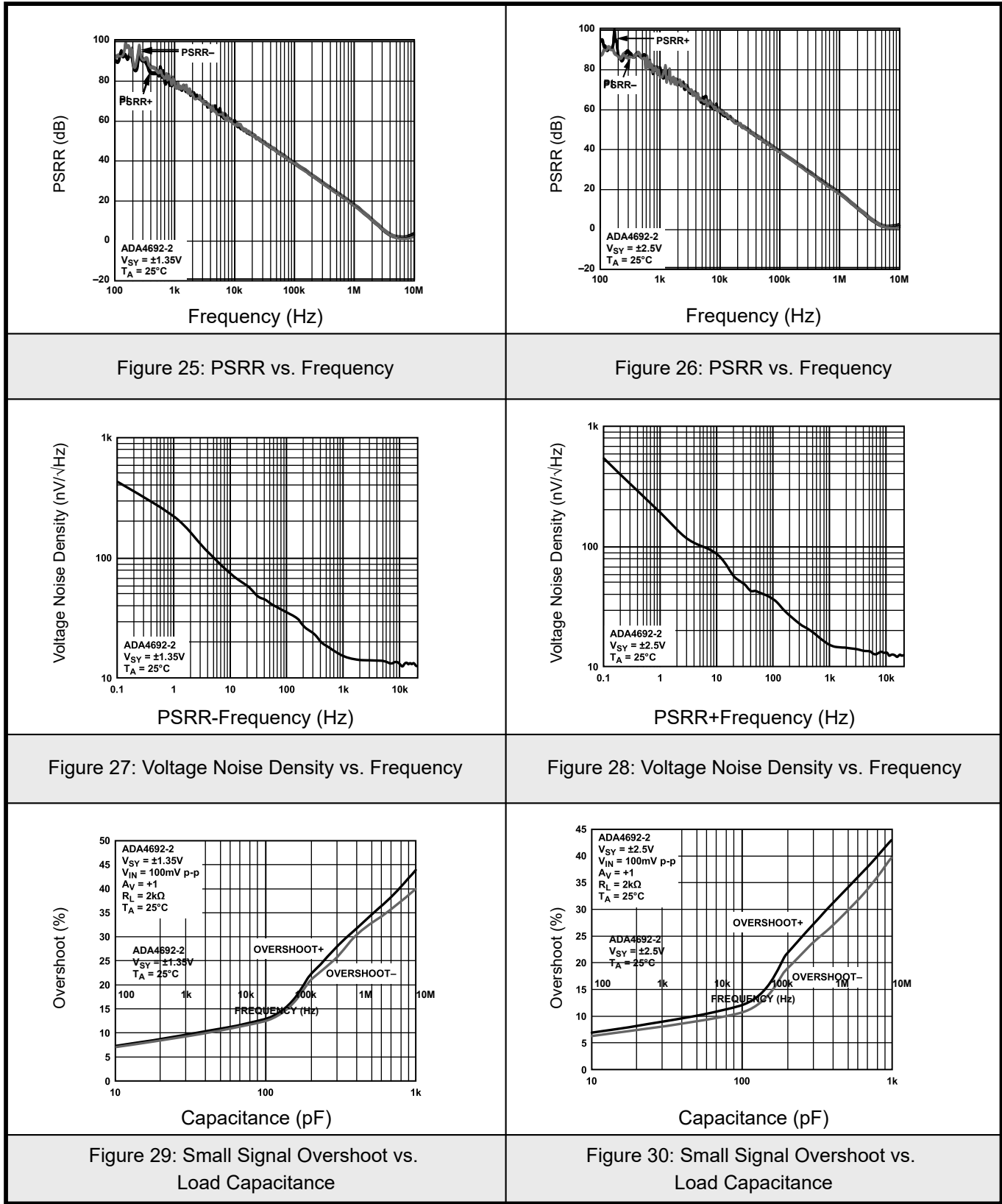


Figure 24: CMRR vs. Frequency



7.5Typical Characteristic



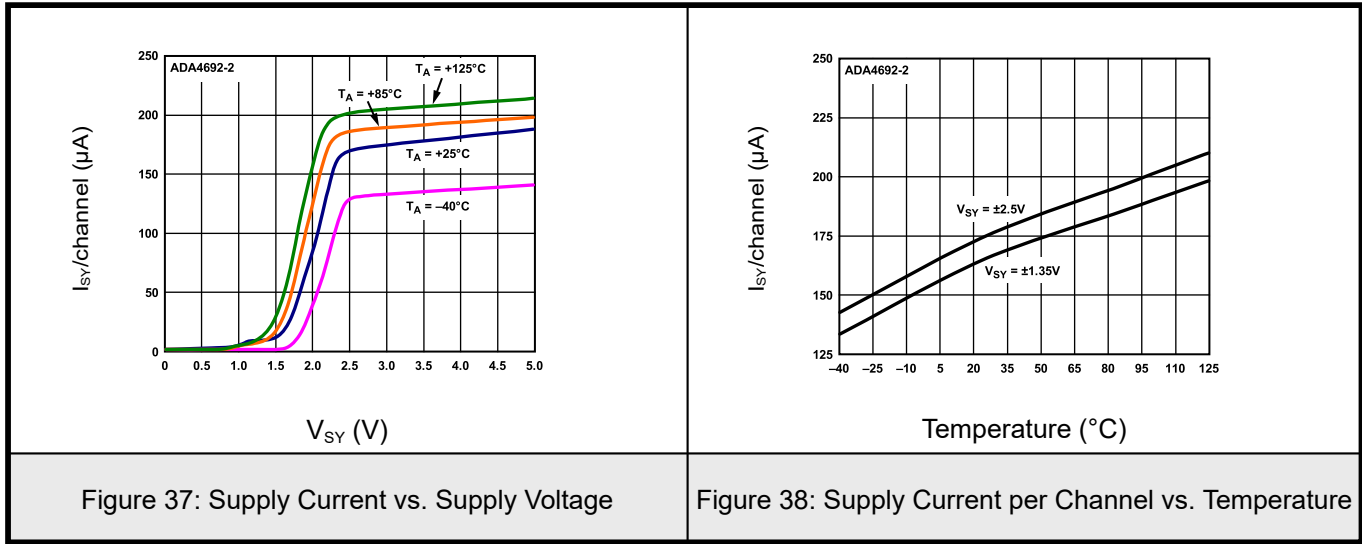


7.6Typical Characteristic

Output (500mV/DIV) Time (2μs/DIV)	Output (500mV/DIV) Time (2μs/DIV)
Figure 31: Large Signal Transient Response	Figure 32: Large Signal Transient Response
Output (20mV/DIV) Time (2μs/DIV)	Output (20mV/DIV) Time (2μs/DIV)
Figure 33: Small Signal Transient Response	Figure 34: Small Signal Transient Response
Output (1μV/DIV) Time (1s/DIV)	Output (1μV/DIV) Time (1s/DIV)
Figure 35: 0.1 Hz to 10 Hz Noise	Figure 36: 0.1 Hz to 10 Hz Noise

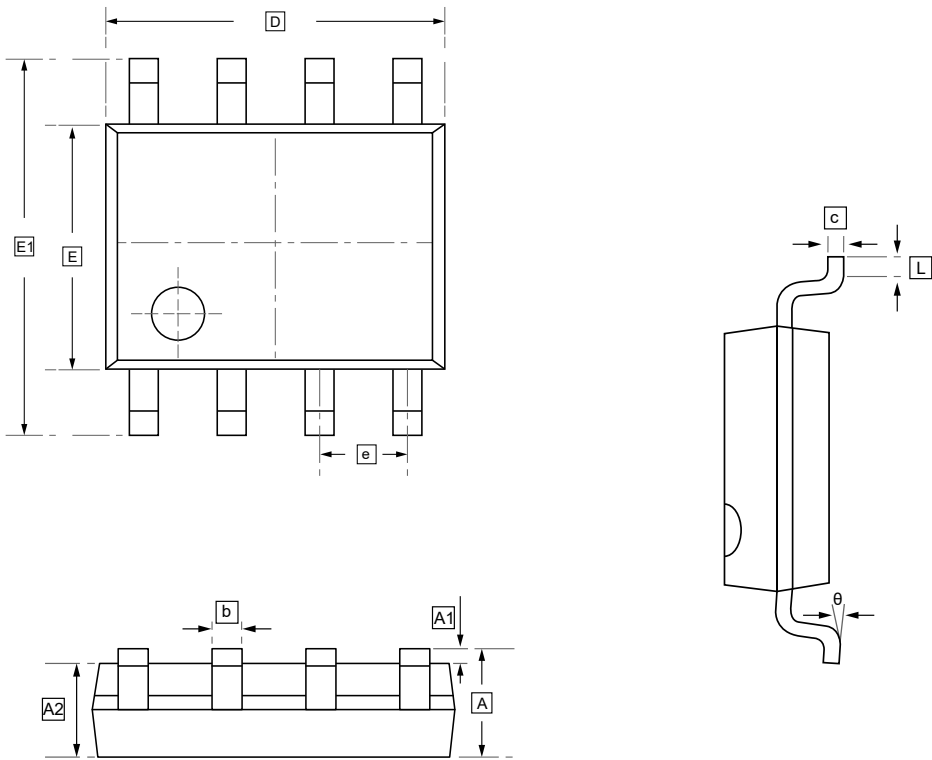


7.7Typical Characteristic





8.1SOP-8 Package Outline Dimensions

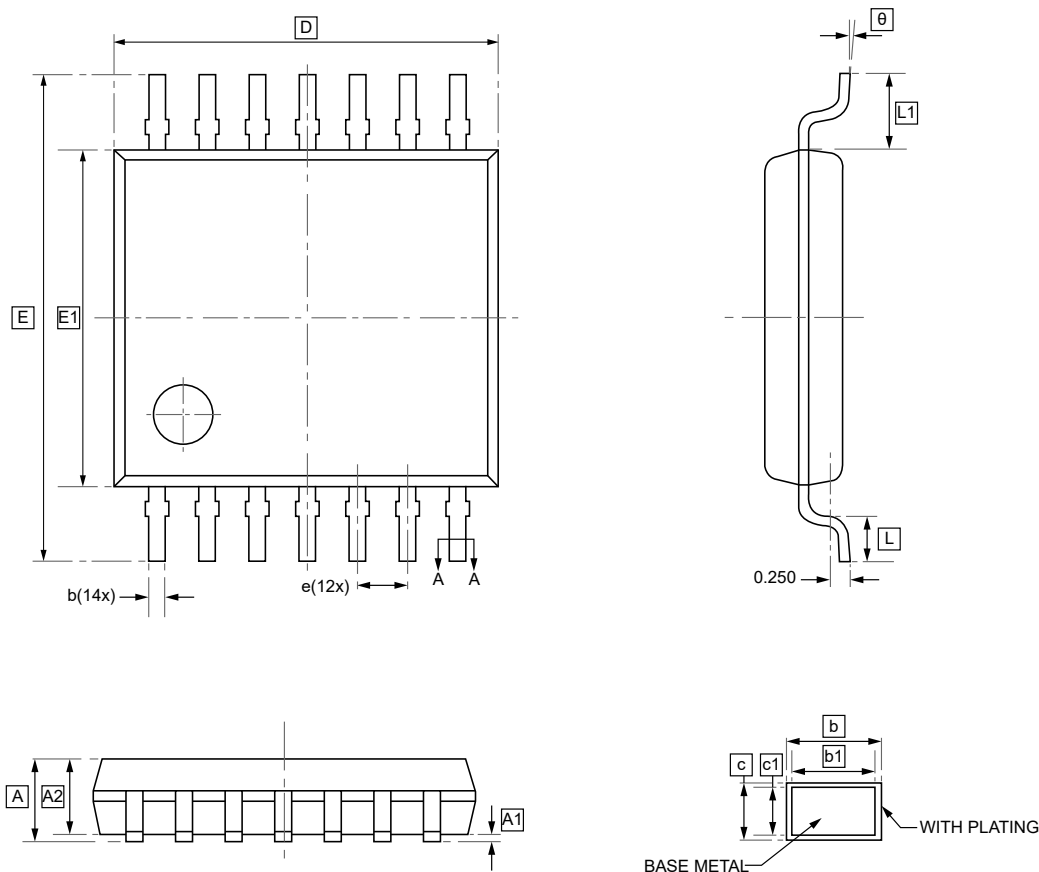


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°



8.2TSSOP-14 Package Outline Dimensions



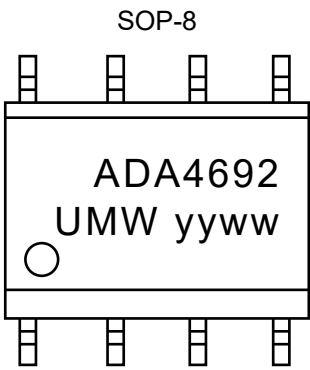
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	b1	c	c1	D	E	E1	e	L1
Min	-	0.05	0.90	0.20	0.19	0.13	0.120	4.90	6.20	4.30	0.65	0.85
Max	1.20	0.15	1.05	0.28	0.25	0.17	0.14	5.10	6.60	4.50	BSC	1.15

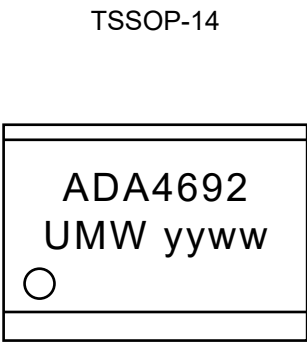
Symbol	L	θ
Min	0.45	0°
Max	0.75	8°



9.Ordering information



yy: Year Code
ww: Week Code



yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW ADA4692-2ARZ	ADA4692	SOP-8	2500	Tape and reel
UMW ADA4692-4ARUZ	ADA4692	TSSOP-14	4000	Tape and reel



10.Disclaimer

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