

1.1Features

- $V_{DS(V)}=60V$
- $I_D=47A(V_{GS}=10V)$
- $R_{DS(ON)}<8.4m\Omega(V_{GS}=10V)$
- Improved Gate, Avalanche and
- Dynamic dv/dt Ruggedness

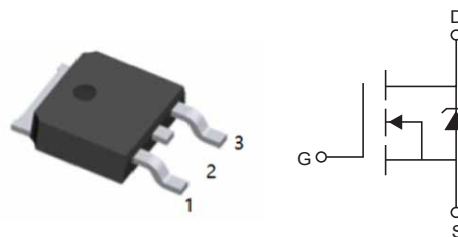
1.2Features

- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability

2.Pinning information

Pin	Symbol	Description
1	G	GATE
3	S	SOURCE
2	D	DRAIN

TO-252(DPAK)
top view



3.Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Continuous Drain Current, V_{GS} @ 10V(Silicon Limited)	$T_C=25^{\circ}C$	I_D	79 ①	A
Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	$T_C=100^{\circ}C$		56 ①	A
Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited)	$T_C=25^{\circ}C$		56	A
Pulsed Drain Current ②		I_{DM}	315	A
Maximum Power Dissipation	$T_C=25^{\circ}C$	P_D	110	W
Linear Derating Factor			0.76	W/°C
Gate-to-Source Voltage		V_{GS}	± 20	V
Peak Diode Recovery ④		dv/dt	21	V/ns
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C
Soldering Temperature, for 10 seconds (1.6mm from case)			300	°C



Single Pulse Avalanche Energy ③	$E_{AS(Thermally\ limited)}$	88	mJ
Avalanche Current ②	I_{AR}	47	A
Repetitive Avalanche Energy ⑤	E_{AR}	11	mJ
Junction-to-Case ⑨	$R_{\theta JC}$	1.32	°C/W
Junction-to-Ambient (PCB Mount) ⑧⑨	$R_{\theta JA}$	50	°C/W
Junction-to-Ambient ⑨	$R_{\theta JA}$	110	°C/W



4. Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	60			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25°C , $I_D=5\text{mA}$ ②		0.073		V/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=47\text{A}$ ⑤		7.1	8.4	m Ω
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=100\mu\text{A}$			4	V
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS}=60\text{V}$, $V_{GS}=0\text{V}$	2		20	μA
		$V_{DS}=48\text{V}$, $V_{GS}=0\text{V}$, $T_J=125^\circ\text{C}$			250	μA
Gate-to-Source Forward Leakage	I_{GSS}	$V_{GS}=20\text{V}$			100	nA
Gate-to-Source Reverse Leakage		$V_{GS}=-20\text{V}$			-100	nA
Forward Transconductance	g_{FS}	$V_{DS}=50\text{V}$, $I_D=47\text{A}$	110			S
Total Gate Charge	Q_g	$I_D=47\text{A}$, $V_{DS}=30\text{V}$, $V_{GS}=10\text{V}$ ⑤		46	69	nC
Gate-to-Source Charge	Q_{gs}			10		nC
Gate-to-Drain ("Miller") Charge	Q_{gd}			12		nC
Total Gate Charge Sync. (Q_g-Q_{gd})	Q_{sync}	$I_D=47\text{A}$, $V_{DS}=30\text{V}$, $V_{GS}=10\text{V}$		34		nC
Internal Gate Resistance	$R_{G(int)}$			0.73		Ω
Turn-On Delay Time	$t_{D(on)}$	$V_{DD}=39\text{V}$, $I_D=47\text{A}$ $R_G=10\Omega$, $V_{GS}=10\text{V}$ ⑤		13		ns
Rise Time	t_r			35		ns
Turn-Off Delay Time	$t_{D(off)}$			55		ns
Fall Time	t_f			46		ns
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}$, $V_{DS}=50\text{V}$ $f=1\text{MHz}$		2290		pF
Output Capacitance	C_{oss}			270		pF
Reverse Transfer Capacitance	C_{rss}			130		pF
Effective Output Capacitance (Energy Related)	$C_{oss\text{eff.}(ER)}$	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V to }60\text{V}$ ⑦		390		pF
Effective Output Capacitance (Time Related)	$C_{oss\text{eff.}(TR)}$	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V to }60\text{V}$ ⑥		630		pF



Diode Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			79①	A
Pulsed Source Current (Body Diode) ②	I_{SM}				315	A
Diode Forward Voltage	V_{SD}	$T_J=25^\circ\text{C}, I_S=47\text{A}, V_{GS}=0\text{V}$ ⑤			1.3	V
Reverse Recovery Time	t_{rr}	$T_J=25^\circ\text{C}, V_R=51\text{V}$		26	39	ns
		$T_J=125^\circ\text{C}, I_F=47\text{A}$		31	47	ns
Reverse Recovery Charge	Q_{rr}	$T_J=25^\circ\text{C}, di/dt=100\text{A}/\mu\text{s}$ ⑤		24	36	nC
		$T_J=125^\circ\text{C}$		35	53	nC
Reverse Recovery Current	I_{RRM}	$T_J=25^\circ\text{C}$		1.8		A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 56A by source bonding technology. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J=25^\circ\text{C}$, $L=0.08\text{mH}$, $R_G=25\Omega$, $I_{AS}=47\text{A}$, $V_{GS}=10\text{V}$. Part not recommended for use above this value.
- ④ $I_{SD} \leq 47\text{A}$, $di/dt \leq 1668\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R_θ is measured at T_J approximately 90°C .



6.1 Typical Characteristics

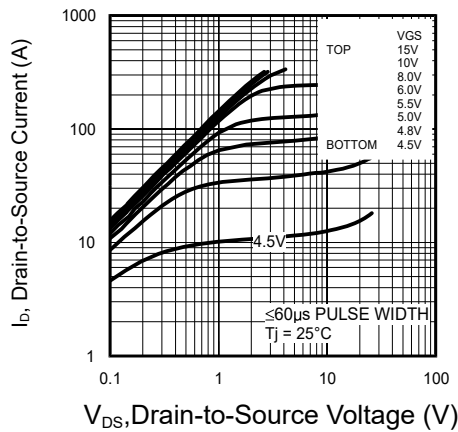


Figure 1: Typical On-Resistance vs. Gate Voltage

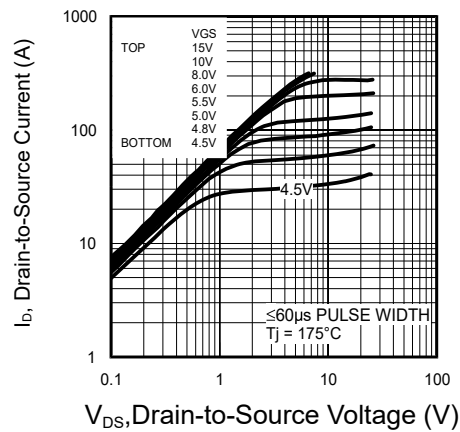


Figure 2: Typical Output Characteristics

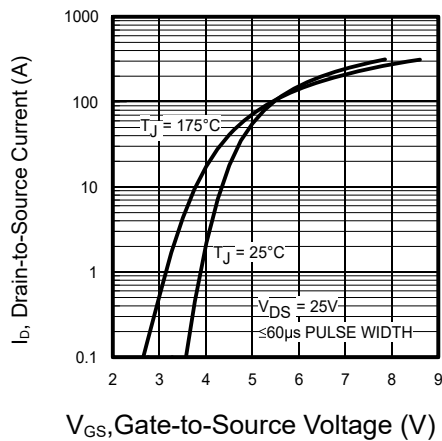


Figure 3: Typical Output Characteristics

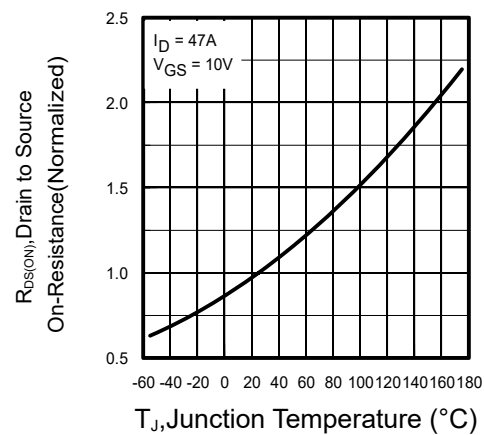


Figure 4: Normalized On-Resistance vs. Temperature

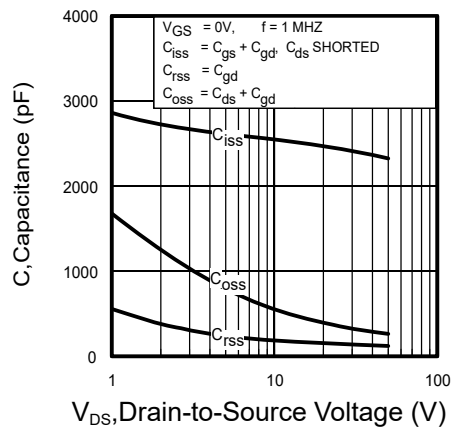


Figure 5: Typical Capacitance vs. Drain-to-Source Voltage

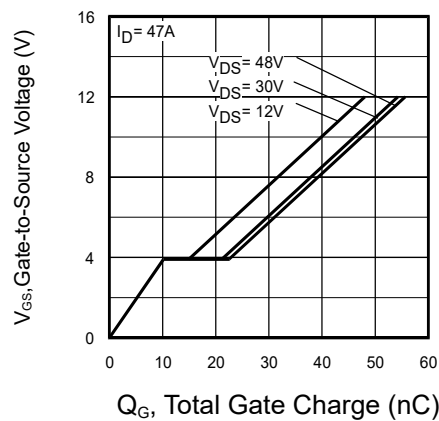


Figure 6: Typical Gate Charge vs.



6.2 Typical Characteristics

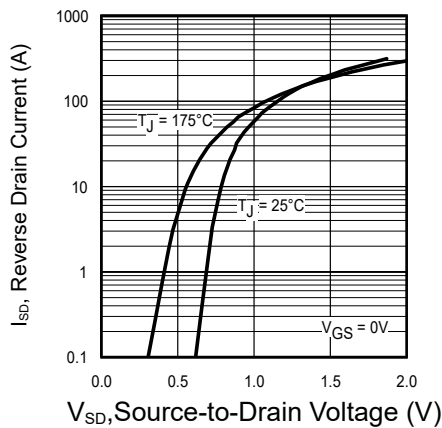


Figure 7: Typical Capacitance vs. Drain-to-Source Voltage

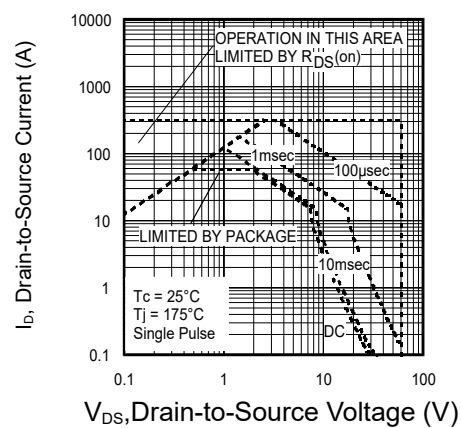


Figure 8: Maximum Safe Operating Area

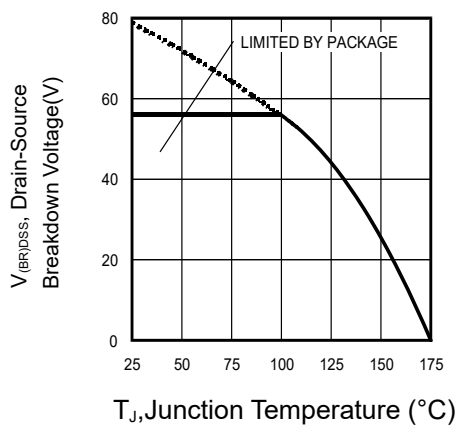


Figure 9: Drain-to-Source Breakdown Voltage

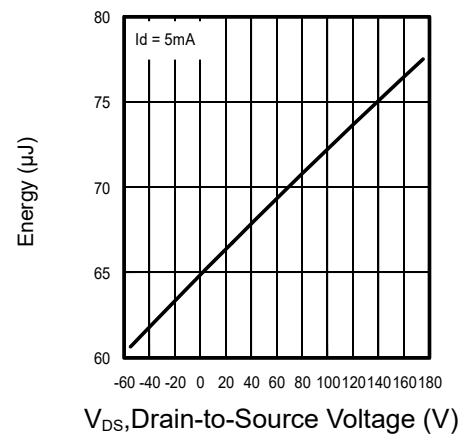


Figure 10: Typical C_{oss} Stored Energy

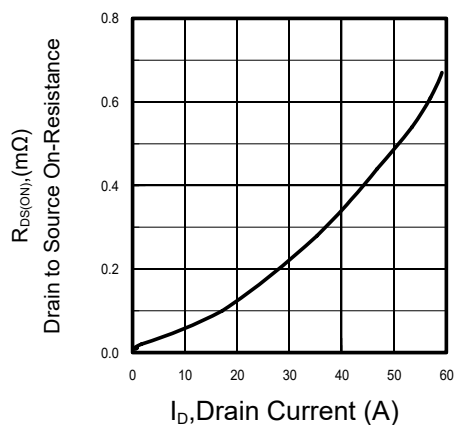


Figure 11: Typical On-Resistance vs. Drain Current

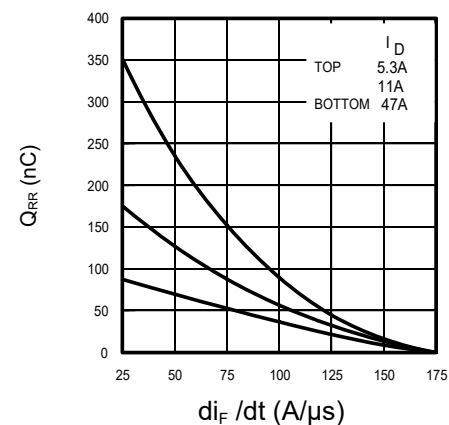


Figure 12: Typical Stored Charge vs. di/dt



6.3 Typical Characteristics

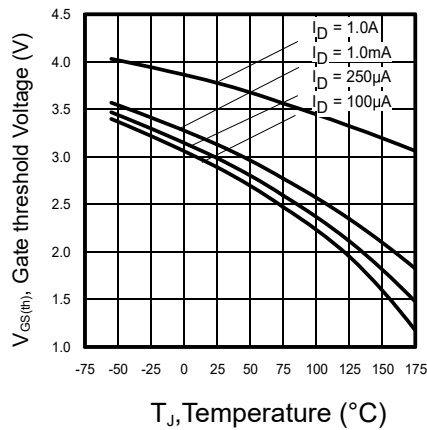


Figure 13: Threshold Voltage vs. Temperature

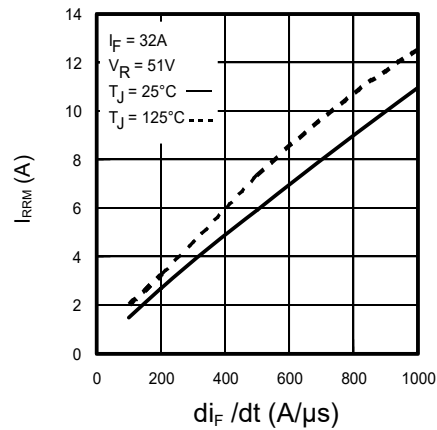


Figure 14: Typical Recovery Current vs. di/dt

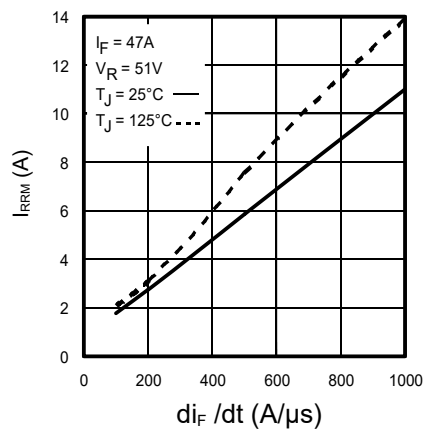


Figure 15: Typical Recovery Current vs. di/dt

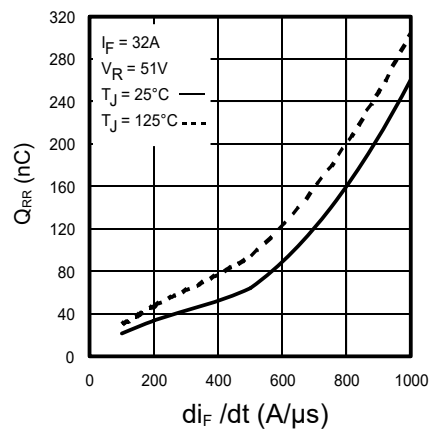


Figure 16: Typical Stored Charge vs. di/dt

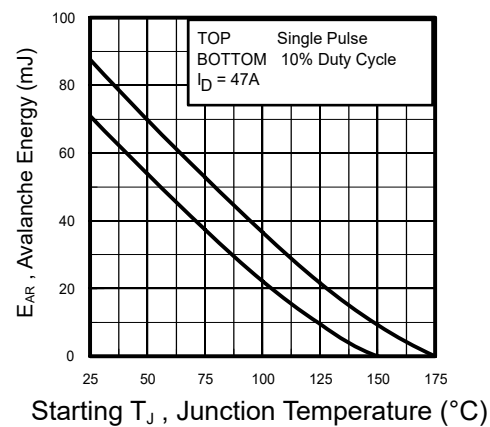


Figure 17: Typical On-Resistance vs. Drain Current

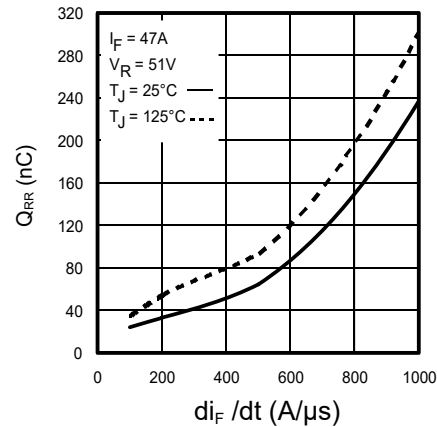


Figure 18: Typical Stored Charge vs. di/dt



6.4Typical Characterisitics

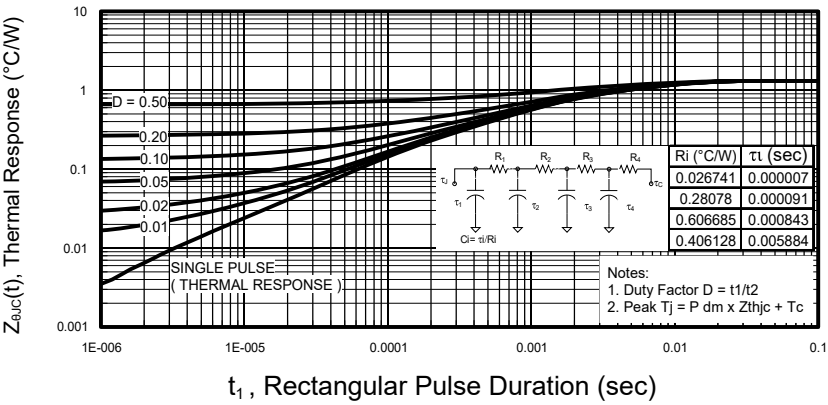


Figure 19: Maximum Effective Transient Thermal Impedance, Junction-to-Case

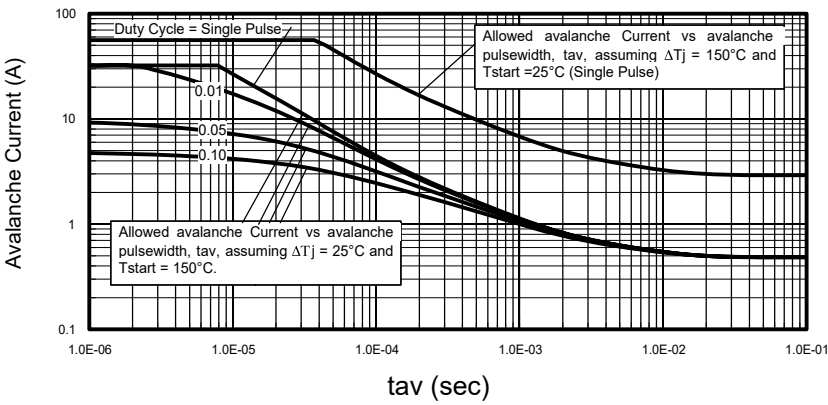
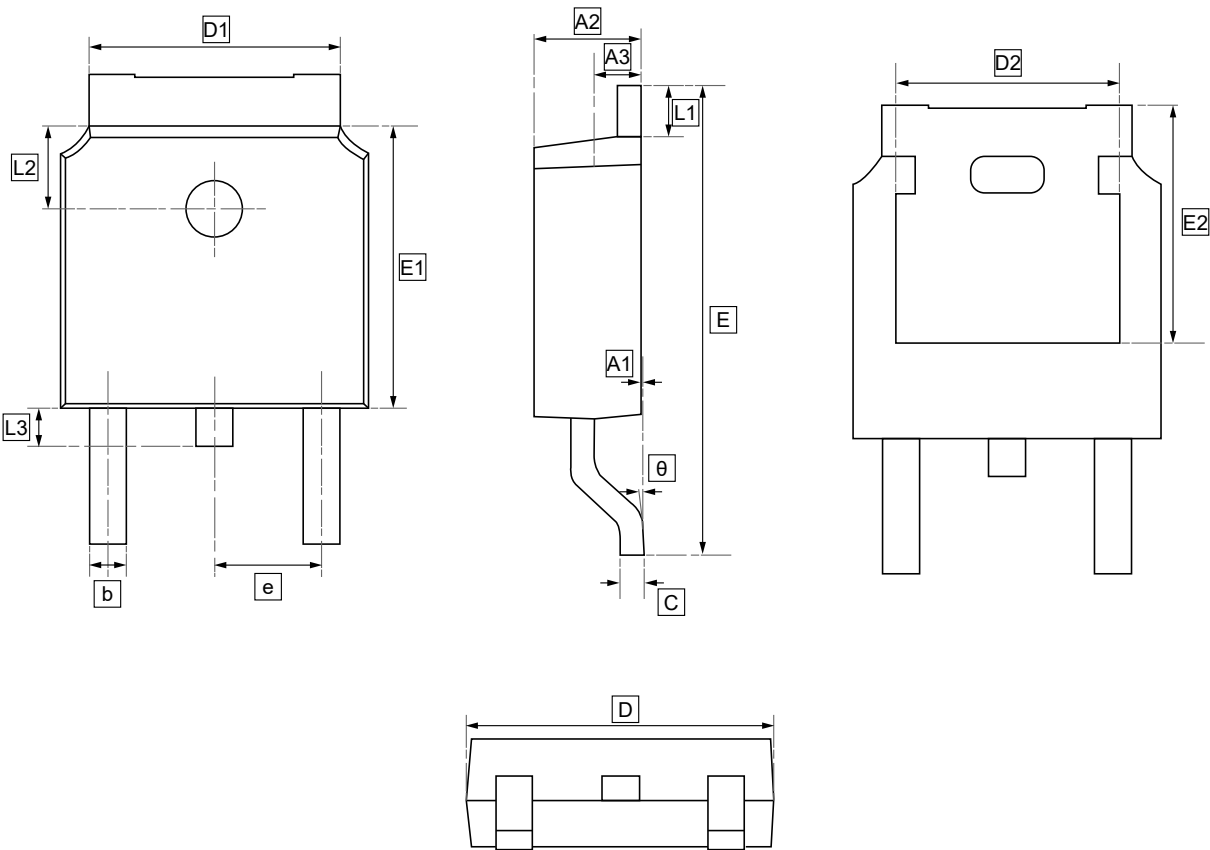


Figure 20: Typical Avalanche Current vs. Pulse width



7.TO-252 Package Outline Dimensions

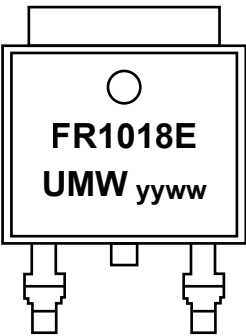


DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286 BSC	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38		1.27	1.90	1.00	8.00



8.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRFR1018ETR	TO-252	2500	Tape and reel



9.Disclaimer

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