UMW FDV301N

20V N-Channel MOSFET

1.Description

This N-Channel logic level enhancement mode field effect transistor is produced using Fairchild's proprietary, high celldensity, DMOS technology. This very high density process isespecially tailored to minimize on-state resistance.

2.Features

- $V_{DS(V)}$=20V
- I_D=6A(V_{GS}=10V)
- $R_{DS(ON)}$<28mΩ(V_{GS}=4.5V)
- $R_{DS(ON)}$<42mΩ(V_{GS}=2.5V)
- $R_{DS(ON)}$<50mΩ(V_{GS}=1.8V)

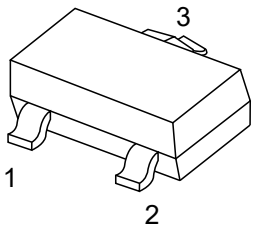
3.Applications

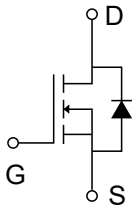
- DC/DC Converters
- Load Switch for Portable Applications

4.Pinning information

Pin	Symbol	Description
1	G	GATE
2	S	SOURCE
3	D	DRAIN

SOT-23





5.Maximum ratings (T_A=25°C unless otherwise noted)

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous DrainCurrent (T_J = 150 °C)	T_C=25°C	I_D	6[a]	A
	T_C=70°C		5.1	
	T_A=25°C		5[b,c]	
	T_A=70°C		4[b,c]	
Pulsed Drain Current		I_{DM}	20	
Continuous Source-Drain Diode Current	T_C=25°C	I_S	1.75	
	T_A=25°C		1.04[b,c]	

Maximum Power Dissipation	T_C=25°C	P_D	2.1	W
	T_C=70°C		1.3	
	T_A=25°C		1.25[b,c]	
	T_A=70°C		0.8[b,c]	
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55 to 150	°C
Soldering Recommendations (Peak Temperature)			260	°C

6.Thermal resistance rating

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [b,d]	t ≤5s	R_{thJA}	80	100	°C/W
Maximum Junction-to-Foot (Drain)	Steady-State	R_{thJF}	40	60	°C/W

Notes:

a. Package limited

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 5 s.

d. Maximum under steady state conditions is 125 °C/W.

e. Based on TC = 25 °C.

7.Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{DS}=0V, I_D=250μA	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D=250μA		25		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-2.6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	0.45		1	V
Gate-Source Leakage	I_{GSS}	V_{DS}=0V, V_{GS}=±8V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V, V_{GS}=0V			1	μA
		V_{DS}=20V, V_{GS}=0V, T_J=70°C			10	
On-State Drain Current[a]	$I_{D(ON)}$	V_{DS}≤5V, V_{GS}=4.5V	20			A
Drain-Source On-State Resistance[a]	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=5A		28		mΩ
		V_{GS}=2.5V, I_D=4.7A		42		
		V_{DS}=1.8V, I_D=4.3A		50		
Forward Transconductance[a]	g_{FS}	V_{DS}=10V, I_D=5A		24		S
Dynamic [b]						
Input Capacitance	C_{iss}	V_{DS}=10V, V_{GS}=0V, f=1MHz		865		pF
Output Capacitanc	C_{oss}			105		
Reverse Transfer Capacitance	C_{rss}			55		
Total Gate Charge	Q_g	V_{DS}=10V, V_{GS}=5V		12	18	nC
		I_D=5A		8.8	14	
Gate Source Charge	Q_{gs}	V_{DS}=10V, V_{GS}=4.5V		1.1		
Gate Drain Charge	Q_{gd}	I_D=5A		0.7		
Gate Resistance	R_g	f=1MHz	0.5	2.4	4.8	Ω
Turn-On DelayTime	$t_{D(on)}$	V_{DD} =10V, R_L=2.2Ω		8	16	ns
Rise Time	t_r	I_D≌4A, V_{GEN}=4.5V		17	26	
Turn-Off DelayTime	$t_{D(off)}$	R_g=1Ω		31	47	
Fall Time	t_f			8	16	

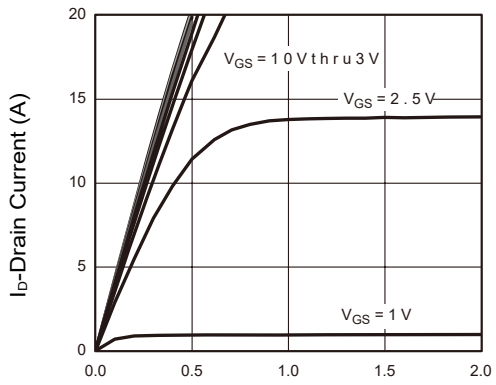
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=10V, R_L=2.2Ω I_D=4A,V_{GEN}=5V Rg=1Ω		5	10	ns
Rise Time	t_r			13	20	ns
Turn-Off Delay Time	$t_{D(off)}$			21	32	ns
Fall Time	t_f			6	12	ns
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C=25°C			1.75	A
Pulse Diode Forward Current [a]	I_{SM}				20	A
Body Diode Voltage	V_{SD}	I_S=4A, V_{GS}=0V		0.75	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F=4A, dI/dt=100A/μs T_J=25°C		12	20	ns
Body Diode Reverse Recovery Charge	Q_{rr}			5	10	nC
Reverse Recovery Fall Time	t_a			7		ns
Reverse Recovery Rise Time	t_b			5		ns

Notes:

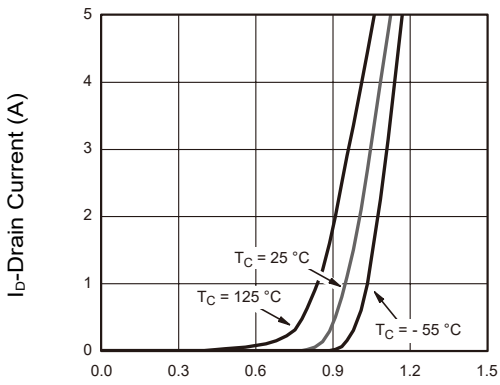
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.

b. Guaranteed by design, not subject to production testing.

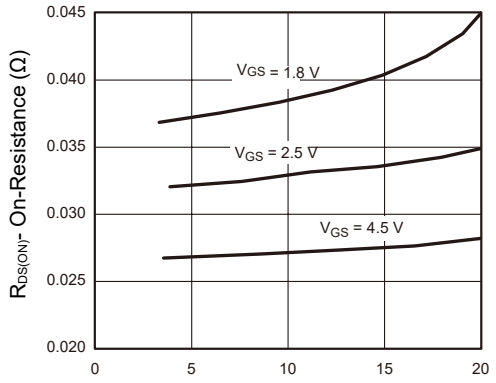
8.1Typical Characterisitics



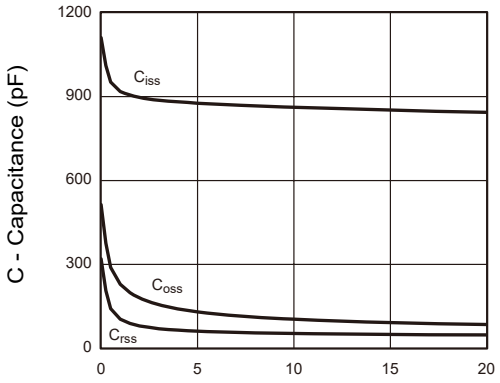
Output Characteristics



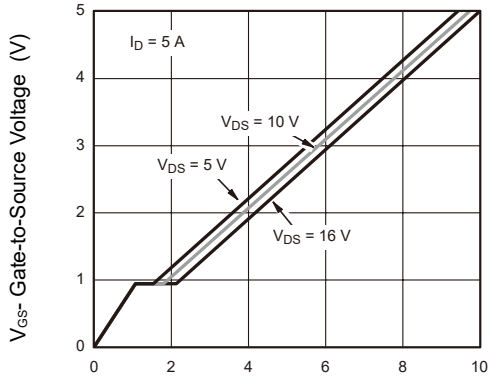
Transfer Characteristics



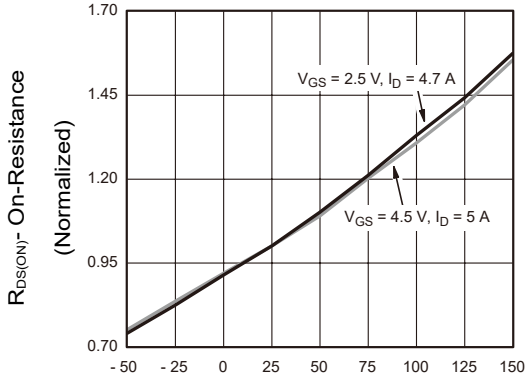
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

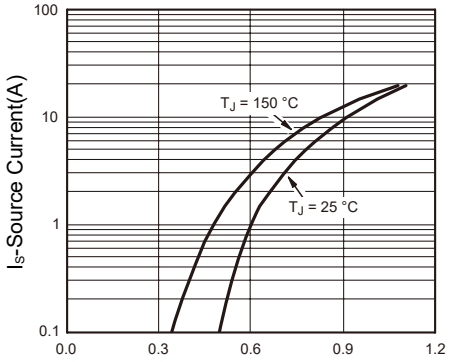


Gate Charge

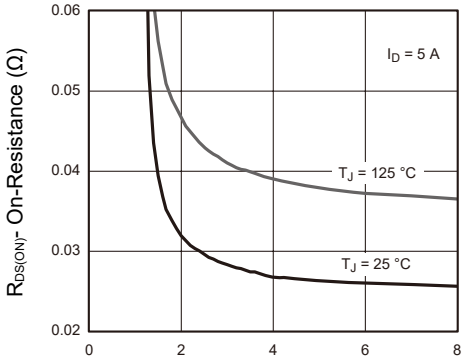


On-Resistance vs. Junction Temperature

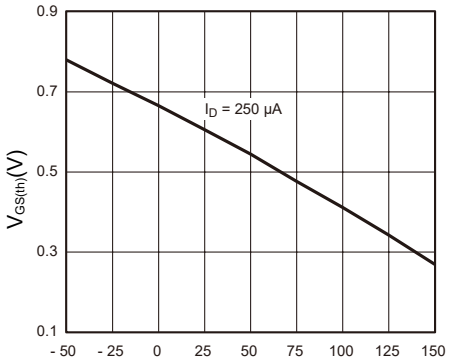
8.2Typical Characterisitics



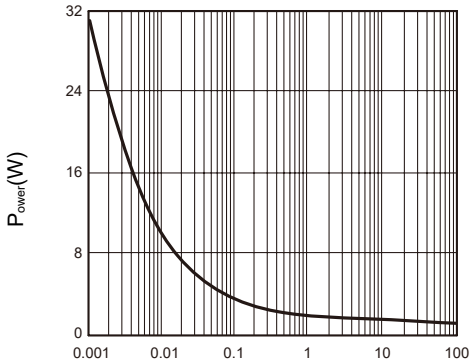
Source-Drain Diode Forward Voltage



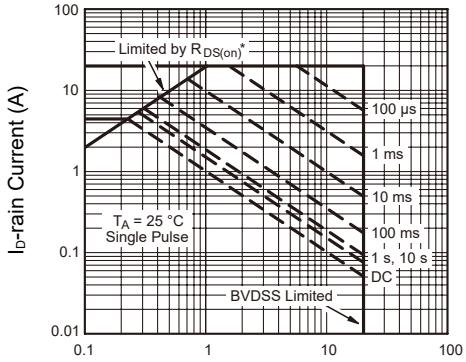
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

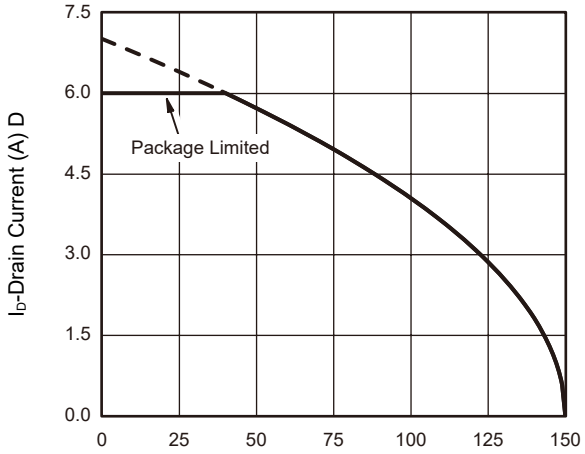


Single Pulse Power, Junction-to-Ambient

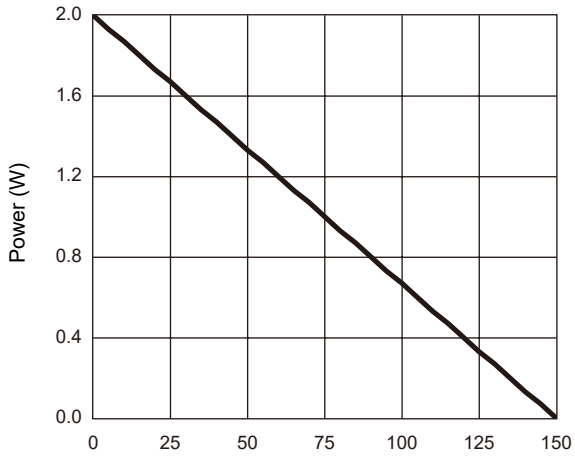


Safe Operating Area, Junction-to-Ambient

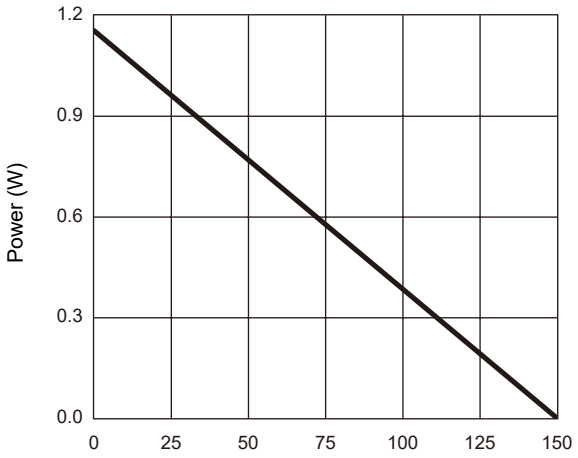
8.3Typical Characterisitics



Current Derating*



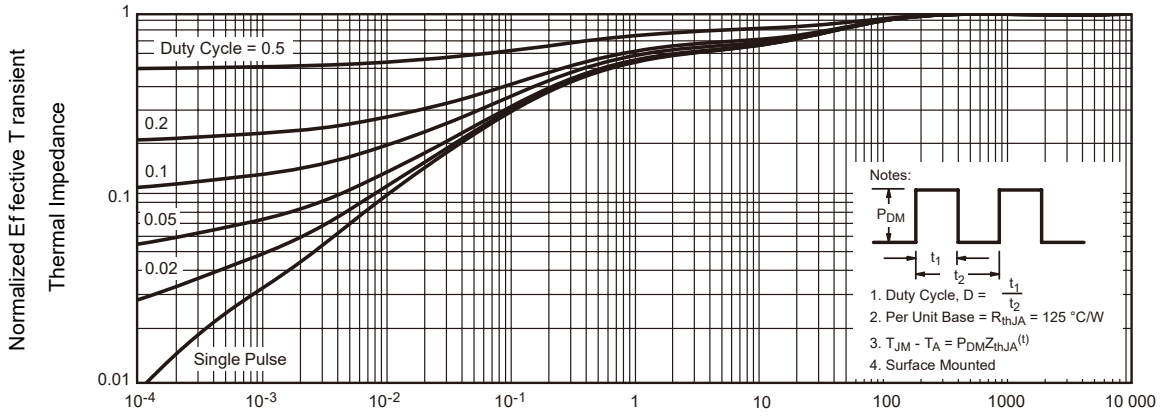
Power Derating, Junction-to-Foot



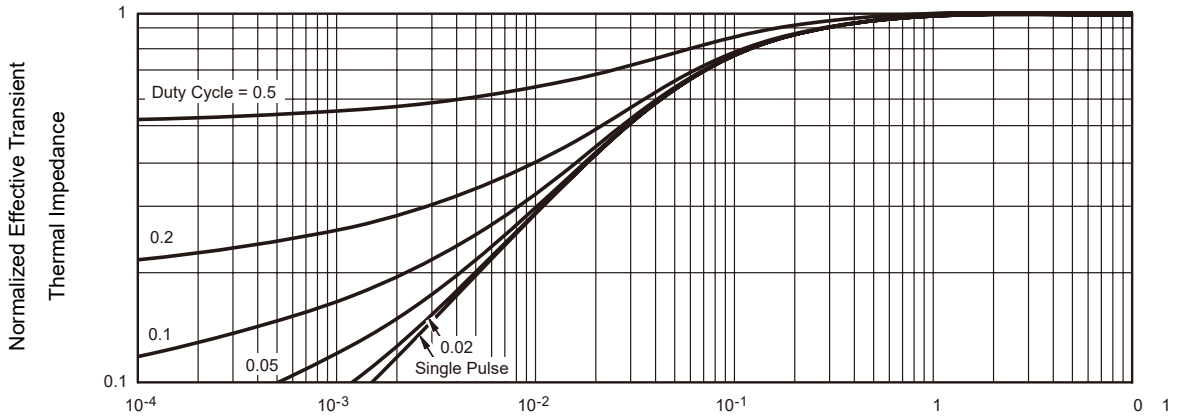
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upperdissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

8.4Typical Characterisitics

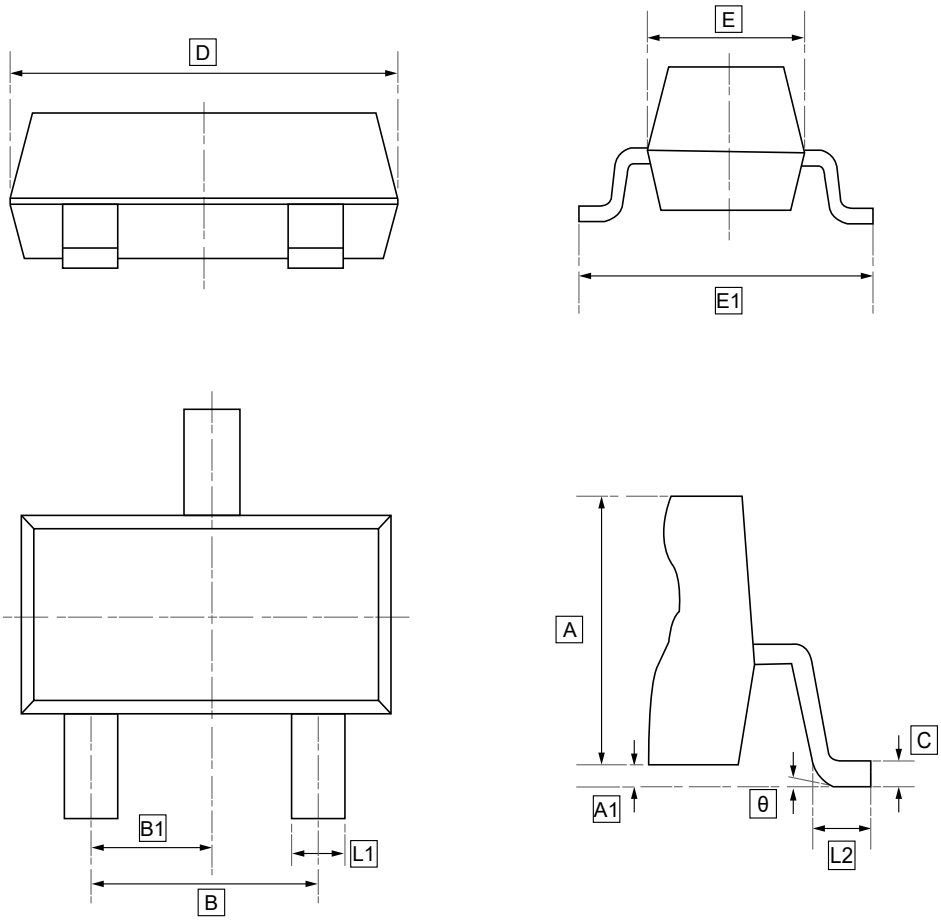


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

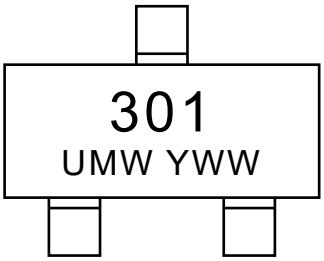
9.SOT-23 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	L1	L2	C	D	E	E1	B	B1	θ
Min	1.050	0.000	0.300	0.350	0.100	2.820	1.500	2.700	1.800	0.950	0°
Max	1.150	0.100	0.500	0.550	0.200	3.020	1.700	2.900	2.000	TYP	8°

10.Ordering information



YWW: Batch Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDV301N	SOT-23	3000	Tape and reel

11.Disclaimer

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