UMW FDD5353

60V N-Channel MOSFET

1.Description

This N-Channel MOSFET is produced using process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

2.Features

- V_{DSS}=60V
- I_D=10.7A(V_{GS}=10V)
- $R_{DS(ON)}$<12.3mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<15.4mΩ(V_{GS}=4.5V)
- RoHS Compliant

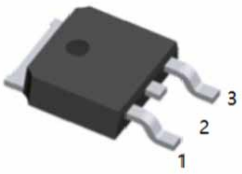
3.Application

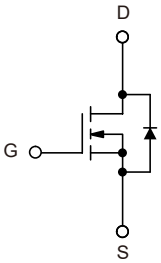
- Inverter
- Synchronous rectifier
- Primary switch

4.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view





5.Absolute Maximum Ratings T_C= 25°C

Parameter			Symbol	Rating	Units
Drain to Source Voltage			V_{DS}	60	V
Gate to Source Voltage			V_{GS}	±20	
Drain Current -Continuous	T_C=25°C		I_D	50	A
-Continuous	T_A=25°C	(Note 1a)		11.5	
-Pulsed				100	
Single Pulse Avalanche Energy		(Note 3)	E_{AS}	253	mJ
Power Dissipation	T_C=25°C		P_D	69	W
Power Dissipation	T_A=25°C	(Note 1a)		3.1	
Operating and Storage Junction Temperature Range			T_J, T_{STG}	-55 to 150	°C/W

6.Thermal Characteristics

Parameter		Symbol	Rating	Units
Thermal Resistance, Junction to Case		$R_{\theta JC}$	1.8	°C/W
Thermal Resistance, Junction to Ambient	(Note 1a)	$R_{\theta JA}$	40	°C/W

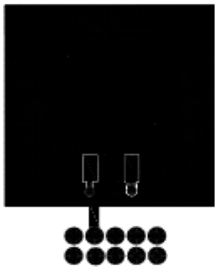
7.Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	60			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D=250μA Referenced to 25°C		77		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=48V, V_{GS}=0V			1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1	1.6	2.5	V
Gate to Source Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D=250μA Referenced to 25°C		-8		mV/°C
Static Drain to Source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=10.7A		10	12	mΩ
		V_{GS}=4.5V, I_D=9.5A		12	15	mΩ
Forward Transconductance	g_{FS}	V_{DD}=5V, I_D=10.7A		41		S
Input Capacitance	C_{iss}	V_{DS}=30V, V_{GS}=0V f=1MHz		2420	3215	pF
Output Capacitance	C_{oss}			215	285	pF
Reverse Transfer Capacitance	C_{rss}			120	180	pF
Gate Resistance	R_g	f=1MHz		1.7		Ω
Turn-On DelayTime	$t_{D(on)}$	V_{DD}=30V, I_D=10.7A V_{GS}=10V, R_{GEN}=6Ω		11	20	ns
Rise Time	t_r			6	11	ns
Turn-Off DelayTime	$t_{D(off)}$			36	58	ns
Fall Time	t_f			4	10	ns
Total Gate Charge	Q_g	V_{GS}=0V to 10V, V_{DD}=30V V_{GS}=0V to 4.5V, I_D=10.7A		46	65	nC
Total Gate Charge	Q_g			23	32	nC
Gate to Source Gate Charge	Q_{gs}			7		nC
Gate to Drain “Miller” Charge	Q_{gd}			9		nC
Source to Drain Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=10.7A (Note 2)		0.8	1.3	V
		V_{GS}=0V, I_S=2.6A (Note 2)		0.7	1.2	V
Reverse Recovery Time	t_{rr}	I_F=10.7A, di/dt=100A/μs		28	45	ns
Reverse Recovery Charge	Q_{rr}			21	34	nC

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.

$R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 40°C/W when mounted on a 1 in ^{2} pad of 2 oz copper

b) 96°C/W when mounted on a minimum pad.

2: Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3: E_{AS} of 253mJ is based on starting T_J=25°C, L=3mH, I_{AS}=13A, V_{DD}=60V, V_{GS}=10V. 100% test at L = 0.1mH, I_{AS}=41A.

8.1Typical characteristic

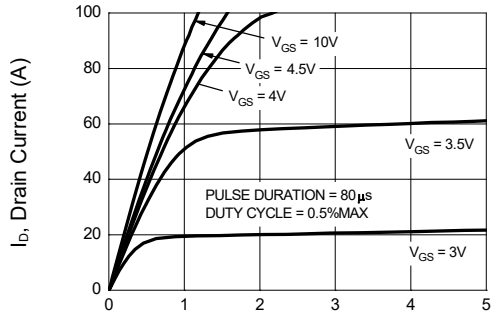


Figure 1: On-Region Characteristics

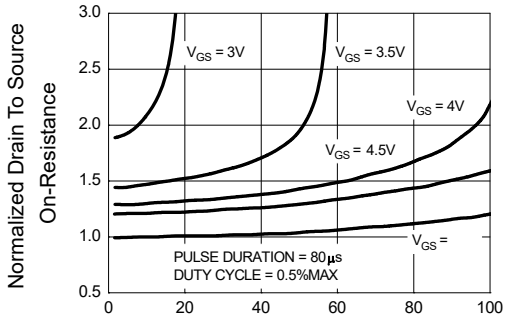


Figure 2: Normalized On-Resistance vs Drain Current and Gate Voltage

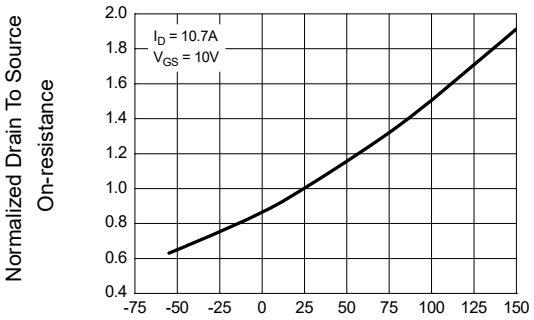


Figure 3: Normalized On Resistance vs Junction Temperature

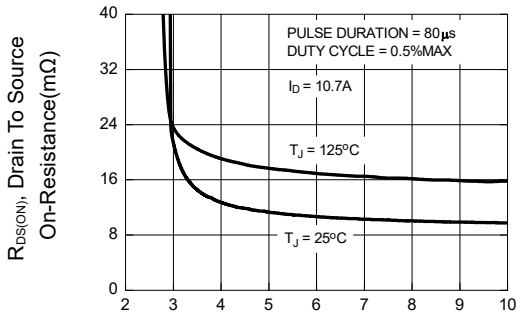


Figure 4: On-Resistance Variation with Gate-to-Source Voltage

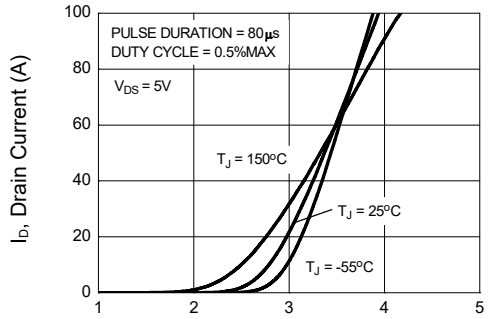


Figure 5: Transfer Characteristics

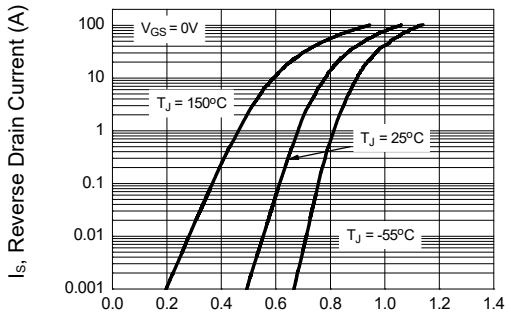


Figure 6: Source to Drain Diode Forward Voltage vs Source Current

8.2Typical characteristic

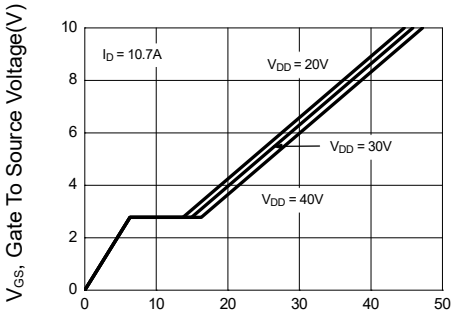


Figure 7: Gate Charge Characteristics

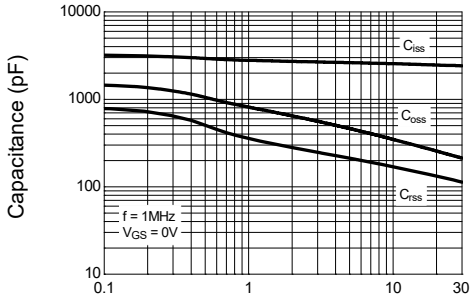


Figure 8: Capacitance vs Drain to Source Voltage

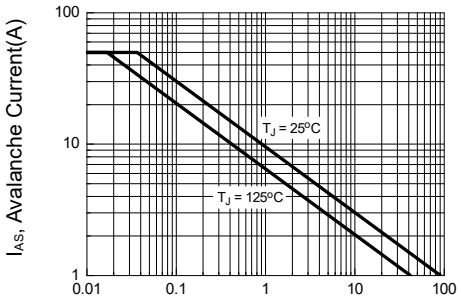


Figure 9: Unclamped Inductive Switching Capability

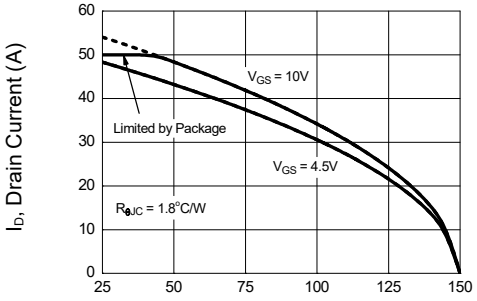


Figure 10: Maximum Continuous Drain Current vs Case Temperature

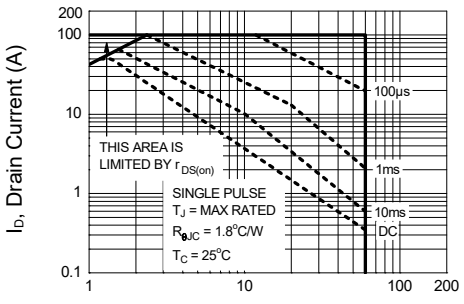


Figure 11: Forward Bias Safe Operating Area

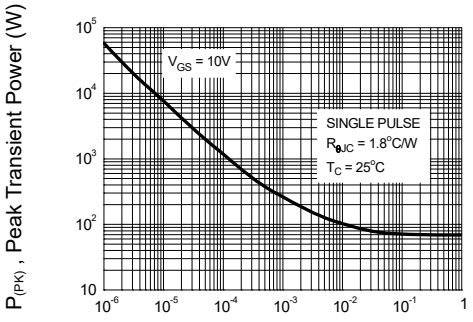
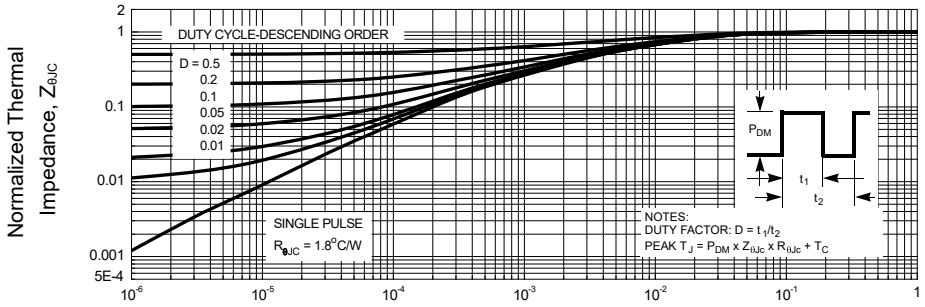


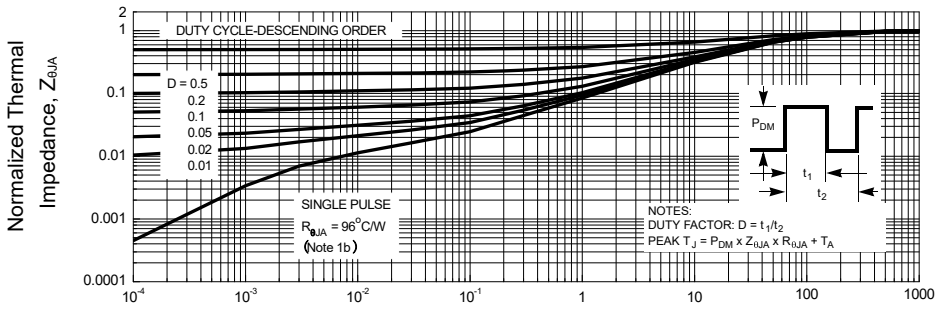
Figure 12: Single Pulse Maximum Power Dissipation

8.3Typical characteristic



t_1 , Rectangular Pulse Duration (sec)

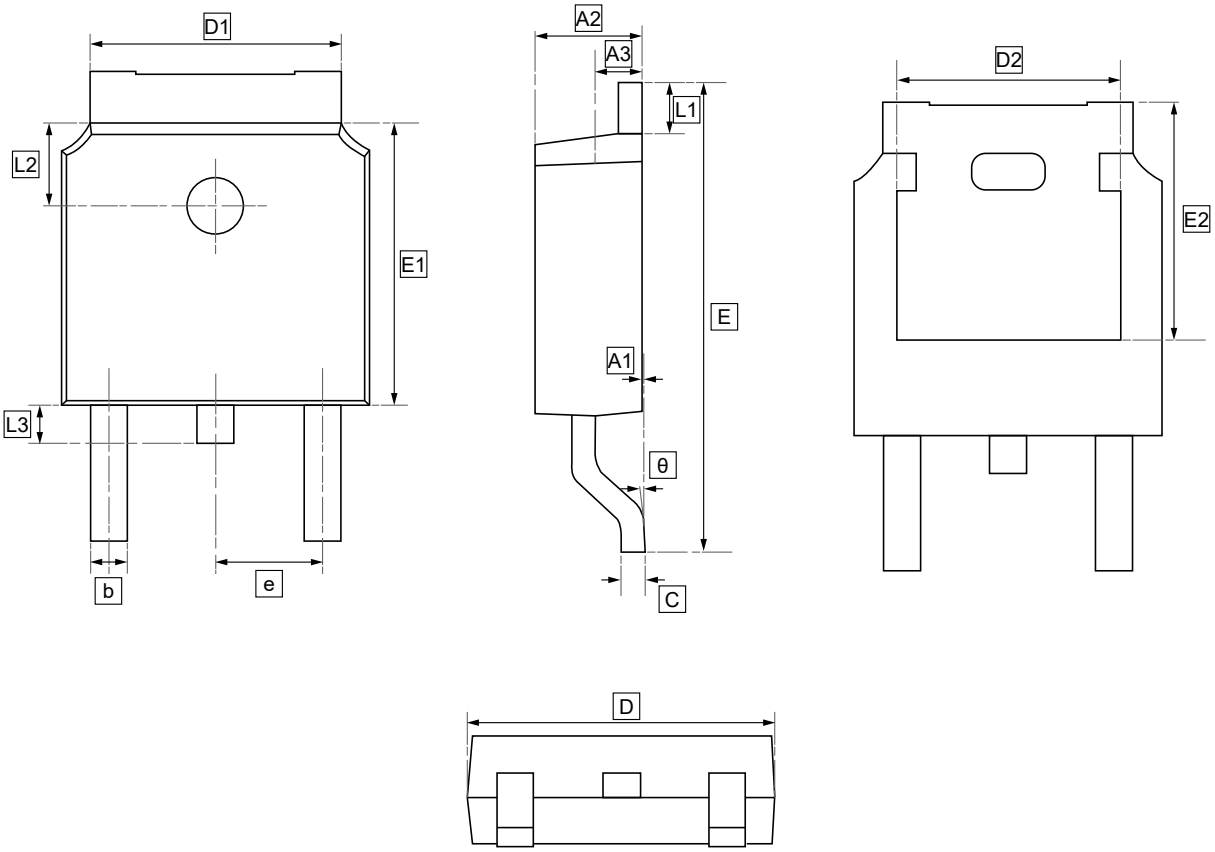
Figure 13: Transient Thermal Response Curve



t, Rectangular Pulse Duration (sec)

Figure 13: Transient Thermal Response Curve

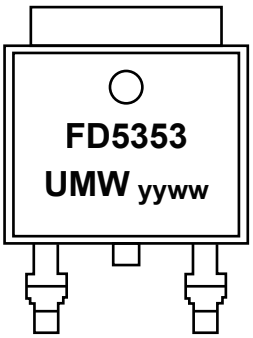
9.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

10.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDD5353	TO-252	2500	Tape and reel

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