UMW FDN340P

SOT-23 Plastic-Encapsulate MOSFETS

1.Description

This P-Channel Logic Level MOSFET is produced using FairchildSemiconductor advancedPower Trenchprocess that hasbeen especiallytailored to minimizethe on-state resistance and yet maintain low gatecharge for superior switchingperformance.

2.Features

- $V_{DS(V)}$=-20V
- I_D=-2A
- $R_{DS(ON)}$<70mΩ(V_{GS}=-4.5V)
- $R_{DS(ON)}$<110mΩ(V_{GS}=-2.5V)
- $R_{DS(ON)}$<210mΩ(V_{GS}=-1.8V)

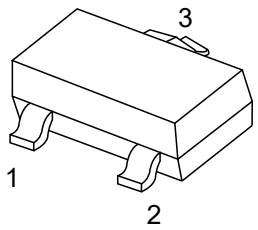
3.Application

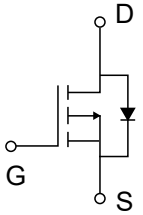
- Battery protection
- Load switch
- Battery management

4.Pinning information

Pin	Symbol	Description
1	G	GATE
2	S	SOURCE
3	D	DRAIN

SOT-23





5.Maximum ratings (T_A=25°C unless otherwise noted)

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±8	V
Continuous Drain Current	I_D	-2	A
Pulsed Drain Current	I_{DM}	-10	A
Power Dissipation	P_D	1.1	W
Thermal Resistance from Junction to Ambient (t≤10s)	$R_{\theta JA}$	250	°C/W
Operating Junction	T_J	150	°C
Storage Temperature	T_{STG}	-55~+150	°C

6.Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=-250μA	-20			V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-0.4		-1.5	V
Gate-source leakage	I_{GSS}	V_{GS}=±8V, V_{DS}=0V			±100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS}=-16V, V_{GS}=0V			-1	μA
Drain-source on-state resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-2A		52	70	mΩ
		V_{GS}=-2.5V, I_D=-1.7A		78	110	mΩ
		V_{GS}=-1.8V, I_D=-1.2A			210	mΩ
Forward transconductance	g_{FS}	V_{DS}=-4.5V, I_D=-2A		8		S
Diode forward voltage	V_{SD}	I_S=-1A, V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Input Capacitance	C_{iss}	V_{DS}=-10V, V_{GS}=0V, f=1MHz		600		pF
Output Capacitance	C_{oss}			175		pF
Reverse Transfer Capacitance	C_{rss}			80		pF
Total gate charge	Q_g	V_{DS}=-10V, V_{GS}=-4.5V I_D=-2A		8		nC
Gate-source charge	Q_{gs}			1.3		nC
Gate-drain charge	Q_{gd}			2.2		nC
Gate resistance	R_g	f=1MHz	0.5		3.2	Ω
Switchingbtr						
Turn-on delay time	$t_{D(on)}$	V_{DS}=-10V, R_L=3.5Ω, I_D≈-1A V_{GEN}=-4.5V, R_G=3Ω		6		ns
Rise time	t_r			9		ns
Turn-off delay time	$t_{D(off)}$			31		ns
Fall time	t_f			26		ns
Drain-source body diode characteristicstr						
Continuous Source-Drain Diode Current	I_S	T_C=25°C			-1.2	A
Pulsed Diode forward Current	I_{SM}				-10	A

Note :

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t < 10 sec.
3. Pulse Test : Pulse Width≤300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

7.1Typical Characterisitics

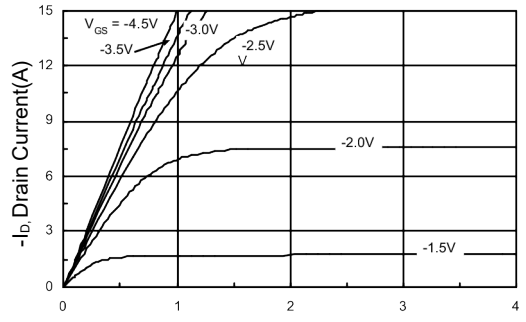


Figure 1: On-Region Characteristics.

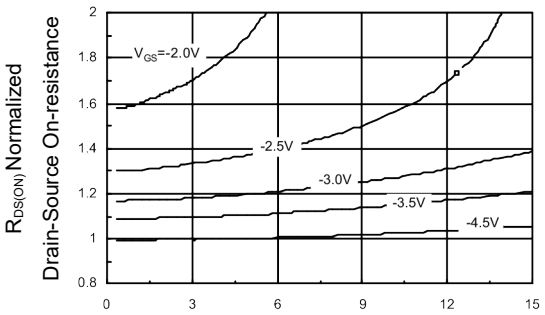


Figure 2: On-Resistance Variation with Drain Current and Gate Voltage.

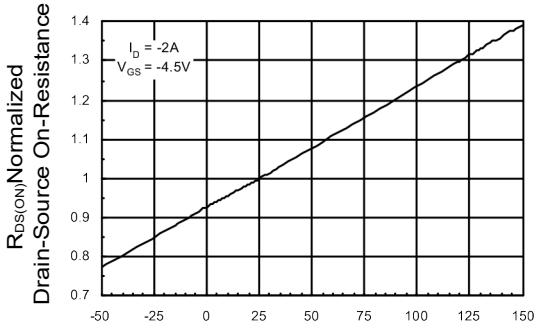


Figure 3: On-Resistance Variation with Temperature.

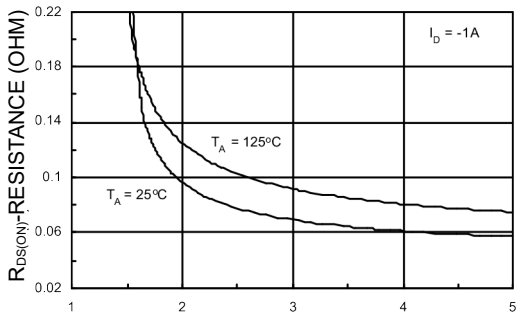


Figure 4: On-Resistance Variation with Gate-to-Source Voltage.

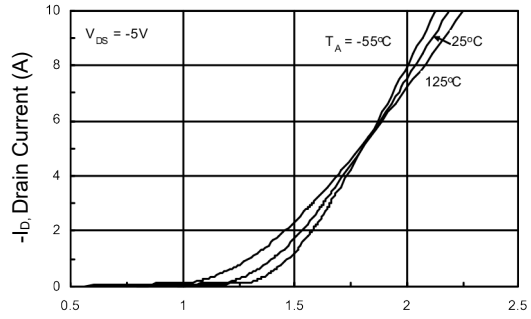


Figure 5: Transfer Characteristics.

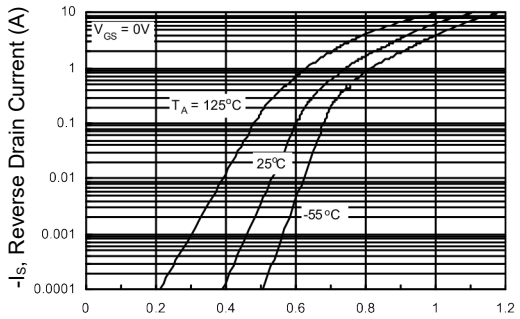


Figure 6: . Body Diode Forward Voltage Variation with Source Current and Temperature.

7.2Typical Characterisitics

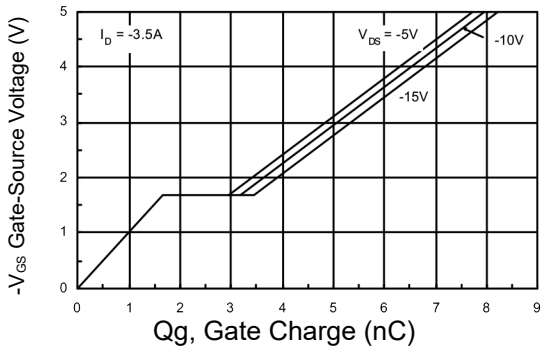


Figure 7: Gate-Charge Characteristics

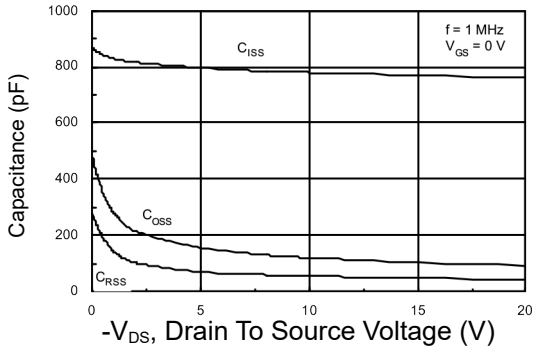


Figure 8: Capacitance Characteristics

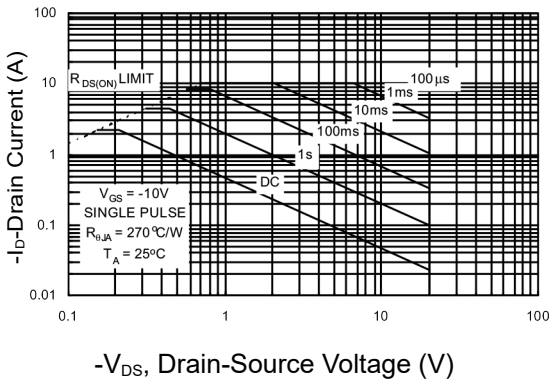


Figure 9: Maximum Safe Operating Area.

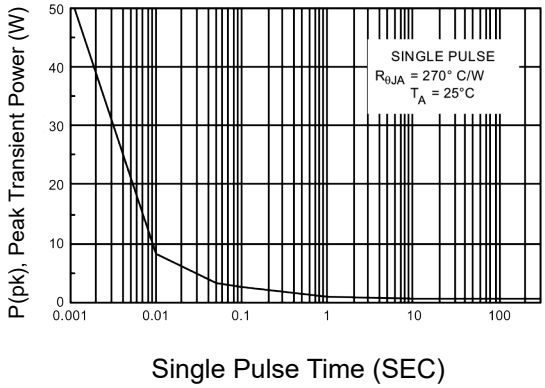


Figure 10: Single Pulse Maximum Power Dissipation.

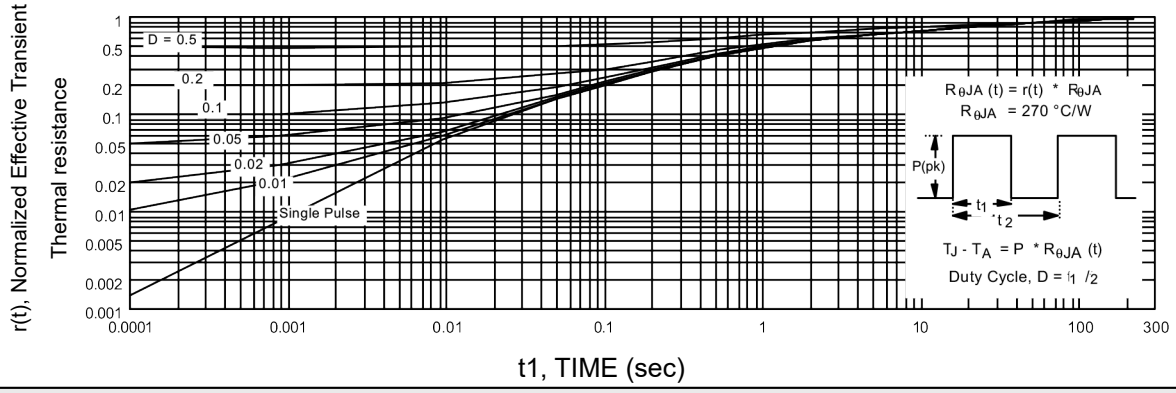
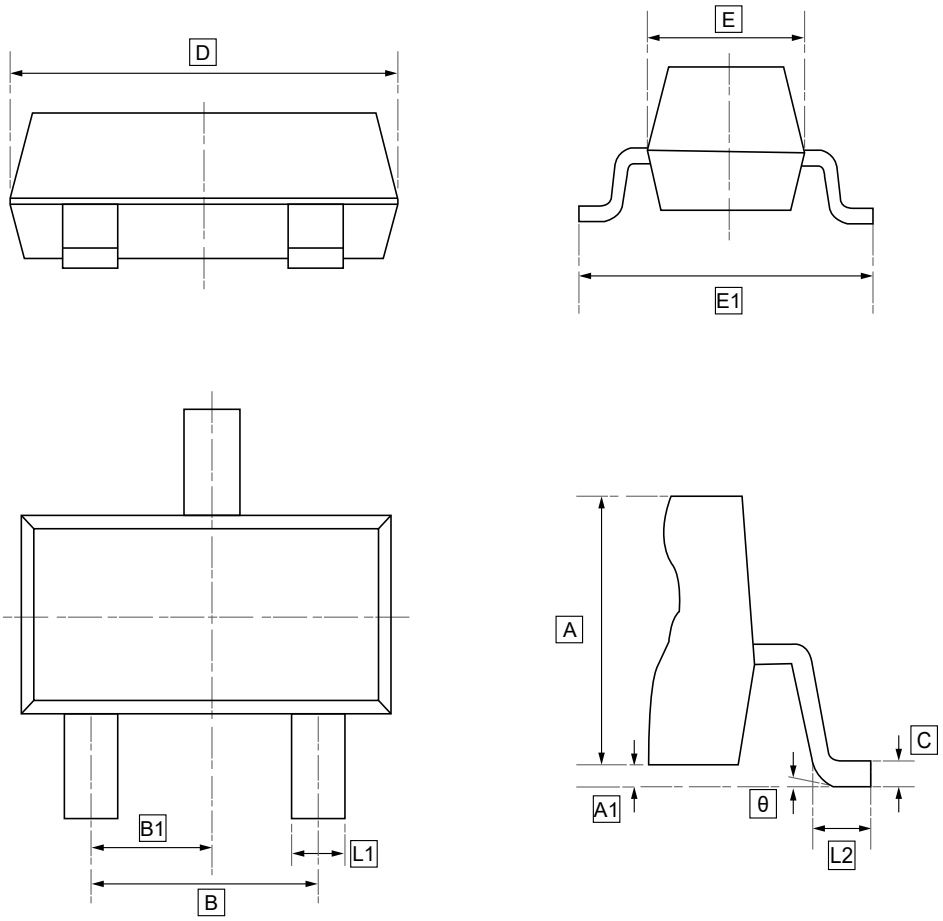


Figure 11. Transient Thermal Response Curve.

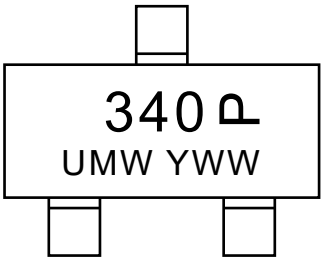
8.SOT-23 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	L1	L2	C	D	E	E1	B	B1	θ
Min	1.050	0.000	0.300	0.350	0.100	2.820	1.500	2.700	1.800	0.950	0°
Max	1.150	0.100	0.500	0.550	0.200	3.020	1.700	2.900	2.000	TYP	8°

9.Ordering information



YWW: Batch Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDN340P	SOT-23	3000	Tape and reel

10.Disclaimer

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