UMW NDS8435A

-30V P-Channel MOSFET

1.Description

SOP-8 P-Channel enhancement mode power field effect transistors are produced using,high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance

2.1Features

- $V_{DS\ (V)}$=-30V
- I_D=-7.9A(V_{GS}=-10V)
- $R_{DS(ON)}$<23mΩ(V_{GS}=-10V)
- $R_{DS(ON)}$<35mΩ(V_{GS}=-4.5V)

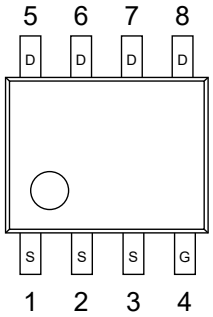
2.2Features

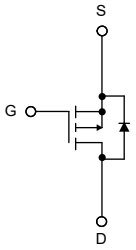
- High power and current handling capability in a widely used surface mount package.
- High density cell design for extremely low $R_{DS(ON)}$

3.Pinning information

Pin	Symbol	Description
1,2,3	S	SOURCE
4	G	GATE
5,6,7,8	D	DRAIN

SOP-8





4.Absolute Maximum Ratings T_A= 25°C

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current - Continuous	(Note 1a)	I_D	-7.9	A
-Pulsed			-25	A
Power Dissipation for Single Operation	(Note 1a)	P_D	2.5	W
	(Note 1b)		1.2	W
	(Note 1c)		1	W
Temperature Range		T_J, T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter		Symbol	Rating	Units
Thermal Resistance, Junction-to-Ambient	(Note 1a)	$R_{\theta JA}$	50	°C/W
Thermal Resistance, Junction-to-Case	(Note 1)	$R_{\theta JC}$	25	°C/W

6.Electrical Characteristic (T_A=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-30			V
Zero Gate Voltage Drain Curent	I_{DSS}	V_{DS}=-24V, V_{GS}=0V			-1	μA
		T_J=55°C			-10	μA
Gate - Body Leakage, Forward	I_{GSSF}	V_{GS}=20V, V_{DS}=0V			100	nA
Gate - Body Leakage, Reverse	I_{GSSR}	V_{GS}=-20V, V_{DS}=0V			-100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1	-1.3	-3	V
		T_J=125°C	-0.7	-1	-2.2	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-7.9A		20	23	mΩ
		V_{GS}=-4.5V, I_D=-6.5A		30	35	mΩ
On-State Drain Current	$I_{D(ON)}$	V_{GS}=-10V, V_{DS}=-5V	-25			A
		V_{GS}=-4.5V, V_{DS}=-5V	-10			A
Forward Transconductance	g_{FS}	V_{DS}=-10V, I_D=-7.9A		-17		S
Input Capacitance	C_{iss}	V_{DS}=-15V, V_{GS}=0V, f=1MHz		1800		pF
Output Capacitance	C_{oss}			950		pF
Reverse Transfer Capacitance	C_{rss}			240		pF
Turn - On Delay Time	$t_{D(on)}$	V_{DD}=-10V, I_D=-1A V_{GEN}=-10V, R_{GEN}=6Ω		11	22	ns
Turn - On Rise Time	t_r			20	35	ns
Turn - Off Delay Time	$t_{D(off)}$			95	180	ns
Turn - Off Fall Time	t_f			46	100	ns
Total Gate Charge	Q_g	V_{DS}=-15V, I_D=-7.9A, V_{GS}=-10V		48	67	nC
Gate-Source Charge	Q_{gs}			6		nC
Gate-Drain Charge	Q_{gd}			12		nC
Maximum Continuous Drain-Source Diode Forward Current	I_S				-2.1	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=-2.1A (Note 2)		-0.74	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

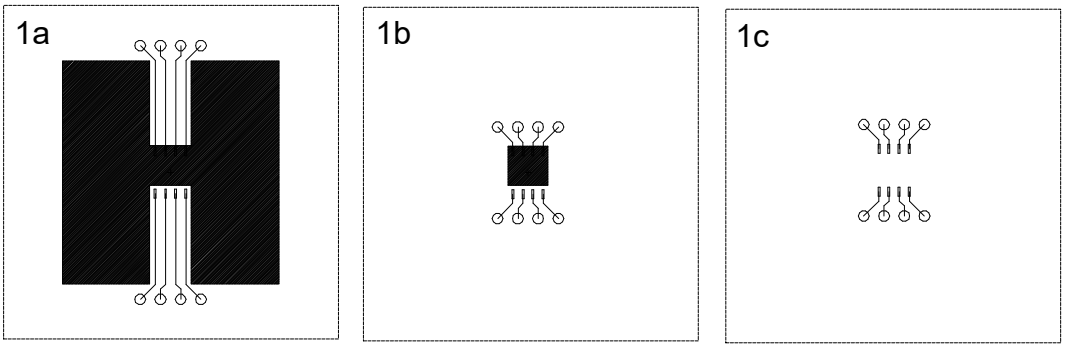
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA(t)}} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA(t)}} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 in^2 pad of 2oz copper.

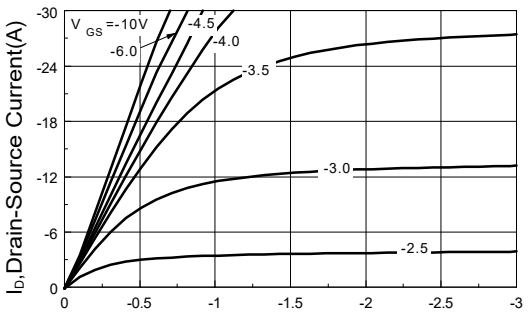
c. 125°C/W when mounted on a 0.006 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

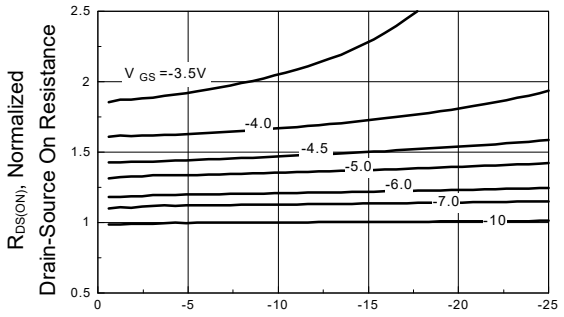
2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%.

7.1Typical characteristic



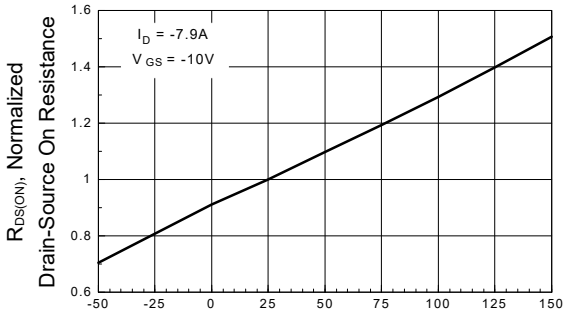
$V_{DS,}$ Drain To Source Voltage (V)

Figure 1: On-Region Characteristics



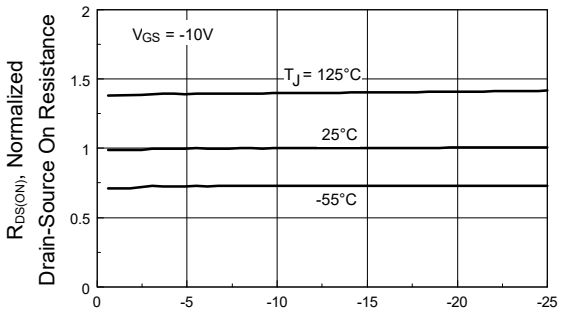
I_D, Drain Current (A)

Figure 2: On-Resistance Variation with Gate Voltage and Drain Current



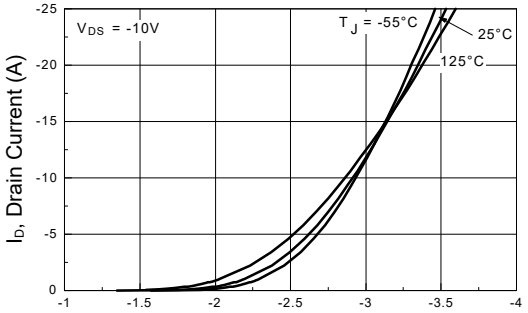
T_J, Junction Temperature (°C)

Figure 3: On-Resistance Variation with Temperature



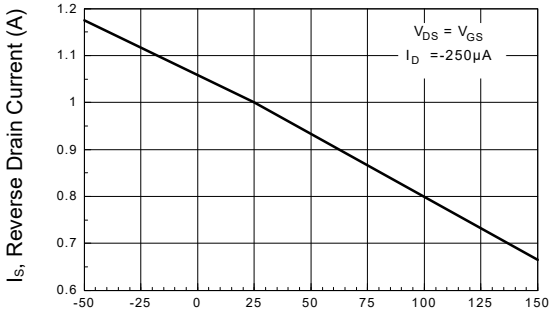
I_D, Drain Current (A)

Figure 4: On-Resistance Variation with Drain Current and Temperature.



V_{GS}, Gate To Source Voltage (V)

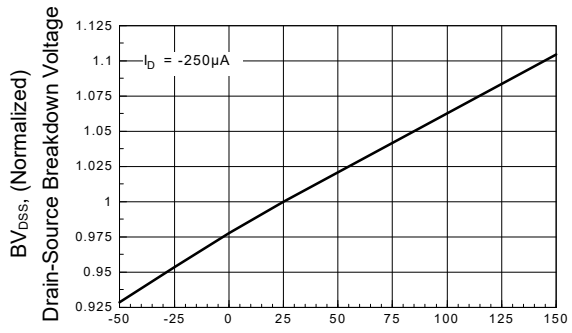
Figure 5: Transfer Characteristics



T_J, Junction Temperature (°C)

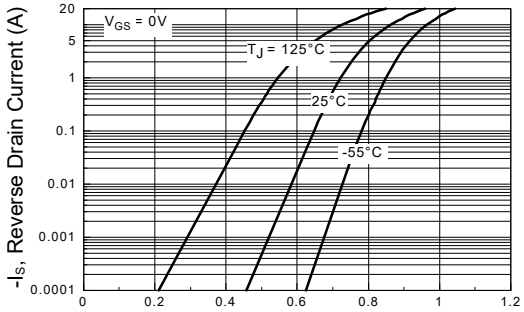
Figure 6: Gate Threshold Variation with Temperature.

7.2Typical characteristic



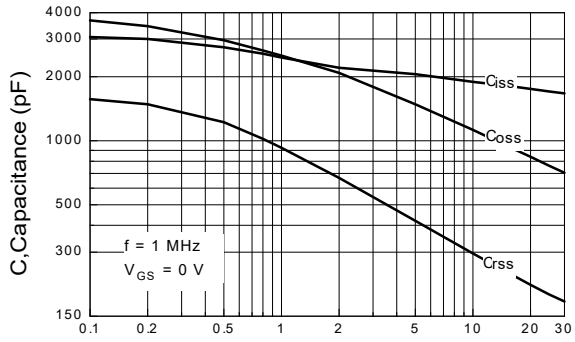
T_J,Junction Temperature (°C)

Figure 7: Breakdown Voltage Variation with Temperature



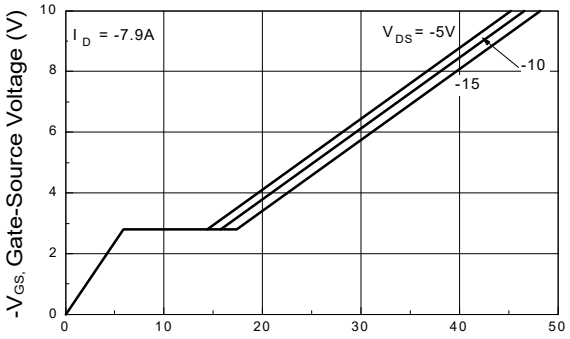
$-V_{SD}$,Body Diode Forward Voltage (V)

Figure 8: Body Diode Forward Voltage Variation with Current and Temperature



$-V_{DS}$, Drain-source Voltage (V)

Figure 9: Capacitance Characteristics



Q_G, Total Gate Charge (nC)

Figure 10: Gate Charge Characteristics

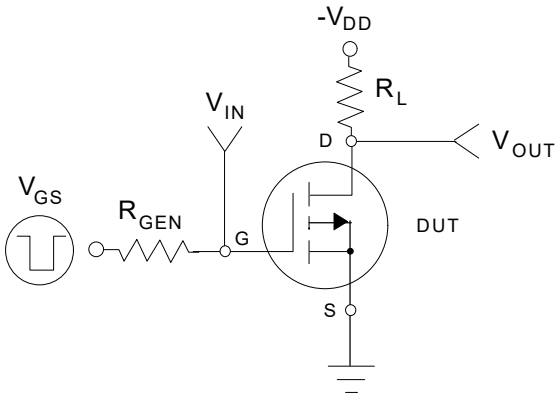


Figure 11: Switching Test Circuit

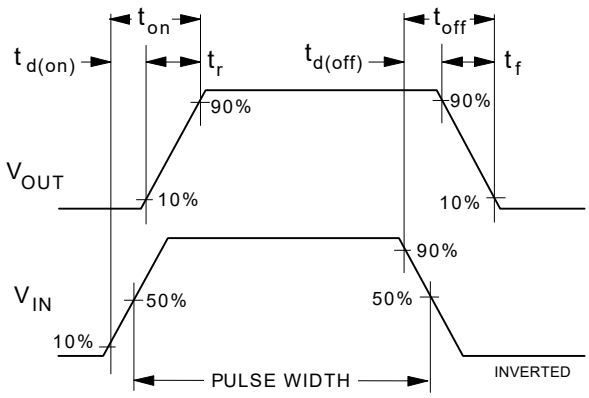


Figure 12: Switching Waveforms

7.3Typical characteristic

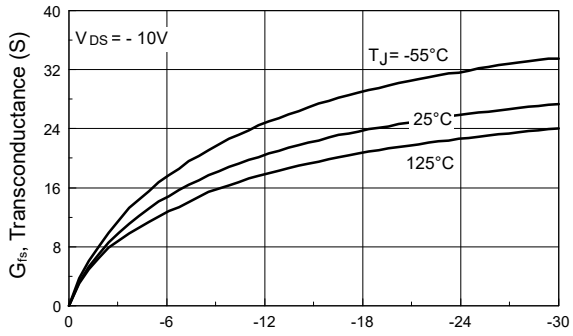


Figure 13: Transconductance Variation with Drain Current and Temperature

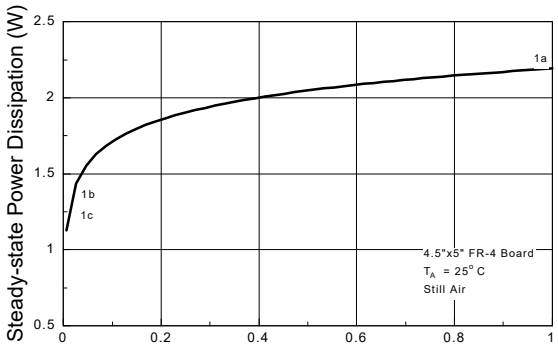


Figure 14: SOT-223 Maximum Steady- tate Power Dissipation versus CopperMounting Pad Area

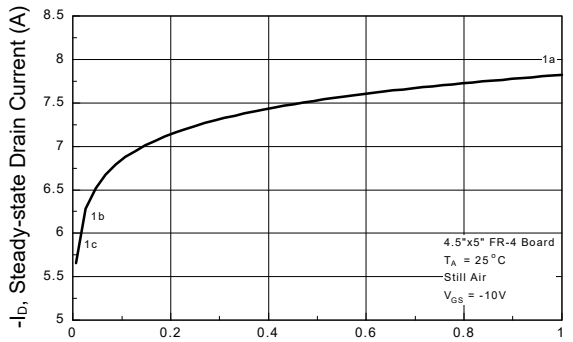


Figure 15:Maximum Steady-State Drain Current versus Copper Mounting PadArea

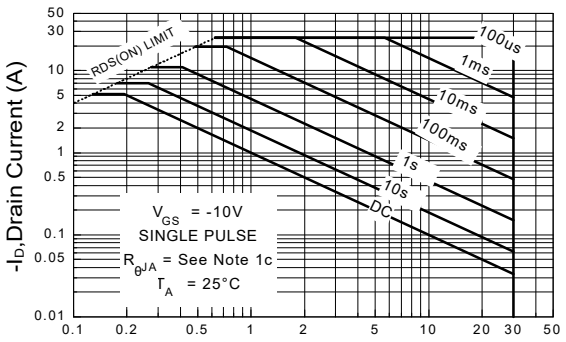


Figure 16: Maximum Safe Operating Area

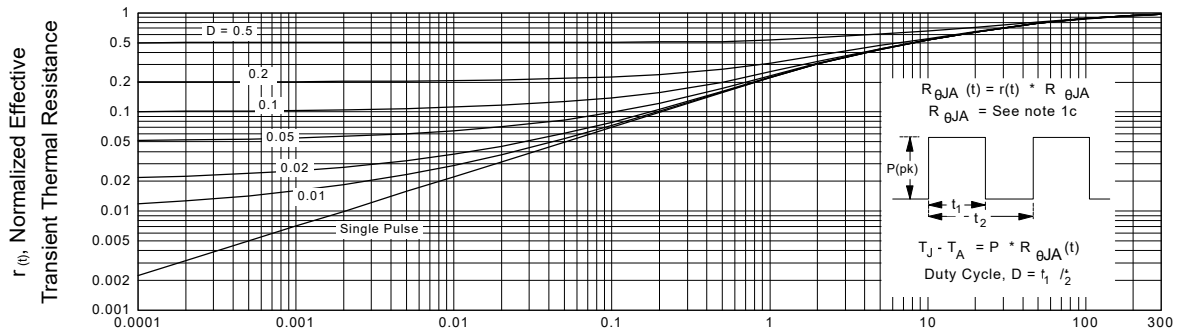
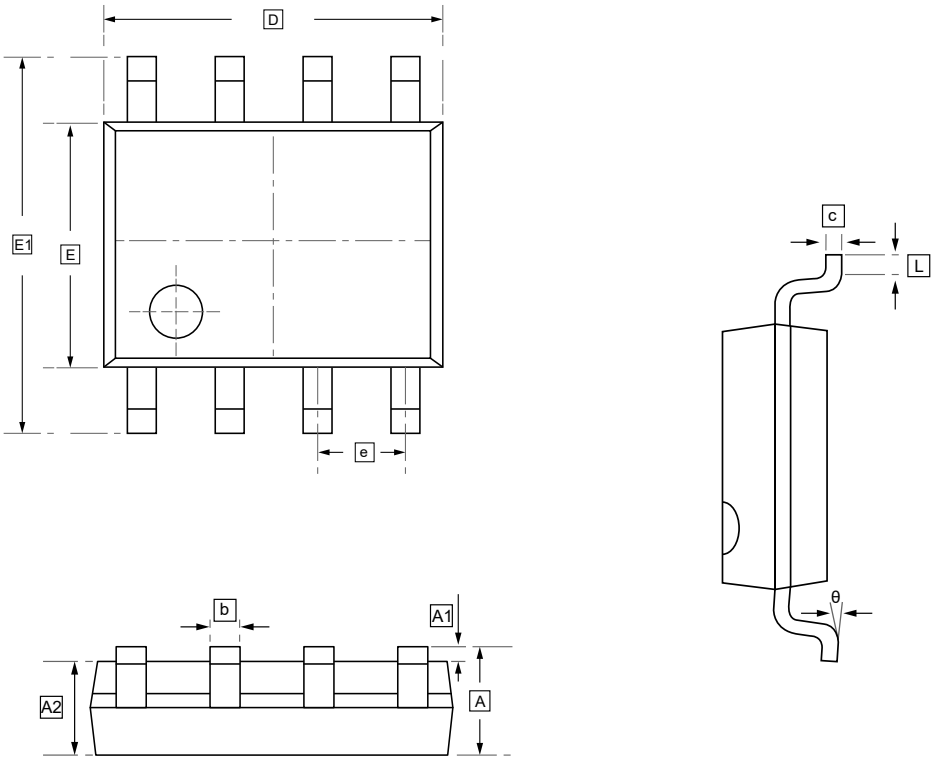


Figure 17: Transient Thermal Response Curve

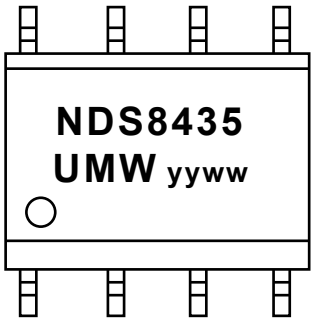
8.SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW NDS8435A	SOP-8	3000	Tape and reel

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