UMW SLVU2.8-4.TBT

2.8V TVS Array For ESD and Latch-Up Protection

1.Description

The SLVU2.8-4.TBTis designed to protect low voltage,CMOS semiconductors from transients caused by electrostatic discharge (ESD),cable discharge events(CDE), lightning and other induced voltage surges. Low capacitance compensation diode is integrated into the TVS to lower the typical capacitance to 6pF per line.

2.Mechanical Characteristics

- Package: SOP-8
- Lead Finish: Matte Tin
- Case Material: “Green” Molding Compound.
- UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminal Connections: See Diagram Below
- Marking Information: See Below

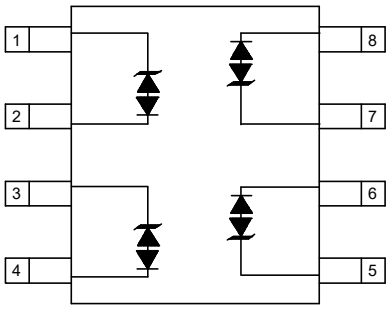
3.Features

- 100W peak pulse power(8/20μs)
- Protects two line pairs(four lines)
- Ultra low leakage: nA level
- Low operating voltage: 2.8V
- Low capacitance
- Ultra low clamping voltage
- JEDEC SO-8 package
- Complies with following standards:
  – IEC 61000-4-2 (ESD) immunity test
  Air discharge: ±30kV
  Contact discharge: ±30kV
  – IEC61000-4-4 (EFT) 40A (5/50ns)
  – IEC61000-4-5 (Lightning) 10A (8/20μs)
- RoHS Compliant

4.Applications

- Base Station
- Analog Inputs
- Switch Systems
- 10/100/1000 Ethernet
- WAN/LAN Equipment
- Desktops, Servers, and Notebooks
- Low Voltage Interfaces

5.Pinning information



SOP-8

6.Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Parameter	Symbol	Value	Units
Peak Pulse Power (8/20μs)	P_{PK}	100	W
Peak Pulse Current (8/20μs)	I_{PP}	10	A
ESD per IEC 61000-4-2(Air)	V_{ESD}	±30	kV
ESD per IEC 61000-4-2(Contact)		±30	kV
Junction Temperature Range	T_J	-40 to 125	°C
Storage Temperature Range	T_{STG}	-55 to 150	°C

7.Electrical Characteristics (T_A=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reverse Working Voltage	V_{RWM}				2.8	V
Punch-Through Voltage	V_{PT}	I_{PT}=2μA	3	3.8	4.3	V
Snap-Back Voltage	V_{SB}	I_{SB}=50mA	2.8			
Reverse Leakage Current	I_R	V_{RWM}=2.8V			1	μA
Clamping Voltage	V_C	I_{PP}=1A (8 x 20μs pulse)			5.5	V
		I_{PP}=10A (8 x 20μs pulse)			10	V
Variation in capacitance with reverse bias		Pins 1,8 to 2,7 and pins 3,6 to 4,5 V_R=0 to 2.8V, f=1MHz		1.3		pF
Junction Capacitance	C_J	Pins 1,8 to 2,7 and pins 3,6 to 4,5 V_R=2.8V, f=1MHz		4.5	6	pF

8.Typical characteristic

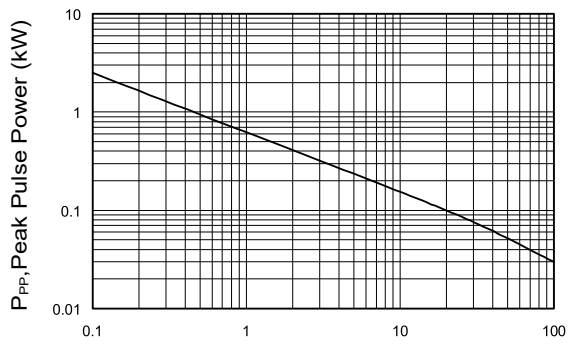


Figure 1: Non-Repetitive Peak Pulse Power vs. Pulse Time

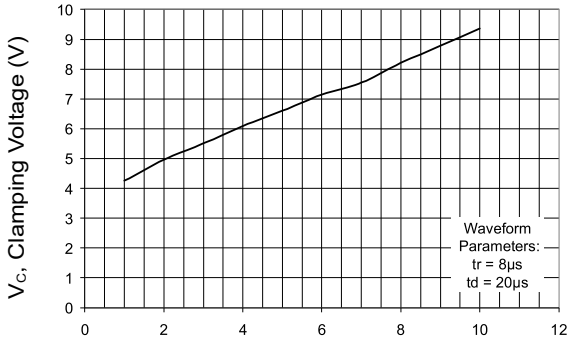


Figure 2: Clamping Voltage vs. Peak Pulse Current

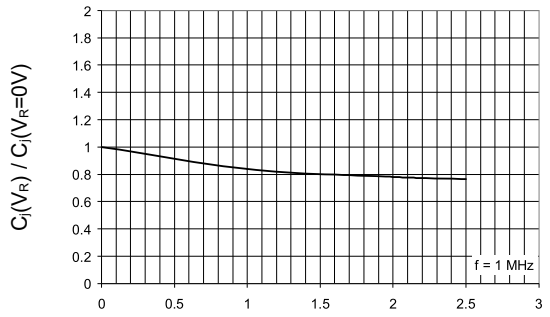


Figure 3: Normalized Junction Capacitance vs. Reverse Voltage

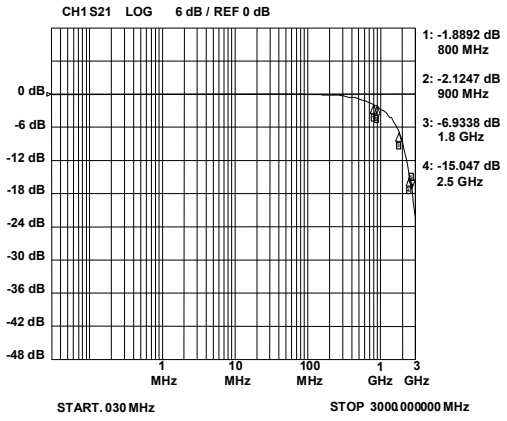


Figure 4: Typical Insertion Loss (S21)

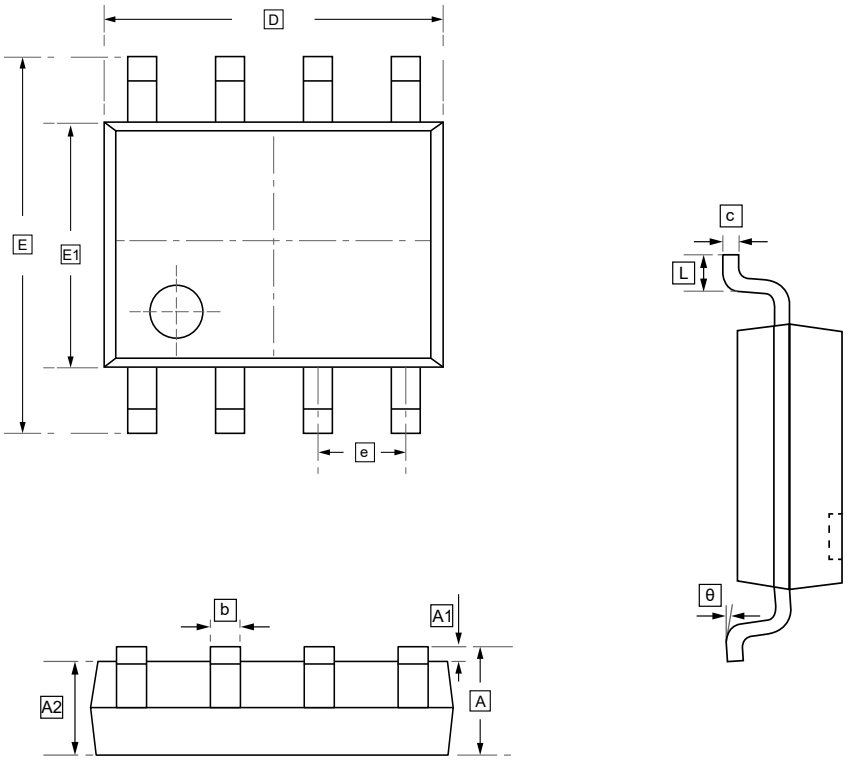
Note: Data is taken with a 10x attenuator

Figure 5: ESD Clamping (8kV Contact per IEC 61000-4-2)

Note: Data is taken with a 10x attenuator

Figure 6: ESD Clamping (-8kV Contact per IEC 61000-4-2)

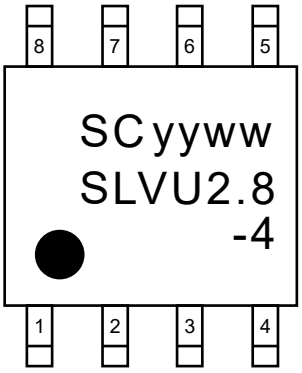
9.SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	e	E	E1	L	θ
Min	1.350	0.100	1.350	0.330	0.170	4.800	1.270	5.800	3.800	0.400	0°
Max	1.750	0.250	1.550	0.510	0.250	5.000	BSC	6.200	4.000	1.270	8°

10.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW SLVU2.8-4.TBT	SOP-8	500	Tape and reel

11.Disclaimer

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