

1.Description

This 20V N-Channel MOSFET uses Fairchild's high voltage PowerTrench process. It has been optimized for power management applications

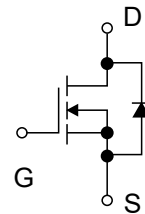
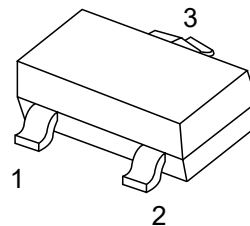
2.Features

- $V_{DS(V)}=20V$
- $R_{DS(ON)} < 125m\Omega (V_{GS}=4.5V)$
- $R_{DS(ON)} < 190m\Omega (V_{GS}=2.5V)$
- $R_{DS(ON)} < 80m\Omega (V_{GS}=1.8V)$

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	S	SOURCE
3	D	DRAIN

SOT-23



4.Maximum ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Value	Units
Drain-Source Voltage	V_{DSS}	20	V
Gate-Source Voltage	V_{GSS}	± 8	V
Drain Current – Continuous (Note 1a) – Pulsed	I_D	2	A
		8	
Maximum Power Dissipation (Note 1a) (Note 1b)	P_D	0.5	W
		0.46	
Storage Junction Temperature Range	T_J, T_{STG}	-55 to 150	$^{\circ}C$
Thermal Characteristics			
Thermal Resistance, Junction-to-Ambient (Note 1a)	$R_{\theta JA}$	250	$^{\circ}C/W$
Thermal Resistance, Junction-to-Case (Note 1)	$R_{\theta JC}$	75	$^{\circ}C/W$



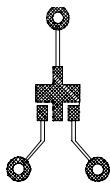
5.Static Electrical Characteristics ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =-250μA, V _{GS} =0V	20			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I _D =250μA Referenced to 25°C		12		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =16V, V _{GS} =0V			1	μA
Gate–Body Leakage, Forward	I _{GSSF}	V _{DS} =0V, V _{GS} =8V			100	nA
Gate–Body Leakage, Reverse	I _{GSSR}	V _{DS} =0V, V _{GS} =-8V			-100	nA
On Characteristics (Note 2)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.4	0.7	1.5	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I _D =250μA Referenced to 25°C		-3		mV/°C
Static Drain–Source On–Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D =2A		40	70	mΩ
		V _{GS} =2.5V, I _D =1.9A		49	80	
		V _{GS} =1.8V, I _D =1.6A		65	120	
On–State Drain Current	I _{D(ON)}	V _{GS} =4.5V, V _{DS} =5V	8			A
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =2A		11		S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =10V, V _{GS} =0V,f =1MHz		423		pF
Output Capacitance	C _{oss}			87		pF
Reverse Transfer Capacitance	C _{rss}			48		pF
SWITCHING PARAMETERS (Note 2)						
Turn-On DelayTime	t _{D(on)}	V _{DD} =10V, I _D =1A V _{GS} =4.5V, R _{GEN} =6Ω		6	12	ns
Turn-On Rise Time	t _r			6.5	16	ns
Turn-Off DelayTime	t _{D(off)}			14	29	ns
Turn-Off Fall Time	t _f			2	4	ns
Total Gate Charge	Q _g	V _{DS} =10V, I _D =2A V _{GS} =4.5V		4.5	6.3	nC
Gate–Source Charge	Q _{gs}			0.89		nC
Gate–Drain Charge	Q _{gd}			0.95		nC

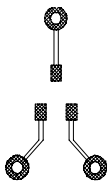


Drain–Source Diode Characteristics and Maximum Ratings						
Maximum Continuous Drain–Source Diode Forward Current	I_S				0.42	A
Drain–Source Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=0.42$ (Note 2)		-0.6	1.2	V

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 250°C/W when mounted on a 0.02 in² pad of 2 oz. copper.



b) 270°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%



6.1 Typical Characteristics

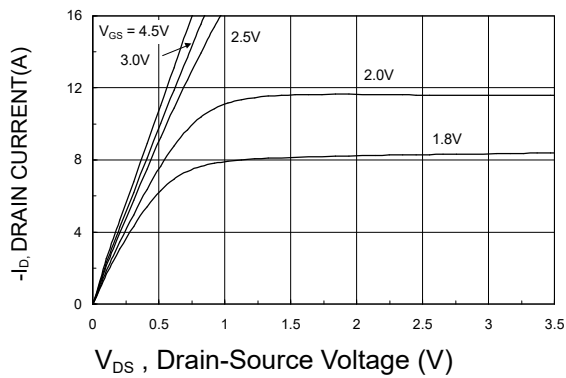


Figure 1: On-Region Characteristics.

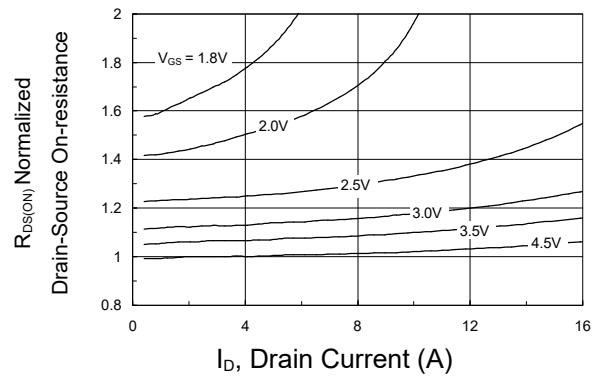


Figure 2: On-Resistance Variation with Drain Current and Gate Voltage.

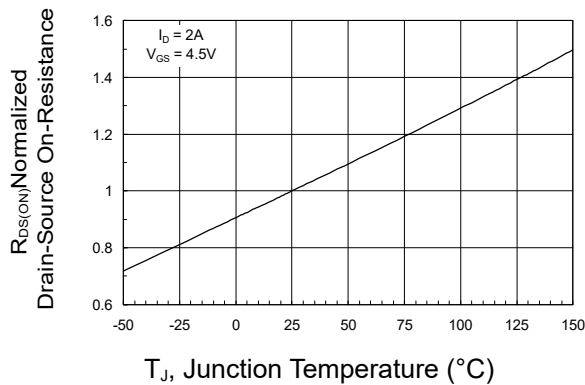


Figure 3: On-Resistance Variation with Temperature.

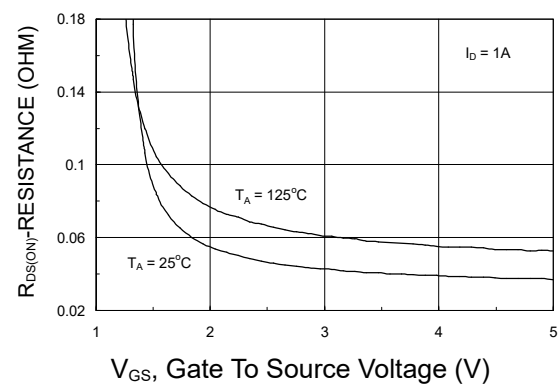


Figure 4: On-Resistance Variation with Gate-to-Source Voltage.

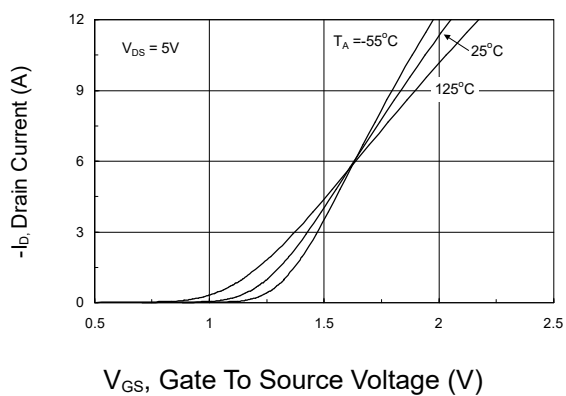


Figure 5: Transfer Characteristics.

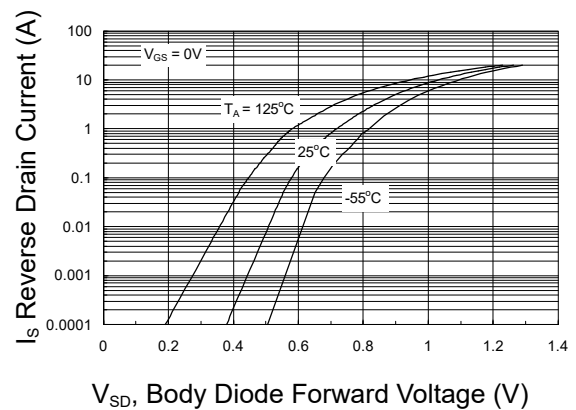


Figure 6: . Body Diode Forward Voltage Variation with Source Current and Temperature.



6.2 Typical Characteristics

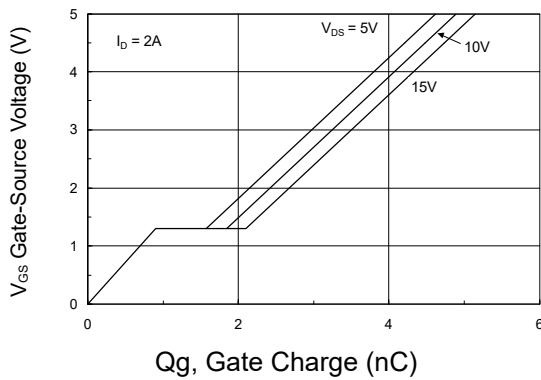


Figure 7: Gate-Charge Characteristics

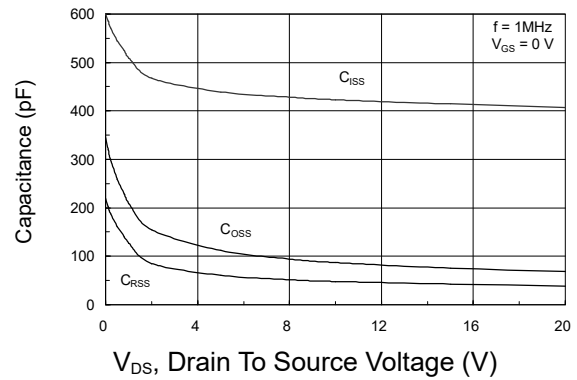


Figure 8: Capacitance Characteristics

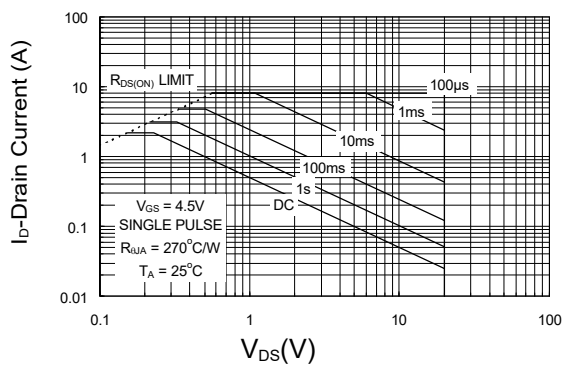


Figure 9: Maximum Safe Operating Area.

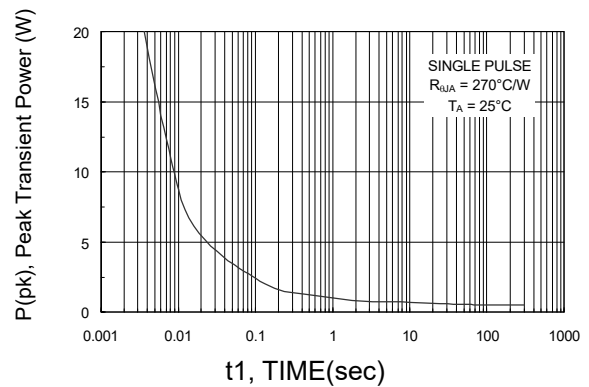


Figure 10: Single Pulse Maximum Power Dissipation.

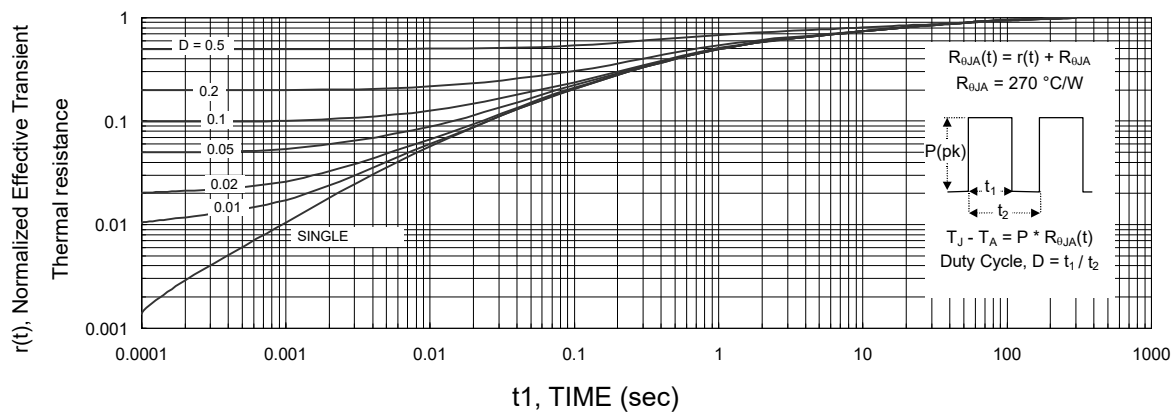
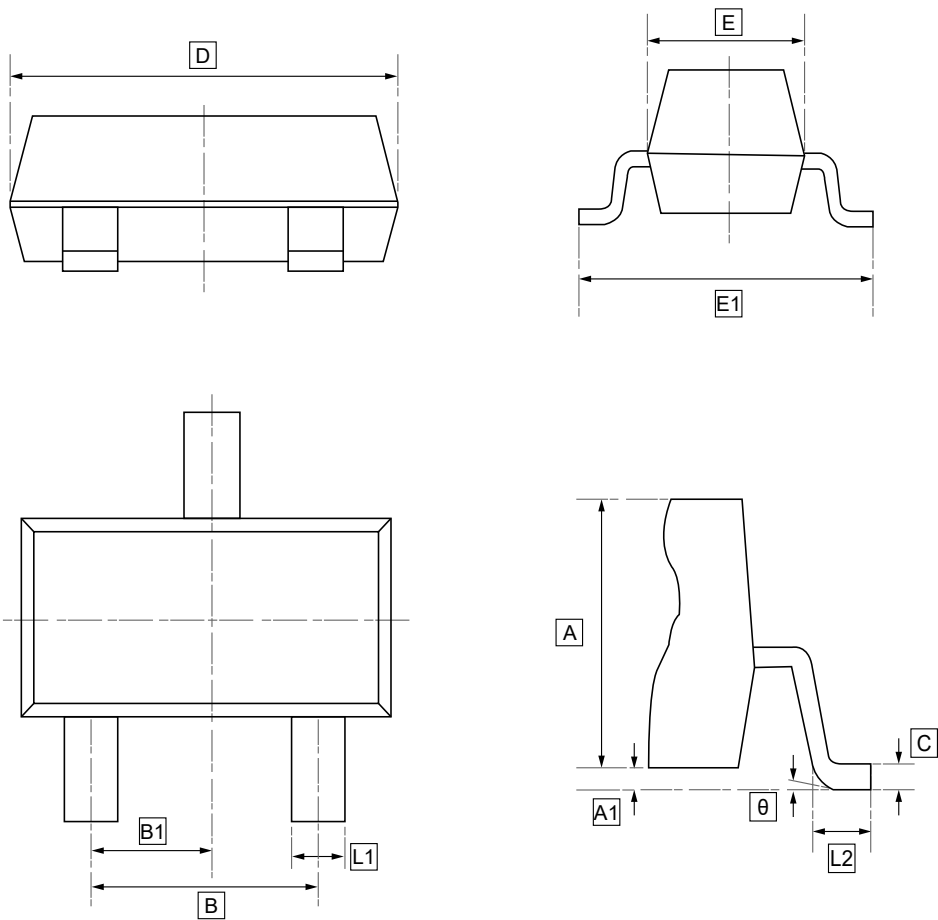


Figure 11. Transient Thermal Response Curve.



7.SOT-23 Package Outline Dimensions

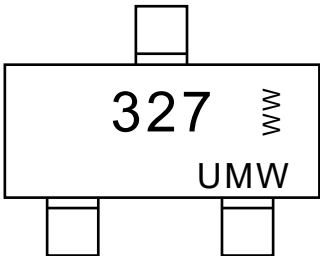


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	L1	L2	C	D	E	E1	B	B1	θ
Min	1.050	0.000	0.300	0.350	0.100	2.820	1.500	2.700	1.800	0.950	0°
Max	1.150	0.100	0.500	0.550	0.200	3.020	1.700	2.900	2.000	TYP	8°



8.Ordering information



WW: Batch Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDN327N	SOT-23	3000	Tape and reel



9.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

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