

1.Description

- Low $R_{DS(ON)}$
- Low Gate Charge
- Low Eoss
- E_{SD} protected
- RoHS and Halogen-Free Compliant

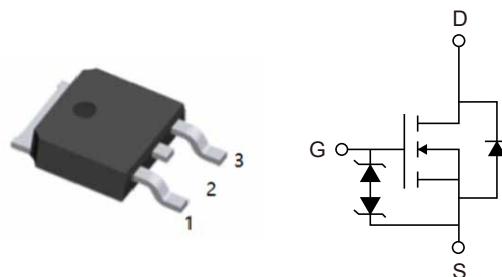
2.Features

- $V_{DS(V)}=60V$
- $I_D=46A(V_{GS}=10V)$
- $R_{DS(ON)}<9.5m\Omega(V_{GS}=10V)$
- $R_{DS(ON)}<13.3m\Omega(V_{GS}=4.5V)$

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view



4.Absolute Maximum Ratings $T_A = 25^\circ C$

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^G	$T_C=25^\circ C$	I_D	46	A
	$T_C=100^\circ C$		36.5	
Pulsed Drain Current ^C		I_{DM}	110	
Continuous Drain Current	$T_A=25^\circ C$	I_{DSM}	19	
	$T_A=70^\circ C$		15	
Avalanche Current ^C		I_{AS}	17	
Avalanche energy $L=0.3mH$ ^C		E_{AS}	43	
V_{DS} Spike ^I	10 μs	V_{SPIKE}	72	
Power Dissipation ^B	$T_C=25^\circ C$	P_D	59.5	W
	$T_C=100^\circ C$		23.5	



UMW AOD2610E

Power Dissipation ^A	$T_C=25^{\circ}\text{C}$	P_{DSM}	6.2	W
	$T_C=70^{\circ}\text{C}$		4	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^{\circ}\text{C}$

5.Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10\text{s}$	$R_{\theta\text{JA}}$	15	20	$^{\circ}\text{C/W}$
Maximum Junction-to-Ambient ^{AD}	Steady-State		40	50	$^{\circ}\text{C/W}$
Maximum Junction-to-Case	Steady-State	$R_{\theta\text{JC}}$	1.7	2.1	$^{\circ}\text{C/W}$



6. Electrical Characteristic ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	60			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60\text{V}$, $V_{GS}=0\text{V}$			1	μA
		$T_J=55^{\circ}\text{C}$			5	μA
Gate-Body leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			± 10	μA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.4	1.8	2.4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$, $I_D=20\text{A}$		7.7	9.5	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=20\text{A}$		10.3	13.3	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5\text{V}$, $I_D=20\text{A}$		52		S
Diode Forward Voltage	V_{SD}	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.72	1	V
Maximum Body-Diode Continuous Current ^G	I_S				46	A
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}$, $V_{DS}=30\text{V}$, $f=1\text{MHz}$		1100		pF
Output Capacitance	C_{oss}			300		pF
Reverse Transfer Capacitance	C_{rss}			28		pF
Gate resistance	R_g	$f=1\text{MHz}$	0.6	1.2	2	Ω
Total Gate Charge	$Q_g(10\text{V})$	$V_{GS}=10\text{V}$, $V_{DS}=30\text{V}$ $I_D=20\text{A}$		14.5	25	nC
Total Gate Charge	$Q_g(4.5\text{V})$			7	13	nC
Gate Source Charge	Q_{gs}			2.5		nC
Gate Drain Charge	Q_{gd}			3.5		nC
Turn-On DelayTime	$t_{D(on)}$	$V_{GS}=10\text{V}$, $V_{DS}=30\text{V}$ $R_L=1.5\Omega$, $R_{GEN}=3\Omega$		6.5		ns
Turn-On Rise Time	t_r			3.5		ns
Turn-Off DelayTime	$t_{D(off)}$			22		ns
Turn-Off Fall Time	t_f			3		ns
Body Diode Reverse Recovery Time	t_{rr}	$I_F=20\text{A}$, $dI/dt=500\text{A}/\mu\text{s}$		19		ns
Body Diode Reverse Recovery Charge	Q_{rr}	$I_F=20\text{A}$, $dI/dt=500\text{A}/\mu\text{s}$		65		nC



- A. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA} \leq 10\text{s}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.
- B. The power dissipation P_D is based on $T_{J(MAX)} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Single pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$.
- D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)} = 150^\circ\text{C}$. The SOA curve provides a single pulse rating.
- G. The maximum current rating is package limited.
- H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$.
- I. The spike duty cycle 5% max, limited by junction temperature $T_{J(MAX)} = 125^\circ\text{C}$.



7.1 Typical characteristic

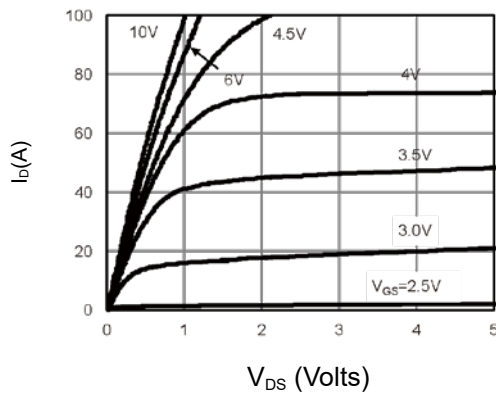


Figure 1: On-Region Characteristics (Note E)

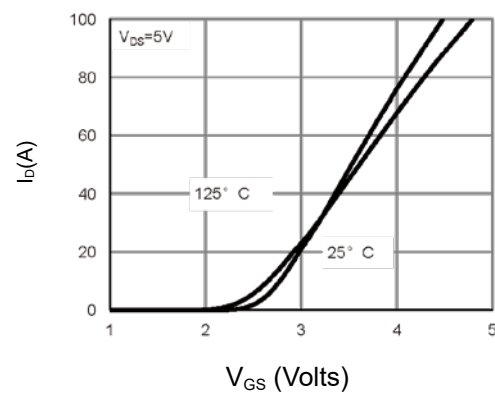


Figure 2: Transfer Characteristics (Note E)

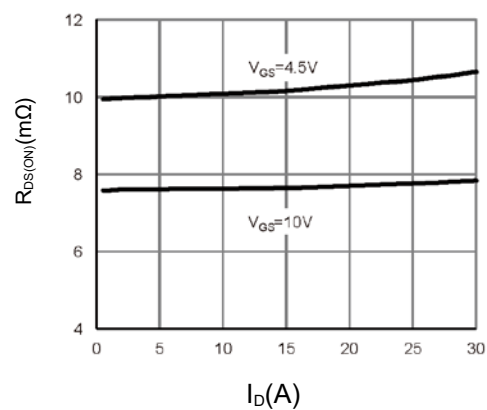


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

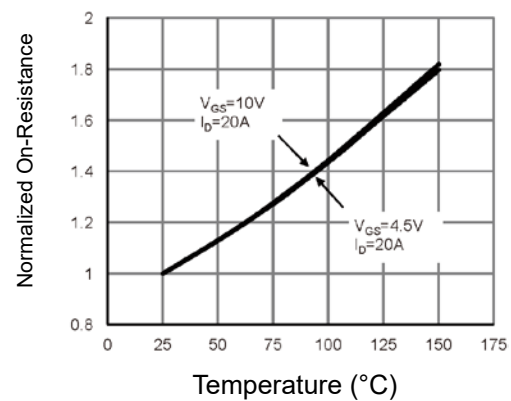


Figure 4: On-Resistance vs. Junction Temperature (Note E)

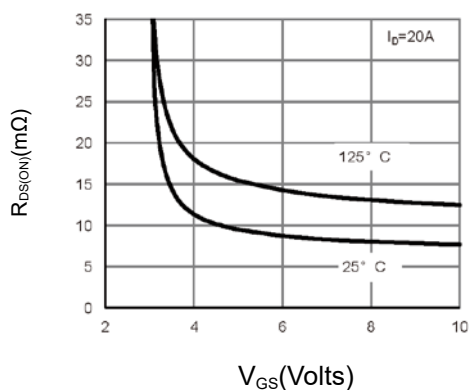


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

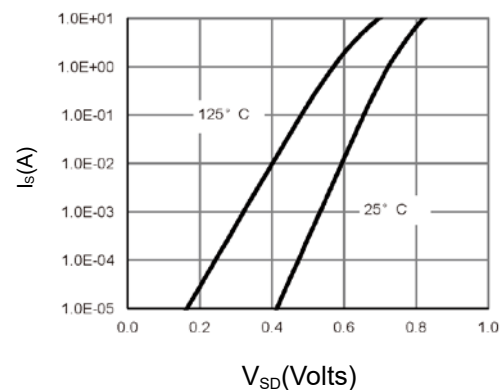


Figure 6: Body-Diode Characteristics (Note E)



7.2 Typical characteristic

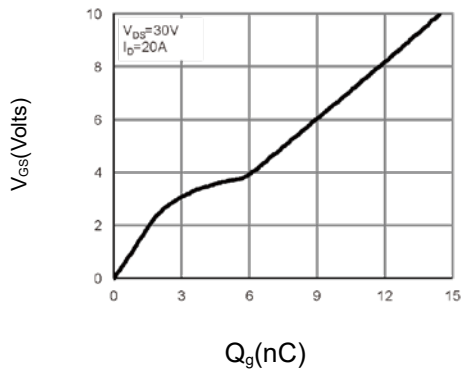


Figure 7: Gate-Charge Characteristics

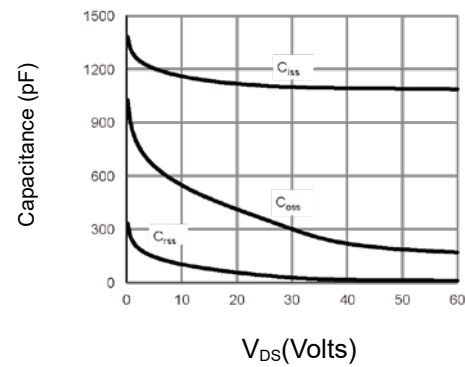


Figure 8: Capacitance Characteristics

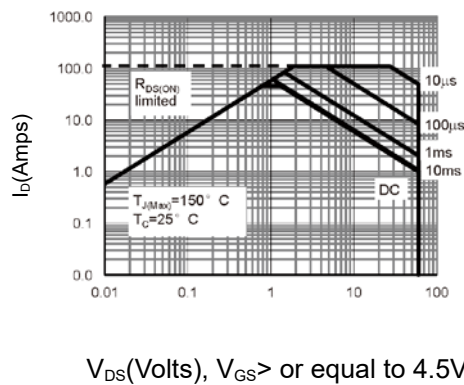


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

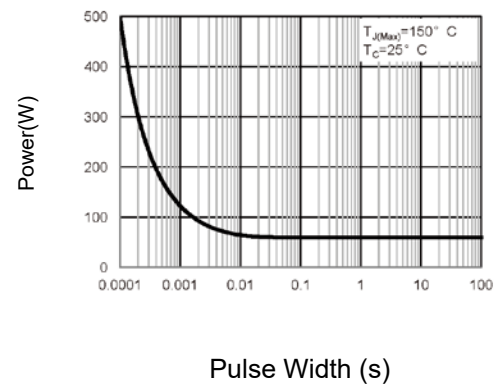


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

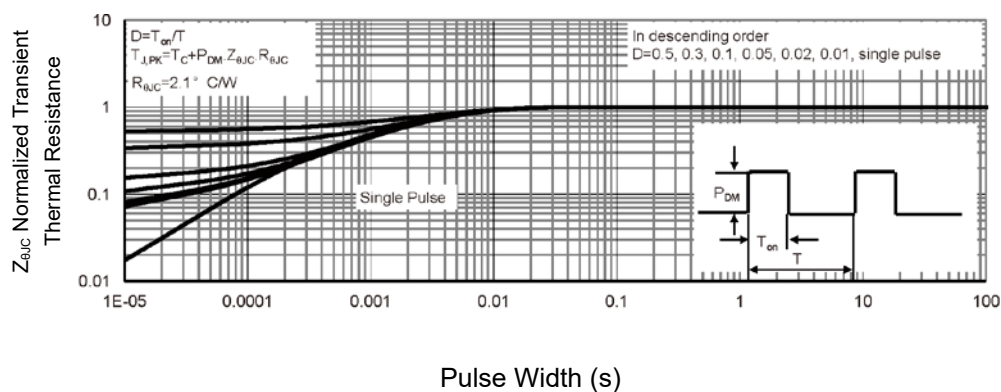


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



7.3 Typical characteristic

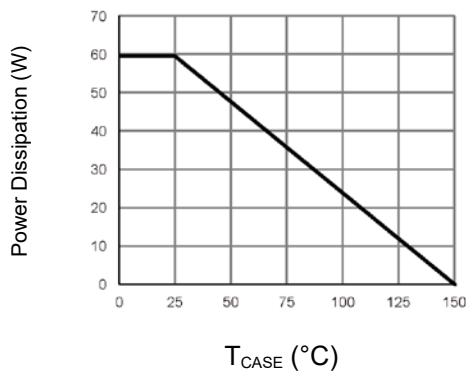


Figure 12: Power De-rating (Note F)

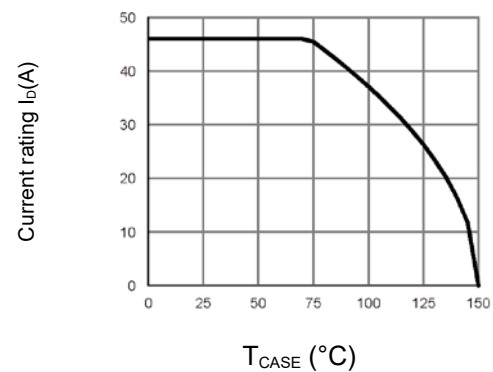


Figure 13: Current De-rating (Note F)

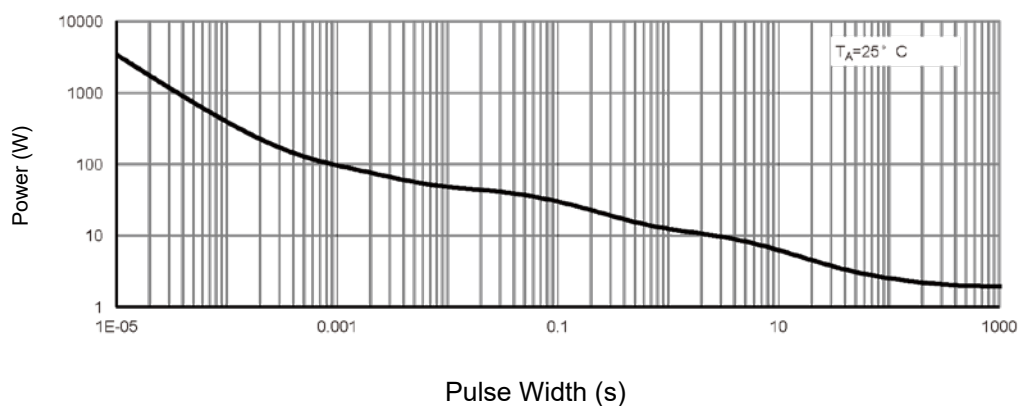


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

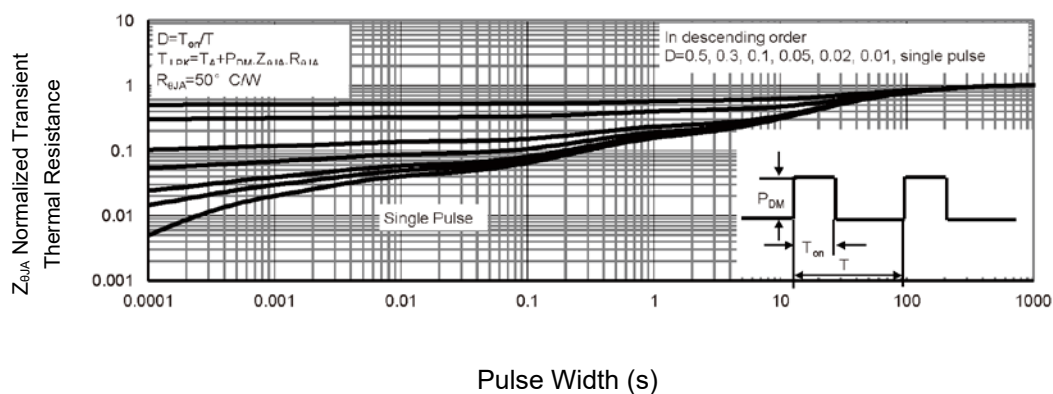


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)



7.4 Typical characteristic

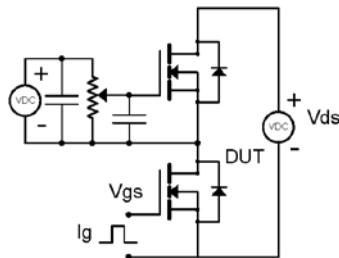


Figure A: Gate Charge Test Circuit & Waveforms

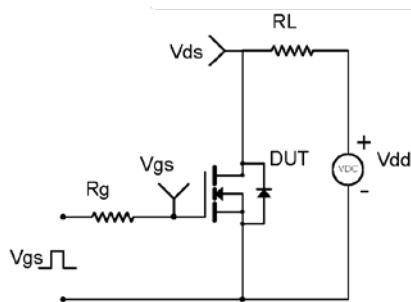


Figure B: Resistive Switching Test Circuit & Waveforms

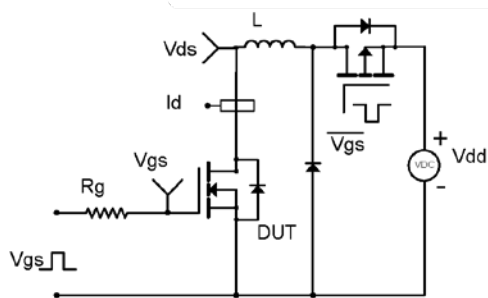


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

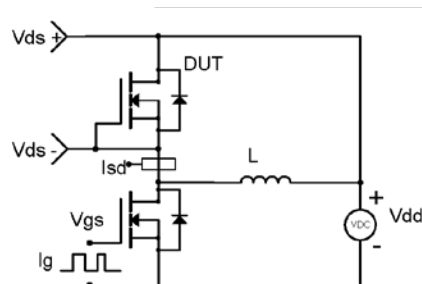
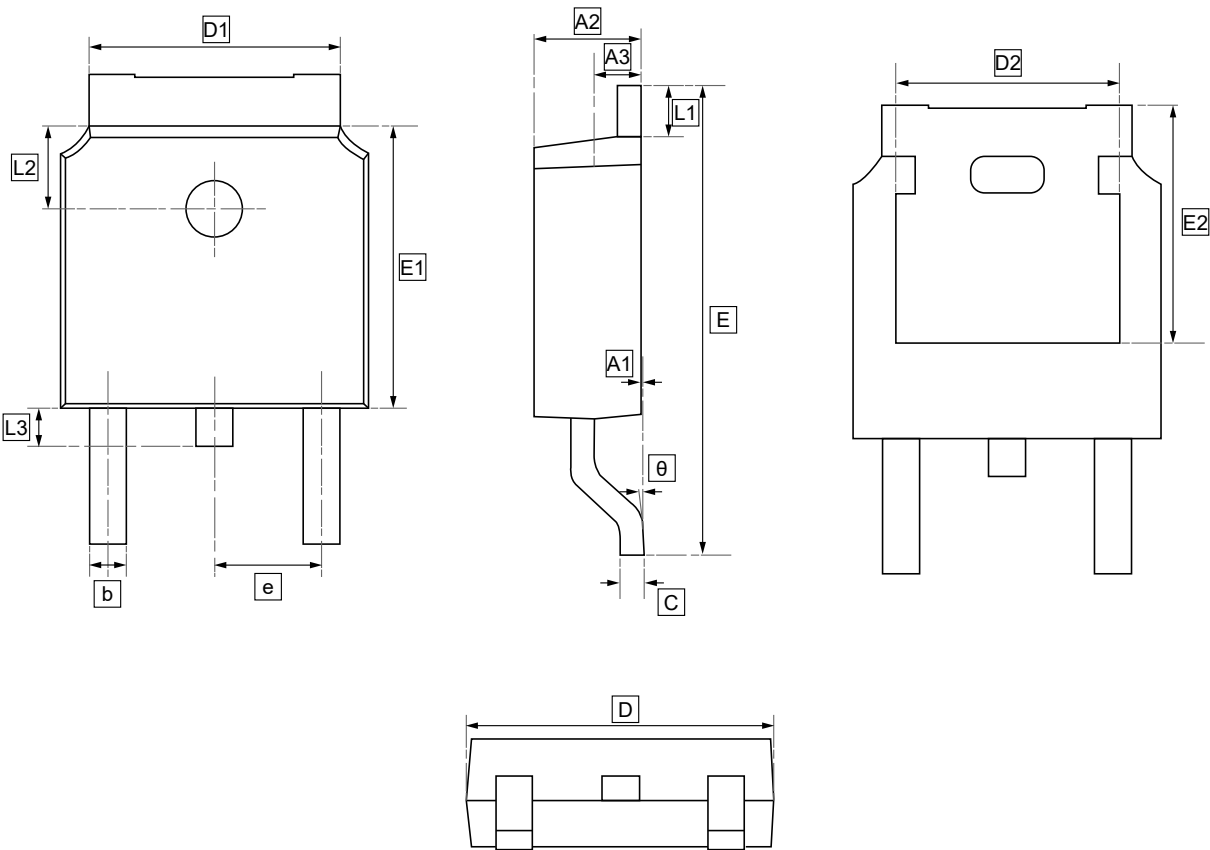


Figure D: Diode Recovery Test Circuit & Waveforms



8.TO-252 Package Outline Dimensions

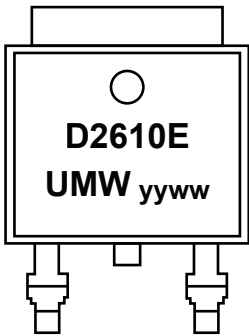


DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38		BSC	1.27	1.90	1.00



9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW AOD2610E	TO-252	2500	Tape and reel



10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

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