RoHS HAL PB Green

Serially Inte rface d, 8 -Digi t LED Displ ay Drivers

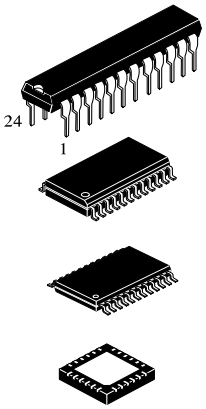
The HT7219A/HT7221A are compact, serial input/out-put common-cathode display drivers that interface microprocessors (µPs) to 7-segment numeric LED dis-plays of up to 8 digits, bar-graph displays, or 64 indi-vidual LEDs. Included on-chip are a BCD code-B decoder, multiplex scan circuitry, segment and digit drivers, and an 8x8 static RAM that stores each digit. Only one external resistor is required to set the seg-ment current for all LEDs. The HT7221A is compatible with SPI™, QSPI™, and Microwire™, and has slew-rate-limited segment drivers to reduce EMI.A convenient 3-wire serial interface connects to all common µPs. Individual digits may be addressed and updated without rewriting the entire display. The HT7219A/HT7221A also allow the user to select code-B decoding or no-decode for each digit.The devices include a 150µA low-power shutdown mode, analog and digital brightness control, a scan- limit register that allows the user to display from 1 to 8 digits, and a test mode that forces all LEDs on.

Feat ures

- **10MHz Serial Interface**
- **Individual LED Segment Control**
- **Decode/No-Decode Digit Selection**
- **150µA Low-Power Shutdown (Data Retained)**
- **Digital and Analog Brightness Control**
- **Display Blanked on Power-Up**
- **Drive Common-Cathode LED Display**
- **Slew-Rate Limited Segment Drivers for Lower EMI (HT7221A)**
- **SPI, QSPI, Microwire Serial Interface (HT7221A)**
- **24-Pin DIP and SO Packages**

Appli cat ions

Bar-Graph Displays
7-Segment Displays
Industrial Controllers
Panel Meters
LED Matrix Displays



DIP24
N SUFFIX

WSOP24
W SUFFIX

TSSOP24
T SUFFIX

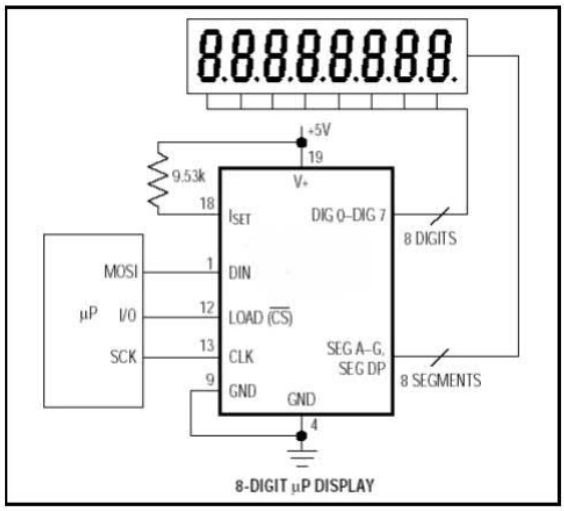
QFN24
Q SUFFIX

ORDERING INFORMATION

HT72xxANZ	DIP24
HT72xxARWZ	WSOP24
HT72xxARTZ	TSSOP24
HT72xxARQZ	QFN24

T_A = -45° to 125° C for all packages

TYPICAL APPLICATION CIRCUIT



8-DIGIT µP DISPLAY

ABSOLUTE HTCSEMIUM RATINGS

Voltage (with respect to GND)
- V+ .....-0.3V to 6V
- DIN, CLK, LOAD, CS .....-0.3V to 6V
- All Other Pins.....-0.3V to (V+ + 0.3V)

Current
- DIG0–DIG7 Sink Current.....500mA
- SEGA–G, DP Source Current.....100mA

Continuous Power Dissipation (T_A = +85°C)
- Narrow Plastic DIP 0.87W
- Wide SO 0.76W
- Narrow CERDIP.....1.1W

ELECTRICAL CHARACTERISTICS

(V+ = 5V ±10%, R_{SET} = 9.53kΩ ±1%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+		4.0		5.5	V
Shutdown Supply Current	I+	All digital inputs at V+ or GND, T_A = +25°C			150	µA
Operating Supply Current	I+	R_{SET} = open circuit			8	mA
		All segments and decimal point on, $I_{SEG\_}$ = -40mA		330		
Display Scan Rate	f_{OSC}	8 digits scanned	500	800	1300	Hz
Digit Drive Sink Current	I_{DIGIT}	V+ = 5V, V_{OUT} = 0.65V	320			mA
Segment Drive Source Current	I_{SEG}	T_A = +25°C, V+ = 5V, V_{OUT} = (V+ - 1V)	-30	-40	-45	mA
Segment Current Slew Rate (HT7221A only)	$\Delta I_{SEG}/\Delta t$	T_A = +25°C, V+ = 5V, V_{OUT} = (V+ - 1V)	10	20	50	mA/µs
Segment Drive Current Matching	ΔI_{SEG}			3.0		%
Digit Drive Leakage (HT7221A only)	I_{DIGIT}	Digit off, V_{DIGIT} = V+			-10	µA
Segment Drive Leakage (HT7221A only)	I_{SEG}	Segment off, V_{SEG} = 0V			1	µA
Digit Drive Source Current (HT7219A only)	I_{DIGIT}	Digit off, V_{DIGIT} = (V+ - 0.3V)	-2			mA
Segment Drive Sink Current (HT7219A only)	I_{SEG}	Segment off, V_{SEG} = 0.3V	5			mA

ELECTRICAL CHARACTERISTICS (continued)

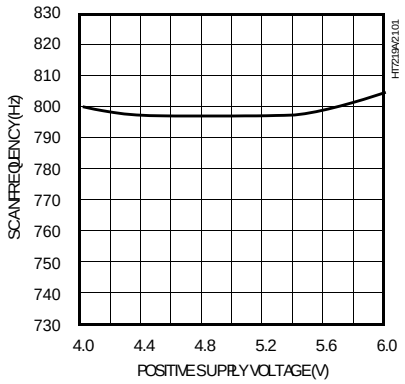
(V+ = 5V ±10%, R_{SET} =9.53kΩ ±1%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Input Current DIN, CLK, LOAD, CS	I_{IH}, I_{IL}	V_{IN} = 0V or V+	-1		1	µA
Logic High Input Voltage	V_{IH}		3.5			V
Logic Low Input Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	DOUT, I_{SOURCE} = -1mA	V+ - 1			V
Output Low Voltage	V_{OL}	DOUT, I_{SINK} = 1.6mA			0.4	V
Hysteresis Voltage	ΔV_I	DIN, CLK, LOAD, CS		1		V
TIMING CHARACTERISTICS						
CLK Clock Period	t_{CP}		100			ns
CLK Pulse Width High	t_{CH}		50			ns
CLK Pulse Width Low	t_{CL}		50			ns
CS Fall to SCLK Rise Setup Time (HT7221A only)	t_{CSS}		25			ns
CLK Rise to CS or LOAD Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		25			ns
DIN Hold Time	t_{DH}		0			ns
Output Data Propagation Delay	t_{DO}	C_{LOAD} = 50pF			25	ns
Load-Rising Edge to Next Clock Rising Edge (HT7219A only)	t_{LDCK}		50			ns
Minimum CS or LOAD Pulse High	t_{CSW}		50			ns
Data-to-Segment Delay	t_{DSPD}				2.25	ms

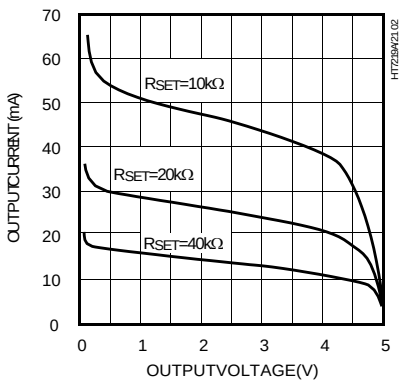
Typical Operating Characteristics

(V+ = +5V, T_A = +25°C, unless otherwise noted.)

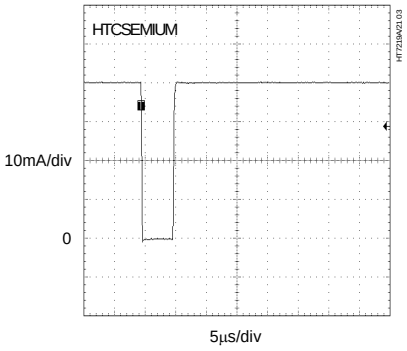
SCAN FREQUENCY vs. POSITIVE SUPPLY VOLTAGE



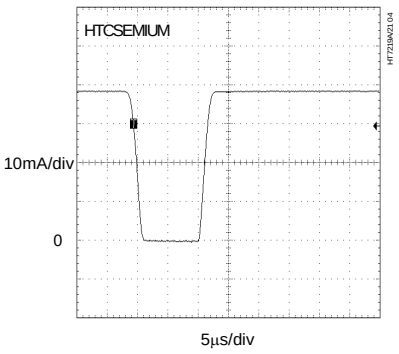
SEGMENT DRIVER OUTPUT CURRENT vs. OUTPUT VOLTAGE



HT7219A SEGMENT OUTPUT CURRENT



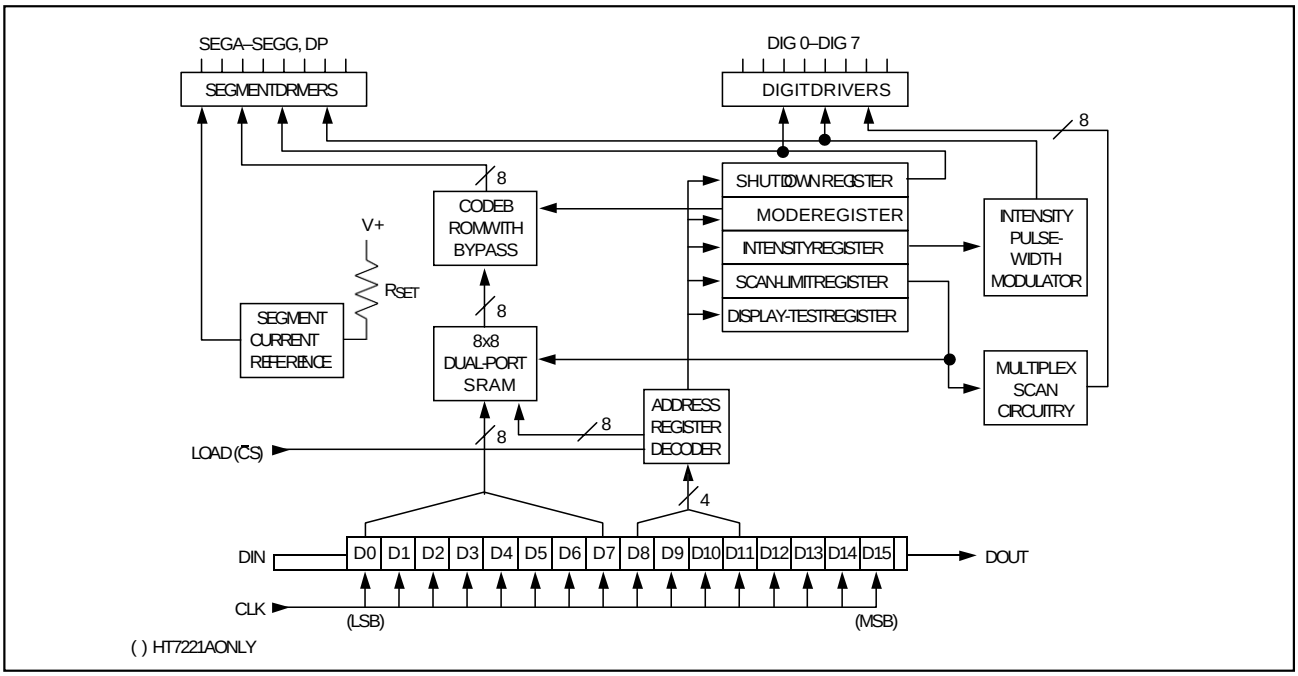
HT7221A SEGMENT OUTPUT CURRENT



Pin Description

PIN	NAME	FUNCTION
1	DIN	Serial-Data Input. Data is loaded into the internal 16-bit shift register on CLK's rising edge.
2, 3, 5–8, 10, 11	DIG 0–DIG 7	Eight-Digit Drive Lines that sink current from the display common cathode. The HT7219A pulls the digit outputs to V+ when turned off. The HT7221A's digit drivers are high-impedance when turned off.
4, 9	GND	Ground (both GND pins must be connected)
12	LOAD (HT7219A)	Load-Data Input. The last 16 bits of serial data are latched on LOAD's rising edge.
	CS (HT7221A)	Chip-Select Input. Serial data is loaded into the shift register while CS is low. The last 16 bits of serial data are latched on CS's rising edge.
13	CLK	Serial-Clock Input. 10MHz HTCSEMIum rate. On CLK's rising edge, data is shifted into the inter- nal shift register. On CLK's falling edge, data is clocked out of DOUT. On the HT7221A, the CLK input is active only while CS is low.
14–17, 20–23	SEG A–SEG G, DP	Seven Segment Drives and Decimal Point Drive that source current to the display. On the HT7219A, when a segment driver is turned off it is pulled to GND. The HT7221A segment dri- vers are high-impedance when turned off.
18	ISET	Connect to V_{DD} through a resistor (R_{SET}) to set the peak segment current (Refer to *Selecting R_{SET} Resistor* section).
19	V+	Positive Supply Voltage. Connect to +5V.
24	DOUT	Serial-Data Output. The data into DIN is valid at DOUT 16.5 clock cycles later. This pin is used to daisy-chain several HT7219A/HT7221A's and is never high-impedance.

Functional Diagram



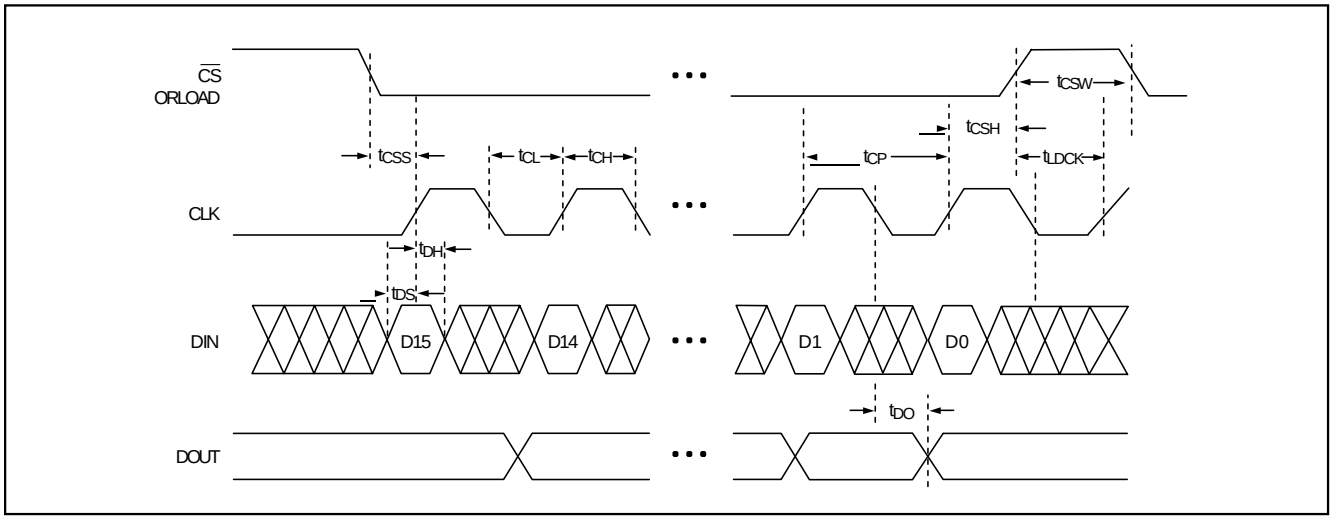


Figure 1. Timing Diagram

Table 1. Serial-Data Format (16 Bits)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	ADDRESS				MSB	DATA						LSB

Deta iled Description

HT7219A /HT7221A Diff erences The HT7219A and HT7221A are identical except for two parameters: the HT7221A segment drivers are slew-rate limited to reduce electromagnetic interfer- ence (EMI), and its serial interface is fully SPI compati- ble.

Serial-Addr essing Modes

For the HT7219A, serial data at DIN, sent in 16-bit packets, is shifted into the internal 16-bit shift register with each rising edge of CLK regardless of the state of LOAD. For the HT7221A, CS must be low to clock data in or out. The data is then latched into either the digit or control registers on the rising edge of LOAD/CS. LOAD/CS must go high concurrently with or after the 16th rising clock edge, but before the next rising clock edge or data will be lost. Data at DIN is propagated through the shift register and appears at DOUT 16.5 clock cycles later. Data is clocked out on the falling edge of CLK. Data bits are labeled D0–D15 (Table 1). D8–D11 contain the register address. D0–D7 contain the data, and D12–D15 are “don’t care” bits. The first received is D15, the most significant bit (MSB).

Digi t and Control Registers

Table 2 lists the 14 addressable digit and control registers. The digit registers are realized with an on-chip, 8x8 dual-port SRAM. They are addressed directly so that individual digits can be updated and retain data as long as V+ typically exceeds 2V. The control registers consist of decode mode, display intensity, scan limit (number of scanned digits), shutdown, and display test (all LEDs on).

Shutdown Mode

When the HT7219A is in shutdown mode, the scan oscillator is halted, all segment current sources are pulled to ground, and all digit drivers are pulled to V+, thereby blanking the display. The HT7221A is identical, except the drivers are high-impedance. Data in the digit and control registers remains unaltered. Shutdown can be used to save power or as an alarm to flash the display by successively entering and leaving shutdown mode. For minimum supply current in shutdown mode, logic inputs should be at ground or V+ (CMOS-logic levels).

Typically, it takes less than 250µs for the HT7219A/ HT7221A to leave shutdown mode. The display driver can be programmed while in shutdown mode, and shutdown mode can be overridden by the display-test function.

Table 2. Register Address Map

REGISTER	ADDRESS					HEX CODE
	D15–D12	D11	D10	D9	D8	
No-Op	X	0	0	0	0	X0
Digit 0	X	0	0	0	1	X1
Digit 1	X	0	0	1	0	X2
Digit 2	X	0	0	1	1	X3
Digit 3	X	0	1	0	0	X4
Digit 4	X	0	1	0	1	X5
Digit 5	X	0	1	1	0	X6
Digit 6	X	0	1	1	1	X7
Digit 7	X	1	0	0	0	X8
Decode Mode	X	1	0	0	1	X9
Intensity	X	1	0	1	0	XA
Scan Limit	X	1	0	1	1	XB
Shutdown	X	1	1	0	0	XC
Display Test	X	1	1	1	1	XF

Initial Power-Up

On initial power-up, all control registers are reset, the display is blanked, and the HT7219A/HT7221A enter shutdown mode. Program the display driver prior to display use. Otherwise, it will initially be set to scan one digit, it will not decode data in the data registers, and the intensity register will be set to its minimum value.

Decode-Mode Register

The decode-mode register sets BCD code B (0-9, E, H, L, P, and -) or no-decode operation for each digit. Each bit in the register corresponds to one digit. A logic high selects code B decoding while logic low bypasses the decoder. Examples of the decode mode control-register format are shown in Table 4.

When the code B decode mode is used, the decoder looks only at the lower nibble of the data in the digit registers (D3–D0), disregarding bits D4–D6. D7, which sets the decimal point (SEG DP), is independent of the decoder and is positive logic (D7 = 1 turns the decimal point on). Table 5 lists the code B font.

When no-decode is selected, data bits D7–D0 correspond to the segment lines of the HT7219A/HT7221A. Table 6 shows the one-to-one pairing of each data bit to the appropriate segment line.

Table 3. Shutdown Register Format (Address (Hex) = XC)

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Shutdown Mode	XC	X	X	X	X	X	X	X	0
Normal Operation	XC	X	X	X	X	X	X	X	1

Table 4. Decode-Mode Register Examples (Address (Hex) = X9)

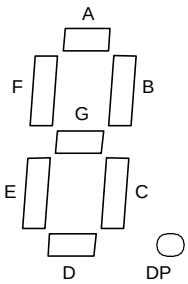
DECODE MODE	REGISTER DATA								HEX CODE
	D7	D6	D5	D4	D3	D2	D1	D0	
No decode for digits 7–0	0	0	0	0	0	0	0	0	00
Code B decode for digit 0 No decode for digits 7–1	0	0	0	0	0	0	0	1	01
Code B decode for digits 3–0 No decode for digits 7–4	0	0	0	0	1	1	1	1	0F
Code B decode for digits 7–0	1	1	1	1	1	1	1	1	FF

Table 5. Code B Font

7-SEGMENT CHARACTER	REGISTER DATA						ON SEGMENTS = 1							
	D7*	D6–D4	D3	D2	D1	D0	DP*	A	B	C	D	E	F	G
0		X	0	0	0	0		1	1	1	1	1	1	0
1		X	0	0	0	1		0	1	1	0	0	0	0
2		X	0	0	1	0		1	1	0	1	1	0	1
3		X	0	0	1	1		1	1	1	1	0	0	1
4		X	0	1	0	0		0	1	1	0	0	1	1
5		X	0	1	0	1		1	0	1	1	0	1	1
6		X	0	1	1	0		1	0	1	1	1	1	1
7		X	0	1	1	1		1	1	1	0	0	0	0
8		X	1	0	0	0		1	1	1	1	1	1	1
9		X	1	0	0	1		1	1	1	1	0	1	1
—		X	1	0	1	0		0	0	0	0	0	0	1
E		X	1	0	1	1		1	0	0	1	1	1	1
H		X	1	1	0	0		0	1	1	0	1	1	1
L		X	1	1	0	1		0	0	0	1	1	1	0
P		X	1	1	1	0		1	1	0	0	1	1	1
blank		X	1	1	1	1		0	0	0	0	0	0	0

*The decimal point is set by bit D7 = 1

Table 6. No-Decode Mode Data Bits and Corresponding SegmentLines



STANDARD 7-SEGMENT LED

	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Corresponding Segment Line	DP	A	B	C	D	E	F	G

Intensity Control and Interdigi t Blanking

The HT7219A/HT7221A allow display brightness to be controlled with an external resistor (R_{SET}) connected between V+ and ISET. The peak current sourced from the segment drivers is nominally 100 times the current entering ISET. This resistor can either be fixed or variable to allow brightness adjustment from the front panel. Its minimum value should be 9.53Ω, which typi- cally sets the segment current at 40mA. Display bright- ness can also be controlled digitally by using the intensity register.

Digital control of display brightness is provided by an internal pulse-width modulator, which is controlled by the lower nibble of the intensity register. The modulator scales the average segment current in 16 steps from a HTCSEMIum of 31/32 down to 1/32 of the peak current set by R_{SET} (15/16 to 1/16 on HT7221A). Table 7 lists the intensity register format. The minimum interdigit blank- ing time is set to 1/32 of a cycle.

Table 7. Intensity Register Format (Address (Hex) = XA)

DUTY CYCLE		D7	D6	D5	D4	D3	D2	D1	D0	HEX CODE
HT7219A	HT7221A									
1/32 (min on)	1/16 (min on)	X	X	X	X	0	0	0	0	X0
3/32	2/16	X	X	X	X	0	0	0	1	X1
5/32	3/16	X	X	X	X	0	0	1	0	X2
7/32	4/16	X	X	X	X	0	0	1	1	X3
9/32	5/16	X	X	X	X	0	1	0	0	X4
11/32	6/16	X	X	X	X	0	1	0	1	X5
13/32	7/16	X	X	X	X	0	1	1	0	X6
15/32	8/16	X	X	X	X	0	1	1	1	X7
17/32	9/16	X	X	X	X	1	0	0	0	X8
19/32	10/16	X	X	X	X	1	0	0	1	X9
21/32	11/16	X	X	X	X	1	0	1	0	XA
23/32	12/16	X	X	X	X	1	0	1	1	XB
25/32	13/16	X	X	X	X	1	1	0	0	XC
27/32	14/16	X	X	X	X	1	1	0	1	XD
29/32	15/16	X	X	X	X	1	1	1	0	XE
31/32	15/16 (max on)	X	X	X	X	1	1	1	1	XF

Table 8. Scan-Limit Register Format (Address (Hex) = XB)

SCAN LIMIT	REGISTER DATA								HEX CODE
	D7	D6	D5	D4	D3	D2	D1	D0	
Display digit 0 only*	X	X	X	X	X	0	0	0	X0
Display digits 0 & 1*	X	X	X	X	X	0	0	1	X1
Display digits 0 1 2*	X	X	X	X	X	0	1	0	X2
Display digits 0 1 2 3	X	X	X	X	X	0	1	1	X3
Display digits 0 1 2 3 4	X	X	X	X	X	1	0	0	X4
Display digits 0 1 2 3 4 5	X	X	X	X	X	1	0	1	X5
Display digits 0 1 2 3 4 5 6	X	X	X	X	X	1	1	0	X6
Display digits 0 1 2 3 4 5 6 7	X	X	X	X	X	1	1	1	X7

*See *Scan-Limit Register* section for application.

Scan-Limit Register

The scan-limit register sets how many digits are displayed, from 1 to 8. They are displayed in a multiplexed manner with a typical display scan rate of 800Hz with 8 digits displayed. If fewer digits are displayed, the scan rate is $8f_{OSC}/N$, where N is the number of digits scanned. Since the number of scanned digits affects the display brightness, the scan-limit register should not be used to blank portions of the display (such as leading zero suppression). Table 8 lists the scan-limit register format.

If the scan-limit register is set for three digits or less, individual digit drivers will dissipate excessive amounts of power. Consequently, the value of the RSET resistor must be adjusted according to the number of digits displayed, to limit individual digit driver power dissipation. Table 9 lists the number of digits displayed and the corresponding HTCSEMIum recommended segment cur- rent when the digit drivers are used.

Displ ay-Test Register

The display-test register operates in two modes: normal and display test. Display-test mode turns all LEDs on by overriding, but not altering, all controls and digit registers (including the shutdown register). In display-test mode, 8 digits are scanned and the duty cycle is 31/32 (15/16 for HT7221A). Table 10 lists the display-test register format.

Table 9. HTCSEMIum Segment Current for 1-, 2-, or 3-Digit Displays

NUMBER OF DIGITS DISPLAYED	HTCSEMIUM SEGMENT CURRENT (mA)
1	10
2	20
3	30

Table 10. Display-Test Register Format (Address (Hex) = XF)

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Normal Operation	X	X	X	X	X	X	X	0
Display Test Mode	X	X	X	X	X	X	X	1

Note: The HT7219A/HT7221A remain in display-test mode (all LEDs on) until the display-test register is reconfigured for normal operation.

No-Op Register

The no-op register is used when cascading HT7219As or HT7221As. Connect all devices' LOAD/CS inputs together and connect DOUT to DIN on adjacent devices. DOUT is a CMOS logic-level output that easily drives DIN of successively cascaded parts. (Refer to the *Serial Addressing Modes* section for detailed information on serial input/output timing.) For example, if four HT7219As are cascaded, then to write to the fourth chip, sent the desired 16-bit word, followed by three no-op codes (hex XX0X, see Table 2). When LOAD/CS goes high, data is latched in all devices. The first three chips receive no-op commands, and the fourth receives the intended data.

Appli cat ions Infor mat ion

Supply Bypassing and Wiring To minimize power-supply ripple due to the peak digit driver currents, connect a 10µF electrolytic and a 0.1µF ceramic capacitor between V+ and GND as close to the device as possible. The HT7219A/HT7221A should be placed in close proximity to the LED display, and connections should be kept as short as possible to minimize the effects of wiring inductance and electromagnetic interference. Also, both GND pins must be connected to ground.

Select ing RSET Resistor and Using Exte rnal Driv ers

The current per segment is approximately 100 times the current in ISET. To select RSET, see Table 11. The HT7219A/HT7221A's HTCSEMIum recommended segment current is 40mA. For segment current levels above these levels, external digit drivers will be need- ed. In this application, the HT7219A/HT7221A serve only as controllers for other high-current drivers or tran- sistors. Therefore, to conserve power, use RSET = 47kΩ when using external current sources as segment dri- vers.

The example in Figure 2 uses the HT7219A/HT7221A's segment drivers, a MAX394 single-pole double-throw analog switch, and external transistors to drive 2.3" AND2307SLC common-cathode displays. The 5.6V zener diode has been added in series with the decimal point LED because the decimal point LED forward voltage is typically 4.2V. For all other segments the LED forward voltage is typically 8V. Since external transistors are used to sink current (DIG 0 and DIG 1 are used as logic switches), peak segment currents of 45mA are allowed even though only two digits are displayed. In applications where the HT7219A/HT7221A's digit drivers are used to sink current and fewer than four digits are displayed, Table 9 specifies the HTCSEMIum allowable segment current. RSET must be selected accordingly (Table 11).

Refer to the Power Dissipation section of the Absolute HTCSEMIum Ratings to calculate acceptable limits for ambient temperature, segment current, and the LED forward-voltage drop.

Table 11. R_{SET} vs. Segment Current and LED Forward Voltage

I_{SEG} (mA)	V_{LED} (V)				
	1.5	2.0	2.5	3.0	3.5
40	12.2	11.8	11.0	10.6	9.69
30	17.8	17.1	15.8	15.0	14.0
20	29.8	28.0	25.9	24.5	22.6
10	66.7	63.7	59.3	55.4	51.2

Table 12. Package Thermal Resistance Data

PACKAGE	THERMAL RESISTANCE (θ_{JA})
24 Narrow DIP	+75°C/W
24 Wide SO	+85°C/W
24 CERDIP	+60°C/W
HTCSEMIum Junction Temperature (T_J) = +150°C	
HTCSEMIum Ambient Temperature (T_A) = +85°C	

Computing Power Dissip ation

The upper limit for power dissipation (PD) for the HT7219A/HT7221A is determined from the following equation:

$$PD = (V + \times 8mA) + (V+ - V_{LED})(DUTY \times I_{SEG} \times N)$$

where:

V+ = supply voltage

DUTY = duty cycle set by intensity register

N = number of segments driven (worst case is 8)

V_{LED} = LED forward voltage

I_{SEG} = segment current set by R_{SET}

Dissipation Example:

I_{SEG} = 40mA, N = 8, DUTY = 31/32, V_{LED} = 1.8V at 40mA, V+ = 5.25V

PD = 5.25V(8mA) + (5.25V - 1.8V)(31/32 x 40mA x 8) = 1.11W

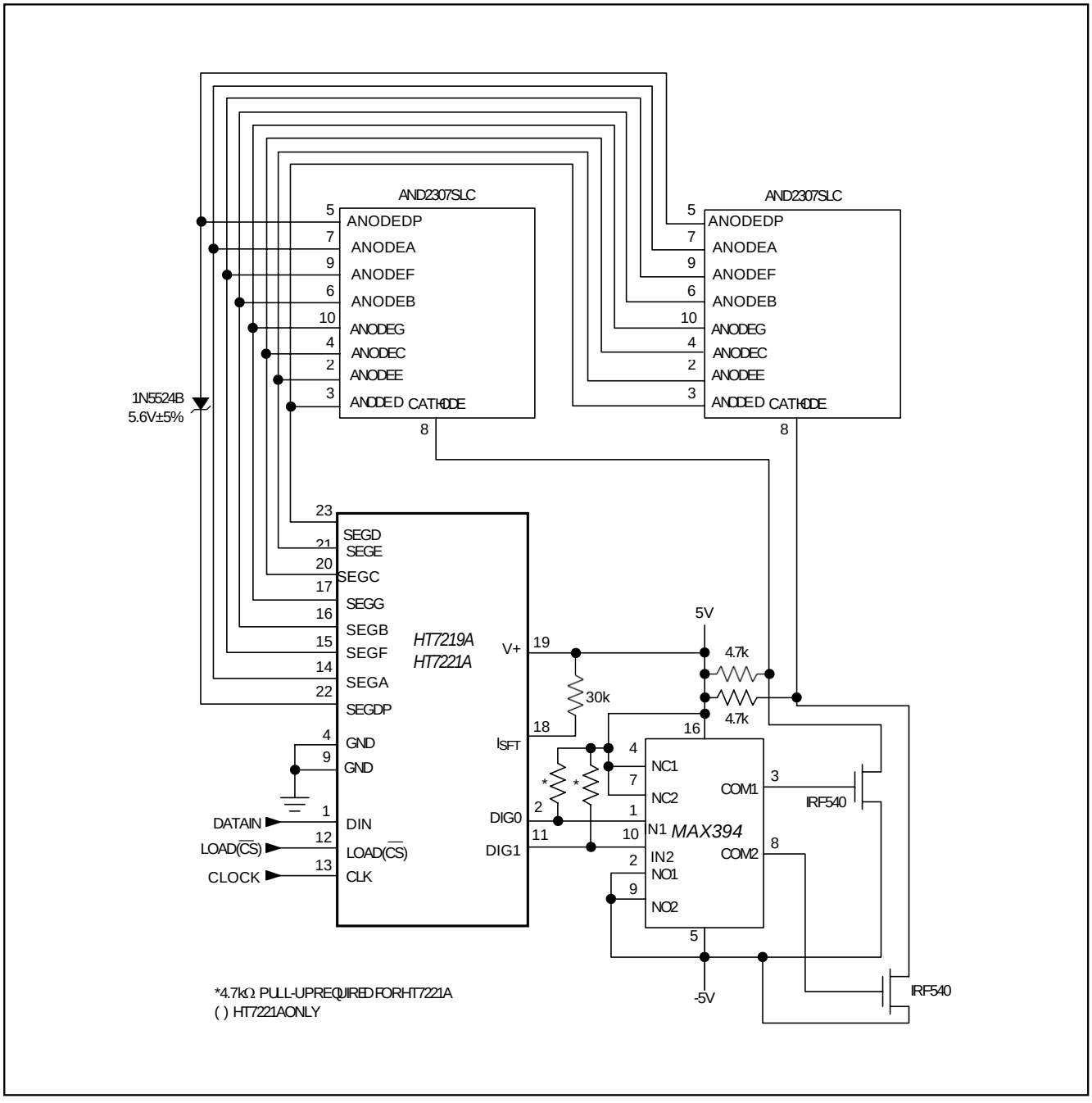
Thus, for a CERDIP package (θ_{JA} = +60°C/W from Table 12), the HTCSEMIum allowed ambient temperature T_A is given by:

$$T_{J(MAX)} = T_A + PD \times \theta_{JA} + 150°C = T_A + 1.11W \times 60°C/W$$

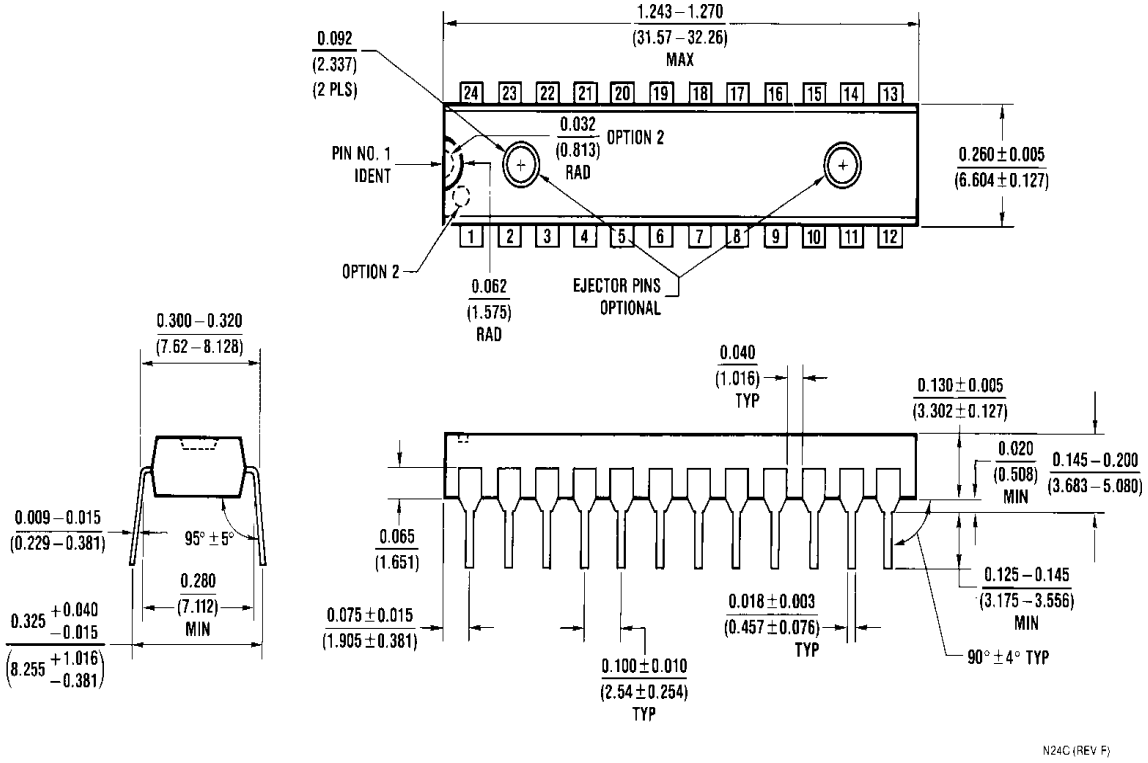
where T_A = +83.4°C.

Cascading Driv ers

The example in Figure 3 drives 16 digits using a 3-wire µP interface. If the number of digits is not a multiple of 8, set both drivers' scan limits registers to the same number so one display will not appear brighter than the other. For example, if 12 digits are need, use 6 digits per display with both scan-limit registers set for 6 digits so that both displays have a 1/6 duty cycle per digit. If 11 digits are needed, set both scan-limit registers for 6 digits and leave one digit driver unconnected. If one display for 6 digits and the other for 5 digits, the second display will appear brighter because its duty cycle per digit will be 1/5 while the first display's will be 1/6. Refer to the *No-Op Register* section for additional information.

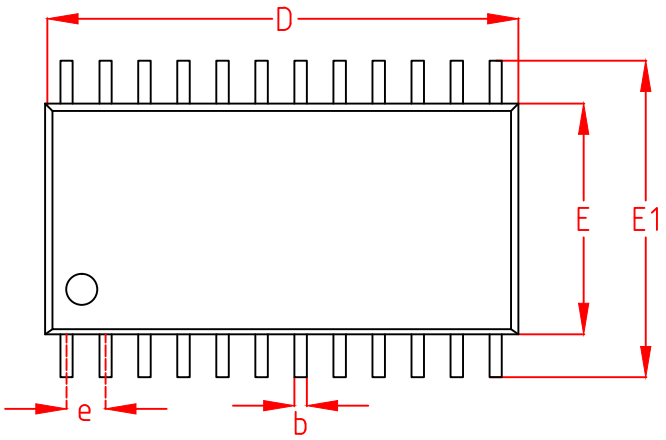

AND2307SLC
ANODEDP
ANODEA
ANODEF
ANODEB
ANODEG
ANODEC
ANODEE
ANODED
CATHODE
1N5524B
5.6V±5%
HT7219A
HT7221A
SEGD
SEGE
SEGC
SEGG
SEGB
SEGF
SEGA
SEGDP
GND
GND
DIN
LOAD(CS)
CLK
DATAIN
LOAD(CS)
CLOCK
V+
ISFT
DIG0
DIG1
5V
4.7k
4.7k
30k
MAX394
NC1
NC2
COM1
N1
IN2
NO1
NC2
COM2
IRF540
IRF540
-5V
*4.7kΩ PULL-UPREQUIRED FORHT7221A
( ) HT7221AONLY

DIP24

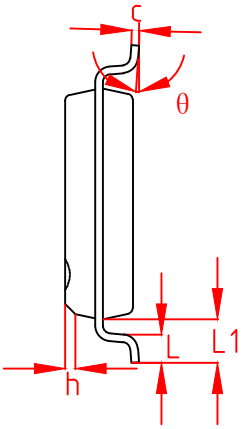

1.243–1.270
(31.57–32.26)
MAX
0.092
(2.337)
(2 PLS)
24 23 22 21 20 19 18 17 16 15 14 13
0.032
(0.813)
RAD
OPTION 2
PIN NO. 1
IDENT
0.260±0.005
(6.604±0.127)
1 2 3 4 5 6 7 8 9 10 11 12
OPTION 2
0.062
(1.575)
RAD
EJECTOR PINS
OPTIONAL
0.300–0.320
(7.62–8.128)
0.040
(1.016)
TYP
0.130±0.005
(3.302±0.127)
0.020
(0.508)
MIN
0.145–0.200
(3.683–5.080)
0.009–0.015
(0.229–0.381)
95° ±5°
0.280
(7.112)
MIN
0.065
(1.651)
0.125–0.145
(3.175–3.556)
MIN
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.075±0.015
(1.905±0.381)
0.018±0.003
(0.457±0.076)
TYP
0.100±0.010
(2.54±0.254)
TYP
90° ±4° TYP
N24C (REV F)

WSOP24

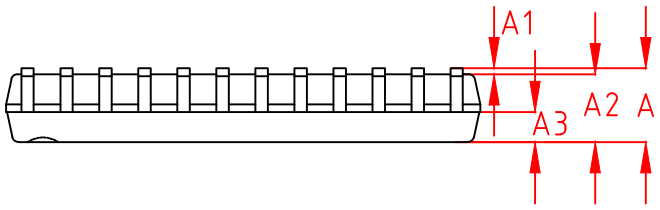
TOP VIEW
正视图



SIDE VIEW
侧视图



SIDE VIEW
侧视图

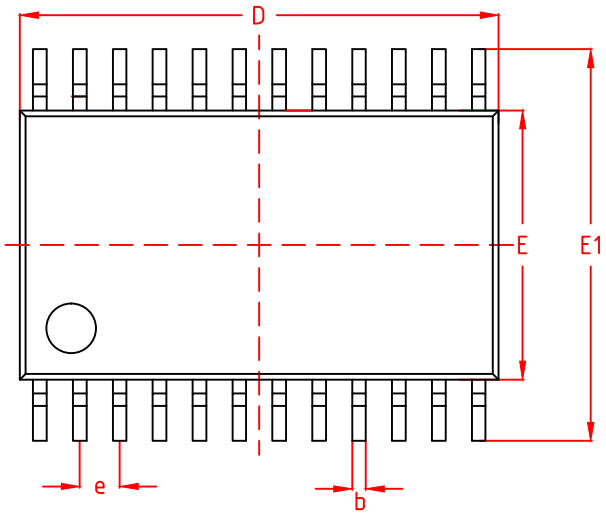


机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	2.65
A1	0.10	–	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	–	0.47
c	0.25	–	0.29
D	15.30	15.40	15.50
E	7.40	7.50	7.60
E1	10.10	10.30	10.50
e	1.27 BSC		
L1	1.40REF		
h	0.25	–	0.75
L	0.70	–	1.00
θ	0°	–	8°

TSSOP24

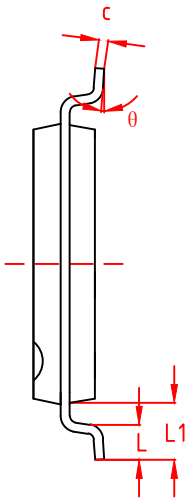
TOP VIEW

正视图



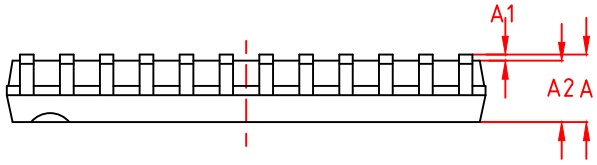
SIDE VIEW

侧视图



SIDE VIEW

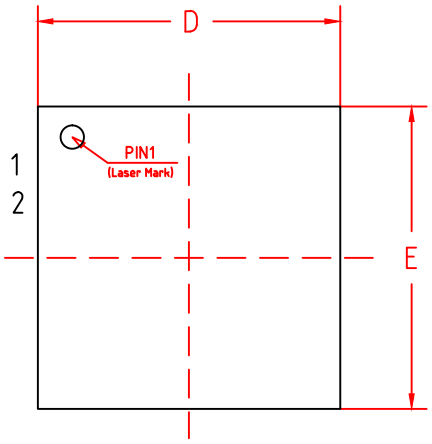
侧视图



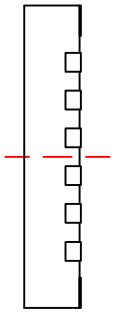
机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	7.70	7.80	7.90
E	4.30	4.40	4.50
E1	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
θ	0°	–	8°

QFN24L(4X4x0.75-P0.5)

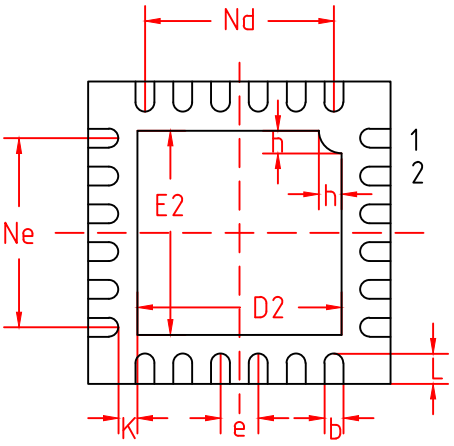
TOP VIEW
正视图



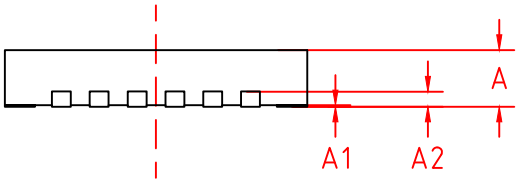
SIDE VIEW
侧视图



BOTTOM VIEW
背视图



SIDE VIEW
侧视图



机械尺寸/mm			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
A2	0.203 REF		
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
e	0.50 BSC		
K	0.20	0.25	0.30
L	0.30	0.40	0.50
h	0.25	0.30	0.35
Ne	2.50 BSC		
Nd	2.50 BSC		