UMW AO4405

P-Channel MOSFET

1.Description

The AO4405 uses advanced trench technologyto provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use as a load switch or in PWM applications.

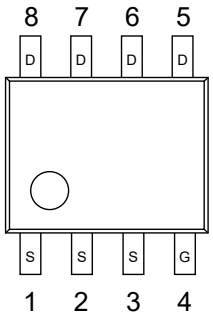
2.Features

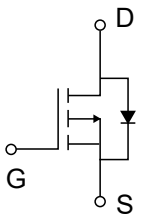
- V_{DS}=-30V
- I_D =-6A
- $R_{DS(ON)}$ <45mΩ(V_{GS}=10V)

3.Pinning information

Pin	Symbol	Description
4	G	GATE
1,2,3	S	SOURCE
5,6,7,8	D	DRAIN

SOP-8





4.Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25°C	I_D	-6	A
	T_A=70°C		-5.1	
Pulsed Drain Current [C]		I_{DM}	-30	
Avalanche Current [C]		I_{AS},I_{AR}	17	A
Avalanche energy L=0.1mH [C]		E_{AS},E_{AR}	14	mJ
V_{DS} Spike	10μs	V_{SPIKE}	-36	V
Power Dissipation [B]	T_A=25°C	P_D	3.1	W
	T_A=70°C		2	
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	31	40	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		59	75	°C/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	16	24	°C/W

6.Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=-250μA, V_{GS}=0V	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V, V_{GS}=0V			-1	μA
		T_J=55°C			-5	
Gate-Body leakage current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1	-1.5	-2.5	V
On state drain current	$I_{D(ON)}$	V_{GS}=-10V, V_{DS}=-5V	-30			A
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-6A		33	45	mΩ
		V_{GS}=-4.5V, I_D=-5A		53	75	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V, I_D=-6A		14		S
Diode Forward Voltage	V_{SD}	I_S=-1A, V_{GS}=0V		-0.8	-1	V
Maximum Body-Diode Continuous Current	I_S				-3.5	A
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-15V, f=1MHz		520		pF
Output Capacitance	C_{oss}			100		pF
Reverse Transfer Capacitance	C_{rss}			65		pF
Gate resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz	3.5	7.5	11.5	Ω
Total Gate Charge	Q_g(10V)	V_{GS}=-10V, V_{DS}=-15V, I_D=-6A		9.2	11	nC
Total Gate Charge	Q_g(4.5V)			4.6	6	nC
Gate Source Charge	Q_{gs}			1.6		nC
Gate Drain Charge	Q_{gd}			2.2		nC
Turn-On DelayTime	$t_{D(on)}$	V_{GS}=-10V, V_{DS}=-15V, R_L=2.5Ω,R_{GEN}=3Ω		7.5		ns
Turn-On Rise Time	t_r			5.5		ns
Turn-Off DelayTime	$t_{D(off)}$			19		ns
Turn-Off Fall Time	t_f			7		ns
Body Diode Reverse Recovery Time	t_{rr}	I_F=-6A, dI/dt=100A/μs		11		ns
Body Diode Reverse Recovery Charge	Q_{rr}	I_F=-6A, dI/dt=100A/μs		5.3		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on $1in^2$ FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on $1in^2$ FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating

7.1Typical characteristic

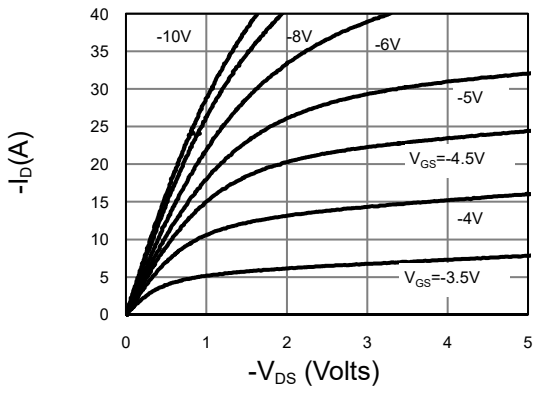


Fig 1: On-Region Characteristics (Note E)

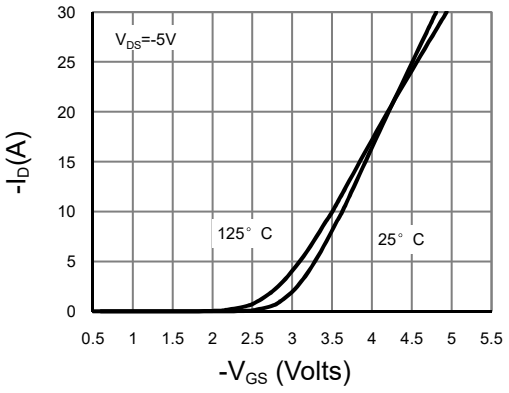


Figure 2: Transfer Characteristics (Note E)

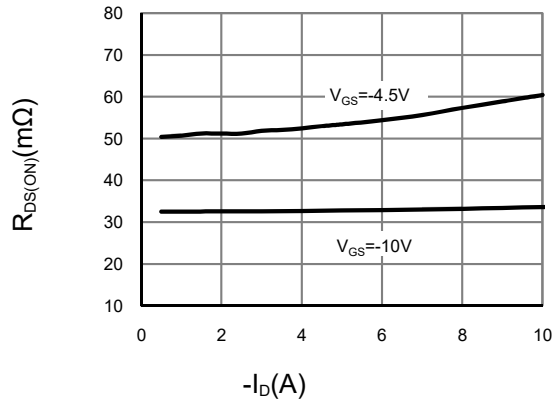


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

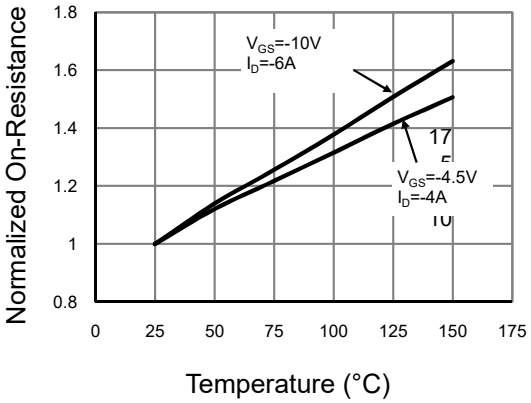


Figure 4: On-Resistance vs. Junction Temperature (Note E)

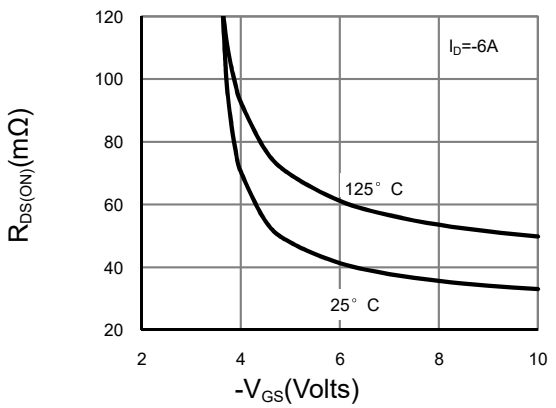


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

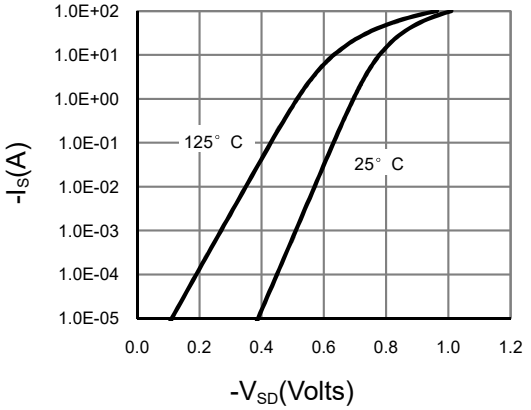


Figure 6: Body-Diode Characteristics(Note E)

7.2Typical characteristic

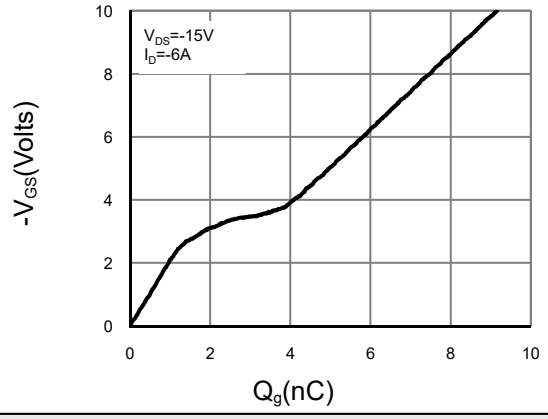


Figure 7: Gate-Charge Characteristics

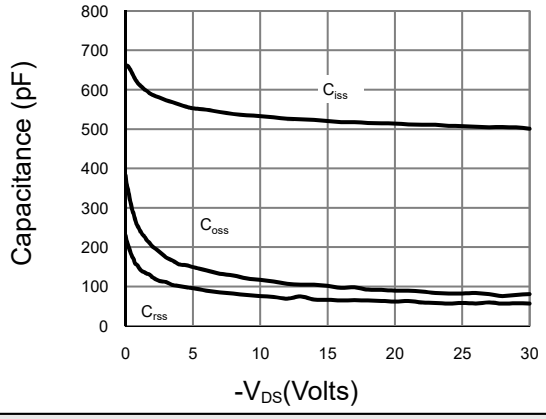


Figure 8: Capacitance Characteristics

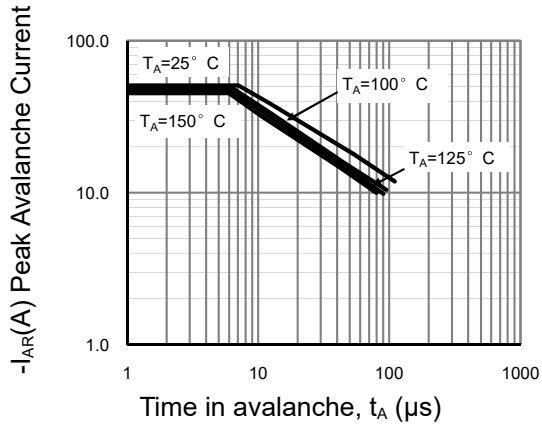


Figure 9: Single Pulse Avalanche capability (Note C)

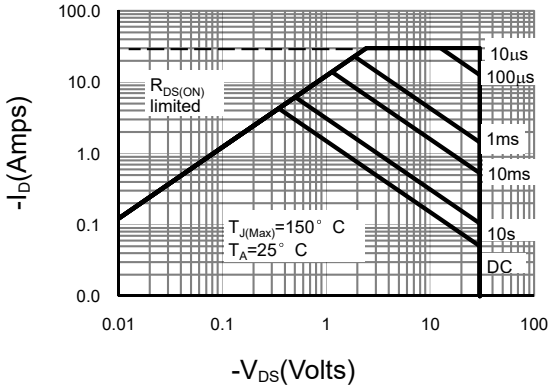


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

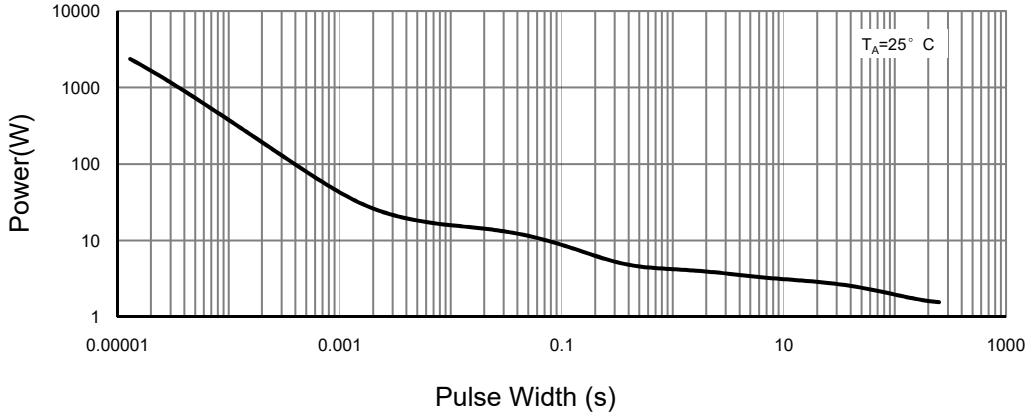


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

7.3Typical characteristic

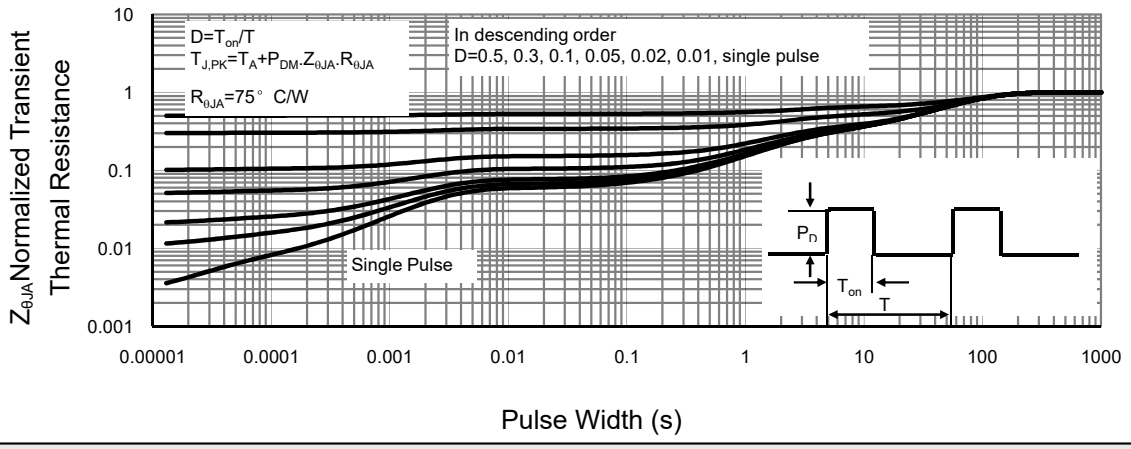
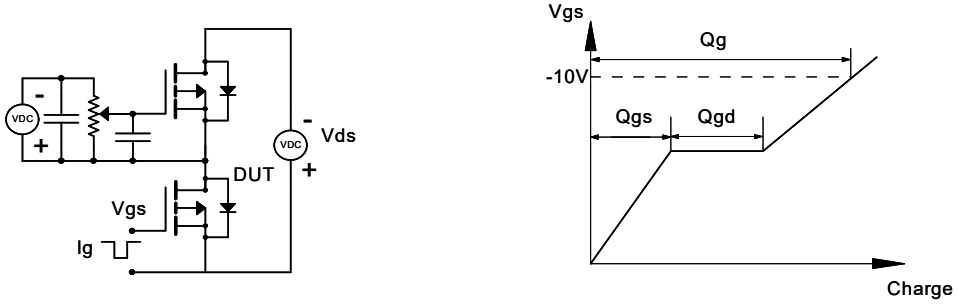
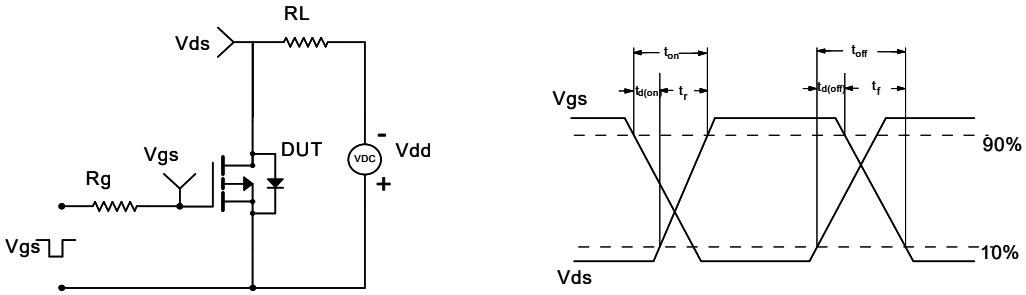


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

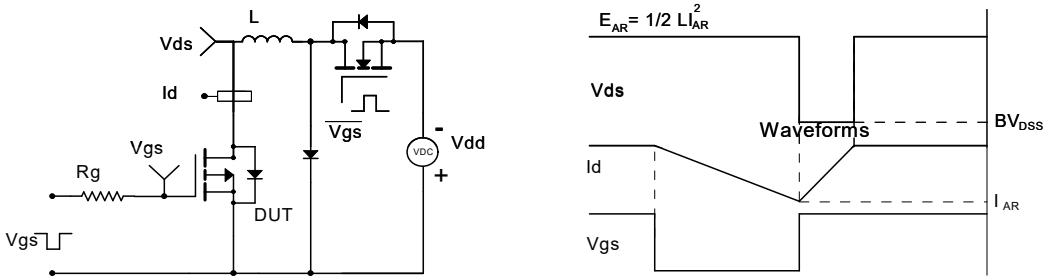
Gate Charge Test Circuit & Waveform



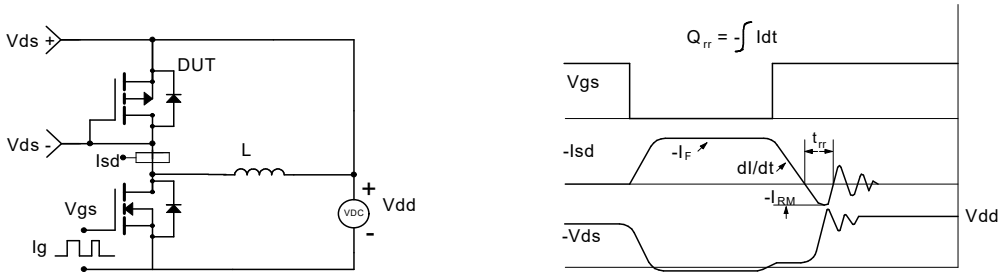
Resistive Switching Test Circuit & Waveforms



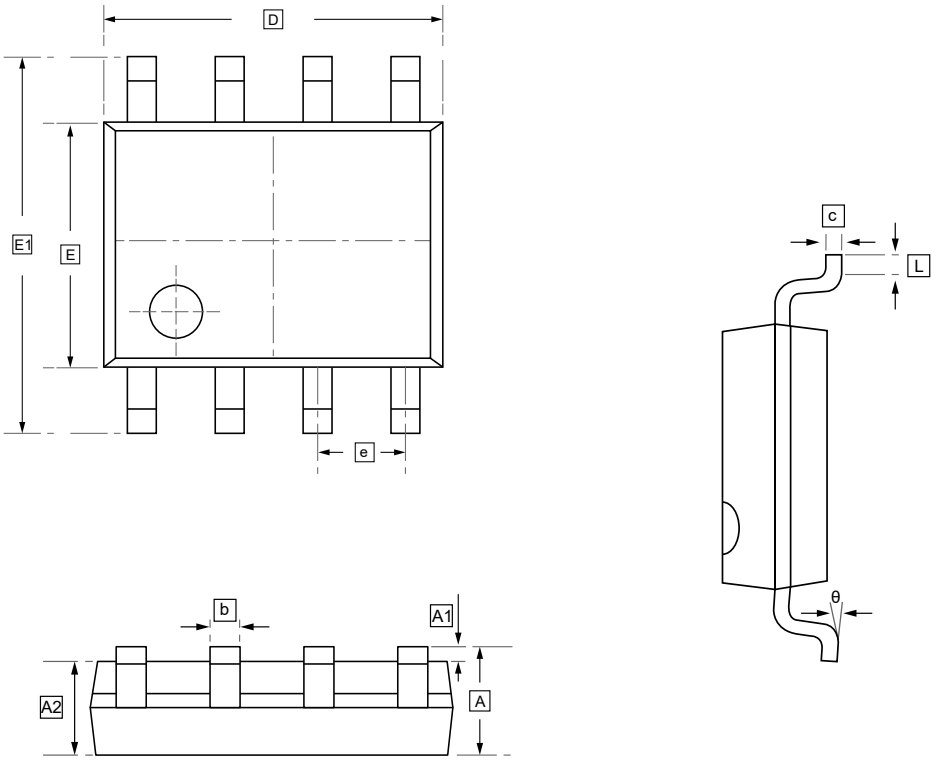
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



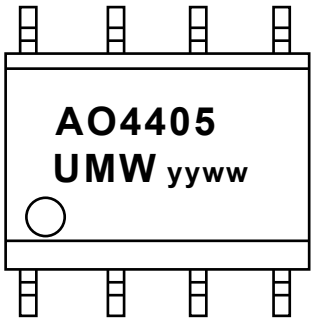
8.SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW AO4405	SOP-8	3000	Tape and reel

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