

1.Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

3.Benefits

- Low Input Capacitance
- Low On-Resistance
- Fast Switching Speed

2.Features

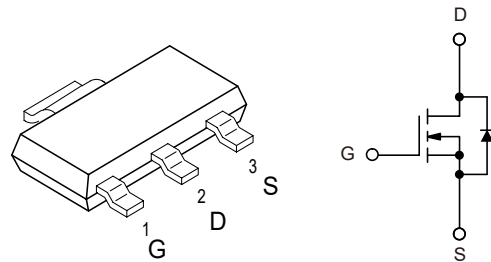
- $V_{DS}=60V$
- $R_{DS(ON)} < 50m\Omega (V_{GS}=10V)$
- $R_{DS(ON)} < 70m\Omega (V_{GS}=4.5V)$

- Lead-Free Finish
- Halogen and Antimony Free

4.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

SOT-223



5.Maximum ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter			Symbol	Maximum	Units
Drain-Source Voltage			V _{DSS}	60	V
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current V _{GS} =10V	(SteadyState)	T _A =+25°C (Note 6)	I _D	6.7	A
		T _A =+70°C (Note 6)		5.4	A
		T _A =+25°C (Note 5)		4.8	A
Maximum Body Diode Forward Current (Note 6)			I _S	5.7	A
Pulsed Drain Current (Note 7)			I _{DM}	28.5	A
Pulsed Source Current (Note 7)			I _{SM}	28.5	A



6. Thermal Characteristics

Parameter		Symbol	Max	Units
Total Power Dissipation	$T_A = +25^{\circ}\text{C}$ (Note 5)	P_D	2	W
Linear Derating Factor			16	mW/ $^{\circ}\text{C}$
Total Power Dissipation	$T_A = +25^{\circ}\text{C}$ (Note 6)	P_D	3.9	W
Linear Derating Factor			31	mW/ $^{\circ}\text{C}$
Thermal Resistance	Steady state (Note 5)	$R_{\theta JA}$	62.5	$^{\circ}\text{C/W}$
Junction to Ambient	Steady state (Note 6)		32	$^{\circ}\text{C/W}$
Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^{\circ}\text{C}$



7. $T_J=25^{\circ}\text{C}$ unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$			1	μA
Gate-Source Leakage	I_{GSS}	$V_{DS}=\pm 20V, V_{GS}=0V$			± 100	nA
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1			V
Static Drain-Source On-Resistance (Note 8)	$R_{DS(on)}$	$V_{GS}=10V, I_D=3.6A$			50	m Ω
		$V_{GS}=4.5V, I_D=3A$			70	m Ω
Diode Forward Voltage (Note 8)	V_{SD}	$V_{GS}=0V, I_S=5.5A$		0.85	0.95	V
Forward Transconductance (Note 8 & 10)	g_{FS}	$V_{DS}=15V, I_D=4.5A$		10.2		S
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V, f=1MHz$		1.063		pF
Output Capacitance	C_{oss}			104		pF
Reverse Transfer Capacitance	C_{rss}			64		pF
Total Gate Charge ($V_{GS}=5V$)	Q_g	$V_{DS}=30V, I_D=1.4A$		11		nC
Total Gate Charge ($V_{GS}=10V$)	Q_g			20.4		nC
Gate-Source Charge	Q_{gs}			4.1		nC
Gate-Drain Charge	Q_{gd}			5.1		nC
Turn-On Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=30V$ $R_G=6\Omega, I_D=1A$		3.8		ns
Turn-On Rise Time	t_r			4		ns
Turn-Off Delay Time	$t_{D(off)}$			26.2		ns
Turn-Off Fall Time	t_f			10.6		ns
Body Diode Reverse Recovery Time	t_{rr}	$I_F=2.2A, dI/dt=100A/\mu s$		22		ns
Body Diode Reverse Recovery Charge	Q_{rr}			21.4		nC



Notes:

5. For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions
6. For a device surface mounted on FR4 PCB measured at $t \leq 10$ secs.
7. Repetitive rating 25mm x 25mm FR4 PCB, $D = 0.02$, pulse width 300 μ s - pulse width limited by maximum junction temperature.
8. Measured under pulsed conditions. Width=300 μ s. Duty cycle $\leq 2\%$.
9. Short duration pulse test used to minimize self-heating effect.



8.1 Typical Characteristics

Figure 1: Safe Operating Area	Figure 2: Transfer Characteristics
Figure 3: Transient Thermal Impedance	Figure 4: Pulse Power Dissipation
Figure 5: Output Characteristics	Figure 6: Output Characteristics

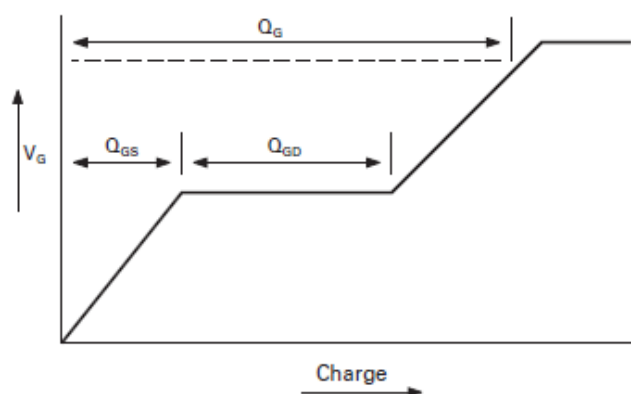


8.2Typical Characterisitics

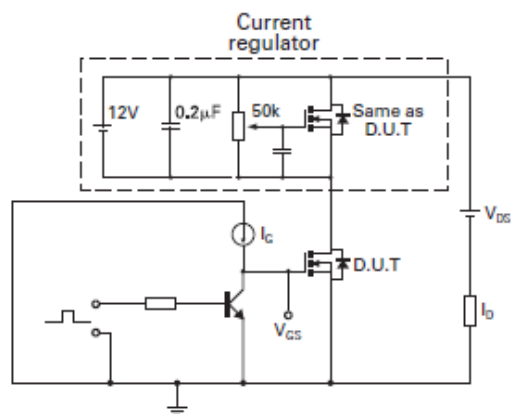
Figure 7: Typical Transfer Characteristics	Figure 8: Normalised Curves v Temperature
Figure 9: On-Resistance v Drain Current	Figure 10: Source-Drain Diode Forward Voltage
Figure 11: Capacitance v Drain-Source Voltage	Figure 12: Gate-Source Voltage v Gate Charge



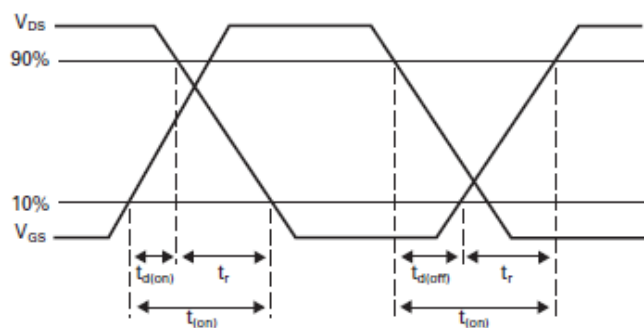
8.3 Typical Characteristics



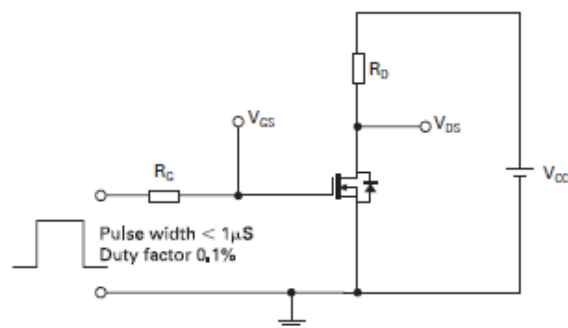
Basic gate charge waveform



Gate charge test circuit



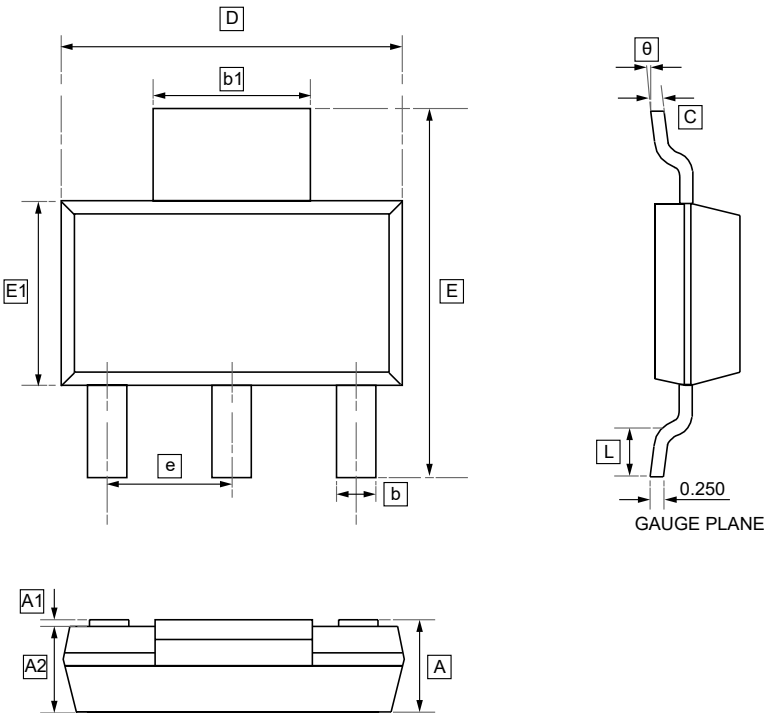
Switching time waveforms



Switching time test circuit



9.SOT-223 Package Outline Dimensions

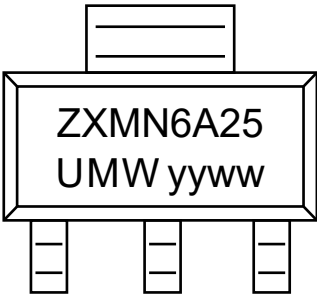


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	b1	c	D	E	E1	e	L	θ
Min	-	0.020	1.500	0.660	2.900	0.230	6.300	6.700	3.300	2.300	0.750	0°
Max	1.800	0.100	1.700	0.840	3.100	0.350	6.700	7.300	3.700	BSC	-	10°



10.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW ZXMN6A25GTA	SOT-223	2500	Tape and reel



11.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.