UMW IRLML5103TR

-30V P-Channel MOSFET

1.Description

The IRLML5103TR uses advanced trench technology to provide excellent $R_{DS(on)}$ with low gate charge. This device is suitable for use as a load switch or in PWM applications.

2.1Features

- $V_{DS\ (V)}$=-30V
- $R_{DS(ON)}$<600mΩ(V_{GS}=-10V)
- $R_{DS(ON)}$<1000mΩ(V_{GS}=-4.5V)

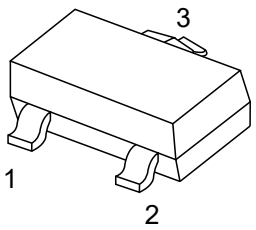
2.2Features

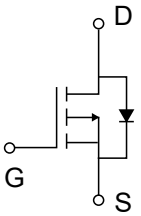
- Generation VTechnology
- UltraLowOn-Resistance
- P-Channel MOSFET
- RoHS CompliantHalogen-Free
- Low Profile(<1.1mm)
- Available in Tape and Reel
- Fast Switching
- Lead-Free

4.Pinning information

Pin	Symbol	Description
1	G	GATE
2	S	SOURCE
3	D	DRAIN

SOT-23





5.Maximum ratings (T_A=25°C unless otherwise noted)

Parameter		Symbol	Value	Units
Continuous Drain Current, V_{GS} @ -10V	T_A=25°C	I_D	-0.76	A
Continuous Drain Current, V_{GS} @ -10V	T_A=70°C		-0.61	
Pulsed Drain Current ①		I_{DM}	-4.8	
Power Dissipation	T_A=25°C	P_D	540	mW
Linear Derating Factor			4.3	mW/°C
Gate-to-Source Voltage		V_{GS}	±20	V
Peak diode Recovery dv/dt ②		dv/dt	-5	V/ns
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to 150	°C

6.Thermal resist ance rating

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambien ④	$R_{\theta JA}$		230	°C/W

7.Electrical Characteristics T_J=25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=-250μA, V_{GS}=0V	-30			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D=-1mA, Reference to 25°C		0.029		V/°C
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-0.6A ③			600	mΩ
		V_{GS}=-4.5V, I_D=-0.3A ③			1000	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1			V
Forward Transconductance	g_{fs}	V_{DS}=-10V, I_D=-0.3A	0.44			S
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=-24V,V_{GS}=0V			-1	μA
		V_{DS}=-24V,V_{GS}=0V,T_J=125°C			-25	
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS}=-20V			-100	nA
Gate-to-Source Reverse Leakage		V_{GS}=20V			100	
Total Gate Charge	Q_g	I_D=-0.6A		3.4	5.1	nC
Gate-to-Source Charge	Q_{gs}	V_{DS}=-24V		0.52	0.78	
Gate-to-Drain ("Miller") Charge	Q_{gd}	V_{GS}=-10V,See Fig.6 and 9 ③		1.1	1.7	
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=-15V		10		ns
Rise Time	t_r	I_D=-0.6A		8.2		
Turn-Off Delay Time	$t_{D(off)}$	R_G=6.2Ω		23		
Fall Time	t_f	R_D=25Ω, See Fig.10 ③		16		
Input Capacitance	C_{iss}	V_{GS}=0V		75		pF
Output Capacitance	C_{oss}	V_{DS}=-25V		37		
Reverse Transfer Capacitance	C_{rss}	f=1MHz, See Fig.5		18		

Source-Drain Ratings and Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			-0.54	A
Pulsed Source Current (Body Diode) ①	I_{SM}				-4.8	
Diode Forward Voltage	V_{SD}	T_J=25°C,I_S=-0.6A,V_{GS}=0V ③			-1.2	V
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=-0.6A		26	39	ns
Reverse Recovery Charge	Q_{rr}	dI/dt=100A/μs ③		20	30	nC

Notes:

① Repetitive rating; pulse width limited bymax.junction temperature.(See fig.11)

② I_{SD}≤ -0.6A, di/dt ≤ 110A/μS, V_{DD} ≤ $V_{(BR)DSS}$,T_J≤ 150°C

③ Pulse width ≤ 300us; duty cycle ≤ 2%.

④ Surface mounted on FR-4 board, t≤ 5sec.

8.1Typical Characterisitics

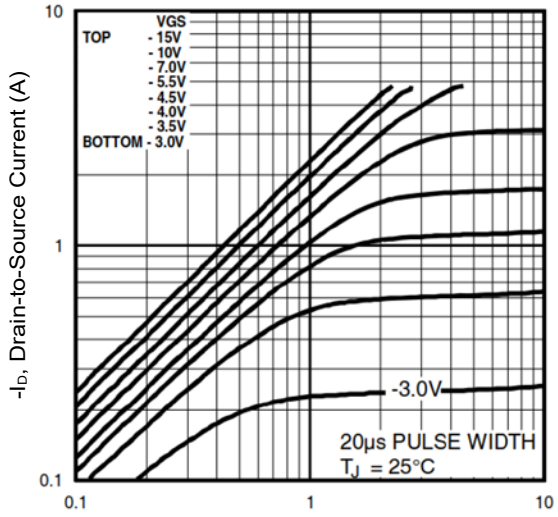


Fig 1. Typical Output Characteristics

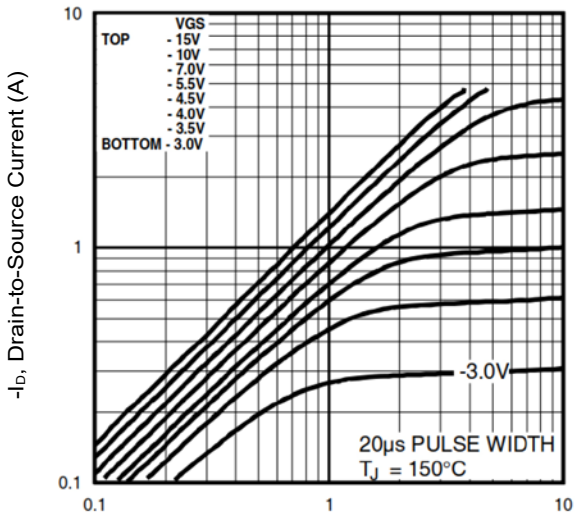


Fig 2. Typical Output Characteristics

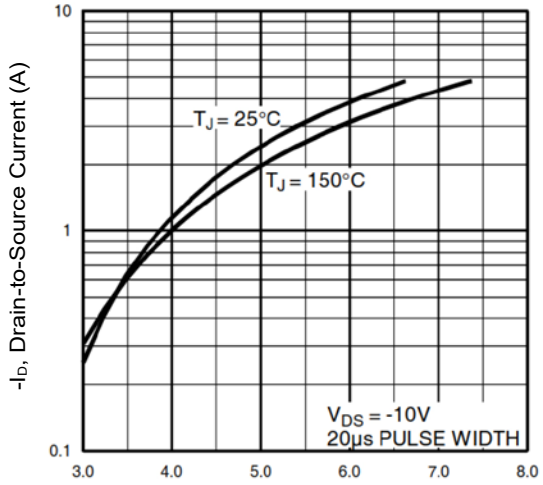


Fig 3. Typical Transfer Characteristics

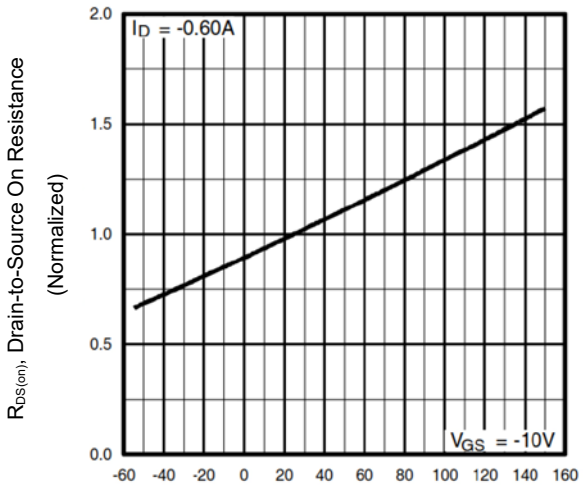
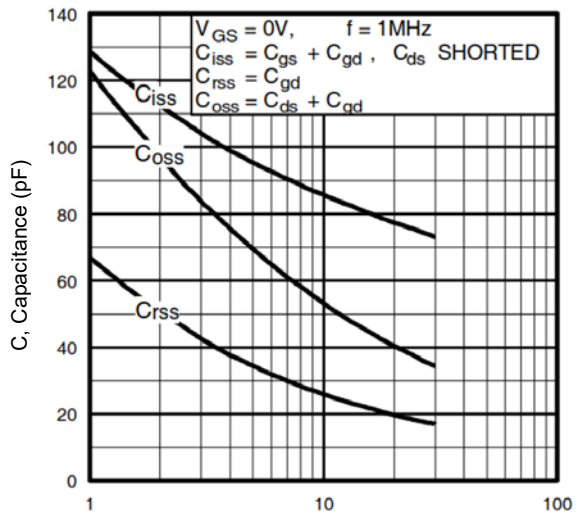


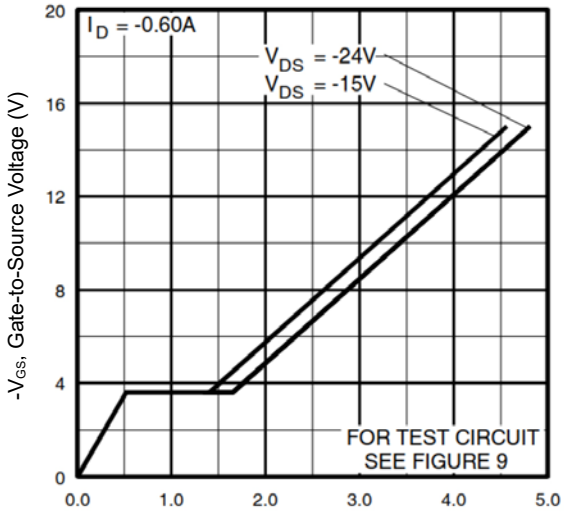
Fig 4. Nomalized On-ResistanceVs. Temperature

8.2Typical Characterisitics



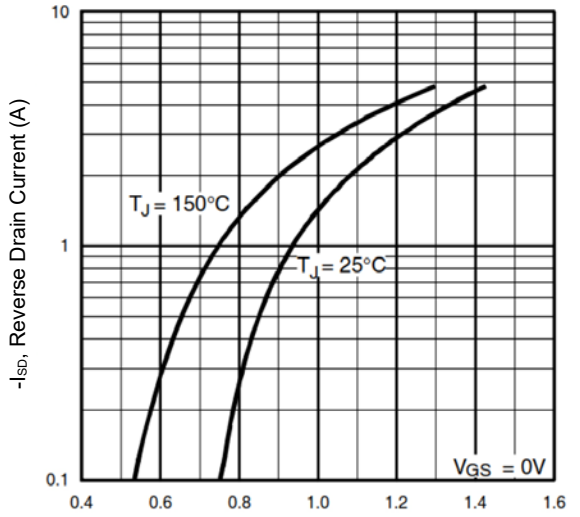
$-V_{DS}$,Drain-to-Source Voltage (V)

Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage



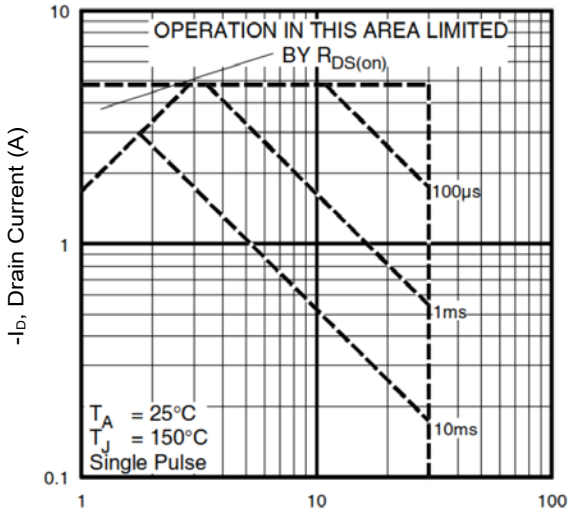
Q_G, Total Gate Charge (nC)

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage



$-V_{SD}$, Source-to-Drain Voltage (V)

Fig 7. Typical Source-Drain Diode Forward Voltage



$-V_{DS}$, Drain-to-Source Voltage (V)

Fig 8. Maximum Safe Operating Area

8.3Typical Characterisitics

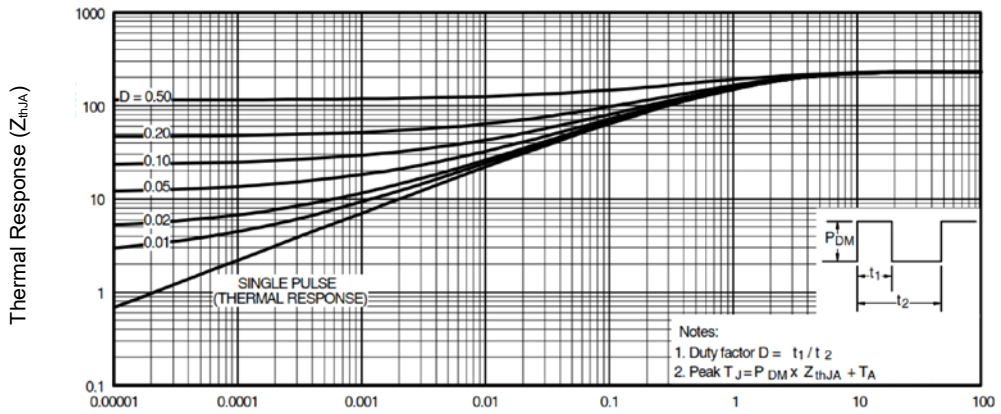


Figure 9. Maximum Effective Transient Themal Impedance, Junction-to-Ambient

8.4Typical Characterisitics

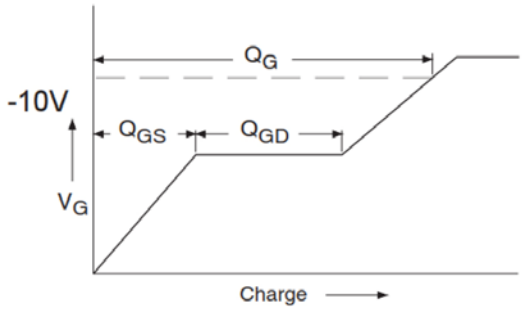


Fig 10a. Basic Gate Charge Wavefomm

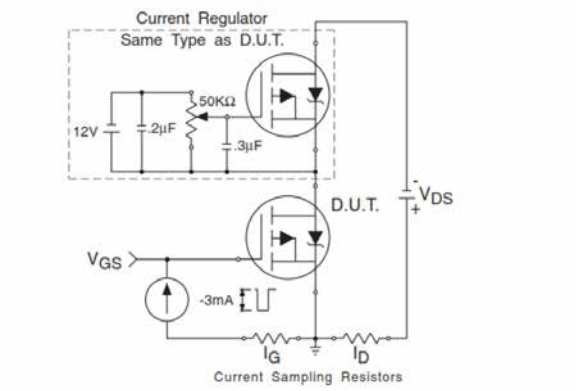


Fig 10a. Switching Time Test Circuit

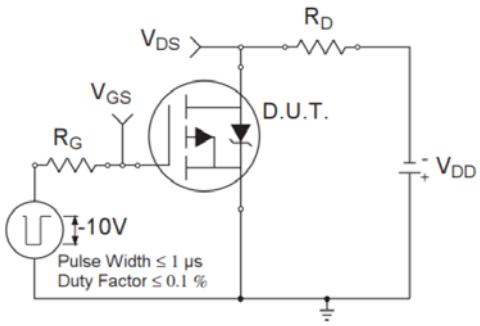


Fig 11a. Gate Charge Test Circuit

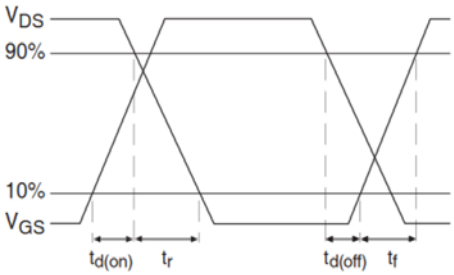
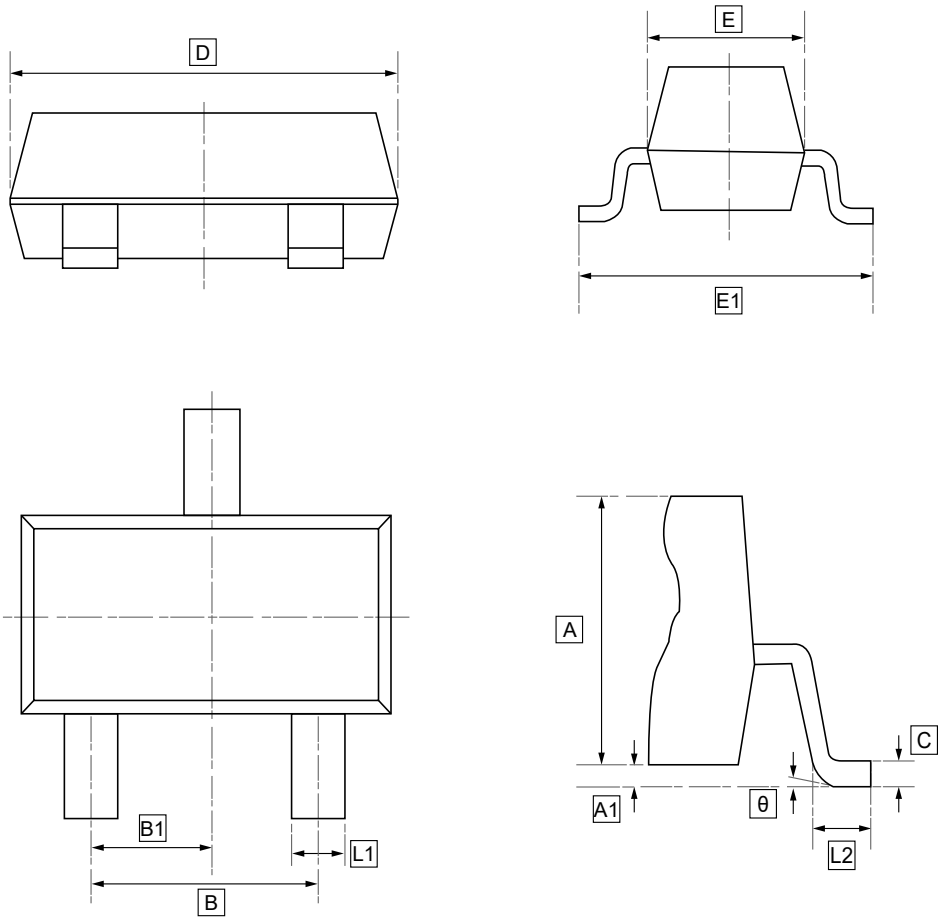


Fig 11b. Switching Time Wavefomms

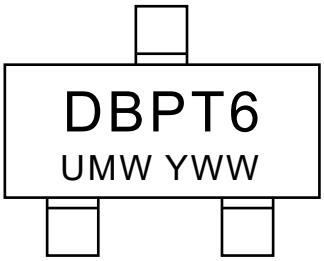
9.SOT-23 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	L1	L2	C	D	E	E1	B	B1	θ
Min	1.050	0.000	0.300	0.350	0.100	2.820	1.500	2.700	1.800	0.950	0°
Max	1.150	0.100	0.500	0.550	0.200	3.020	1.700	2.900	2.000	TYP	8°

10.Ordering information



YWW: Batch Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRLML5103TR	SOT-23	3000	Tape and reel

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