

1.Description

This N-Channel MV MOSFET is produced using process that has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

2.2Features

- Low Gate Charge
- Fast Switching

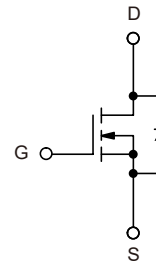
2.1Features

- $V_{DS(V)}=100V$
- $I_D=76A(V_{GS}=10V)$
- $R_{DS(ON)}<8.5m\Omega(V_{GS}=10V)$

- Improved dv/dt Capability
- RoHS Compliant

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	SOURCE
3	S	DRAIN



4.Absolute Maximum Ratings $T_c=25^{\circ}C$

Parameter	Symbol	Rating	Units
Drain to Source Voltage	V_{DS}	100	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current - Continuous $T_c=25^{\circ}C$ (Note 3)	I_D	76	A
- Continuous $T_c=100^{\circ}C$ (Note 3)		54	A
- Pulsed (Note 1)		304	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	181	mJ
Power Dissipation $T_c=25^{\circ}C$	P_D	107	W
Power Dissipation $T_A=25^{\circ}C$		2.4	W
Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^{\circ}C$

* Drain current limited by maximum junction temperature.



5.Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W



6. Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	100			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I _D =250μA Referenced to 25°C		57		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V				μA
		V _{DS} =80V, T _J =150°C			1	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			500	nA
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =130μA	2	3	4	V
Static Drain to Source On Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =76A		7.4	8.5	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =76A		68		S
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz		1765	2475	pF
Output Capacitance	C _{oss}			1010	1415	pF
Reverse Transfer Capacitance	C _{rss}			16	25	pF
Gate Resistance	R _g		0.1	0.8	1.6	Ω
Turn-On Delay Time	t _{D(on)}	V _{DD} =50V, I _D =76A V _{GS} =10V, R _{GEN} =6Ω		12	22	ns
Rise Time	t _r			11	20	ns
Turn-Off Delay Time	t _{D(off)}			18	28	ns
Fall Time	t _f			4	10	ns
Total Gate Charge	Q _g	V _{GS} =0V to 10 V	V _{DD} =50V	25	34	nC
Gate to Source Gate Charge	Q _{gs}	I _D =76A		9		nC
Gate to Drain "Miller" Charge	Q _{gd}			5		nC
Output Charge	Q _{oss}	V _{DD} =50V, V _{GS} =0V		68		nC
Maximum Continuous Drain to Source Diode Forward Current	I _S				76	A
Maximum Pulsed Drain to Source Diode Forward Current	I _{SM}				304	A



Source to Drain Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=76A$		1	1.3	V
Reverse Recovery Time	t_{rr}	$V_{GS}=0V, V_{DD}=50V, I_F=76A$		58	92	ns
Reverse Recovery Charge	Q_{rr}	$dI_F/dt=100A/\mu s$		53	85	nC
Reverse Recovery Time	t_{rr}	$V_{GS}=0V, V_{DD}=50V, I_F=76A$		51	81	ns
Reverse Recovery Charge	Q_{rr}	$dI_F/dt=300A/\mu s$		141	226	nC

Notes:

1. Pulsed I_d please refer to Figure 11 & Figure 12 "Forward Bias Safe Operating Area" for more details.
2. E_{AS} of 181 mJ is based on starting $T_J=25^\circ C$, $L=3mH$, $I_{AS}=11A$, $V_{DD}=100V$, $V_{GS}=10V$. 100% test at $L=0.3mH$, $I_{AS}=25A$.
3. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.



7.1 Typical characteristic

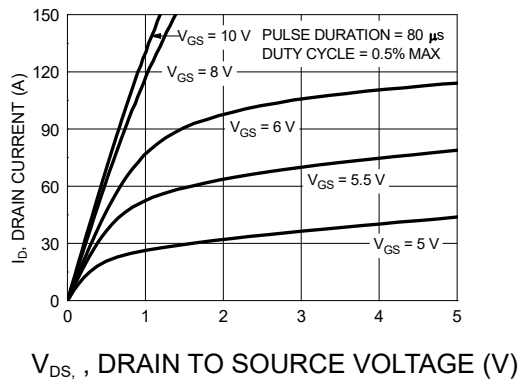


Figure 1: On-Region Characteristics

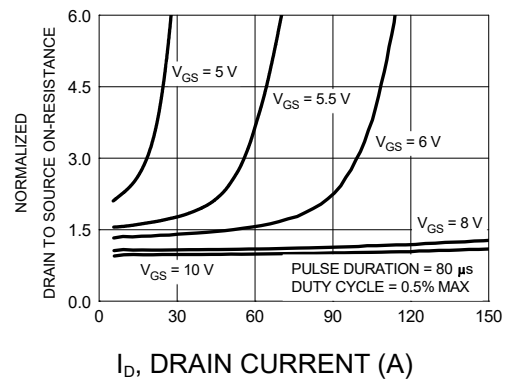


Figure 2: Normalized On-Resistance vs. Drain Current and Gate Voltage

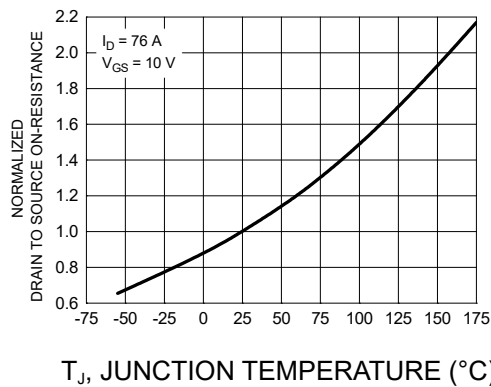


Figure 3: Normalized On Resistance vs. Junction Temperature

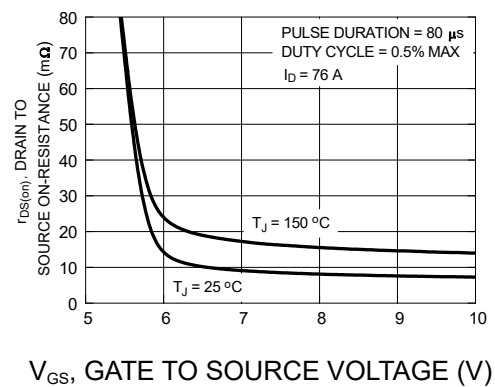


Figure 4: On-Resistance vs. Gate to Source Voltage

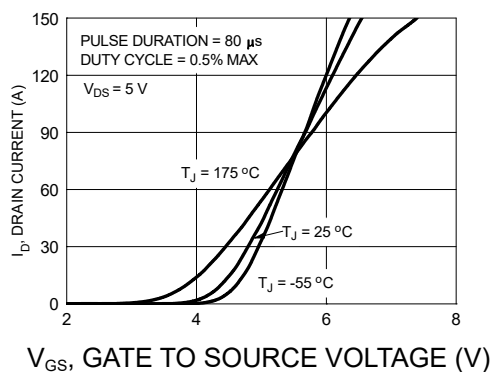


Figure 5: Transfer Characteristics

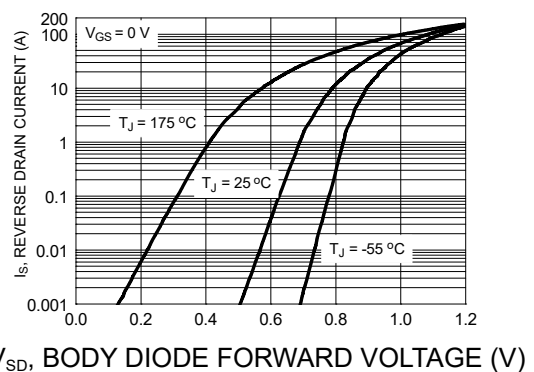


Figure 6: Source to Drain Diode Forward Voltage vs. Source Current



7.2 Typical characteristic

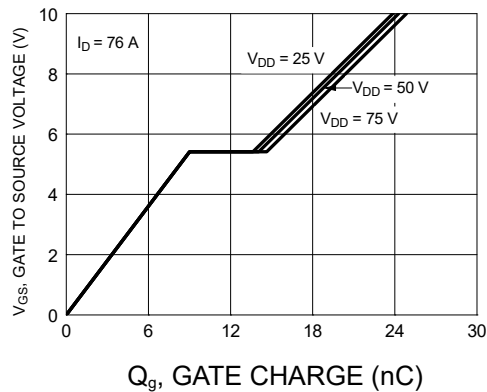


Figure 7: Gate Charge Characteristics

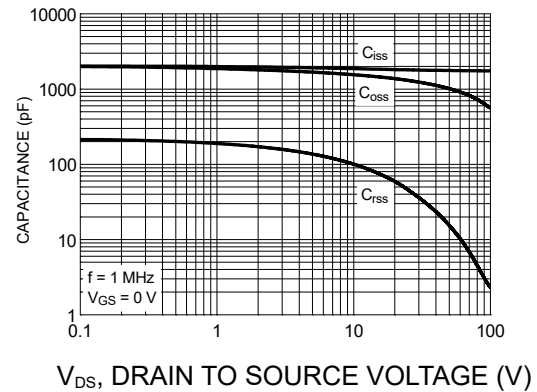


Figure 8: Capacitance vs. Drain to Source Voltage

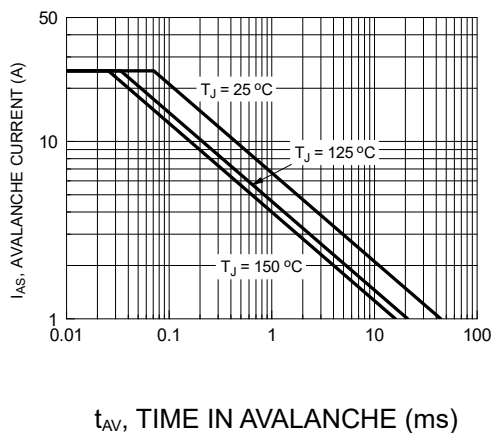


Figure 9: Unclamped Inductive Switching Capability

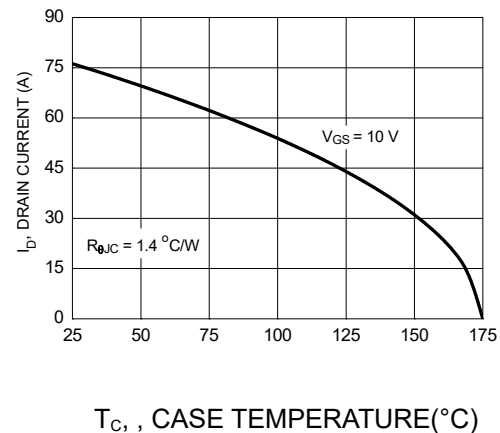


Figure 10: Maximum Continuous Drain Current vs Case Temperature

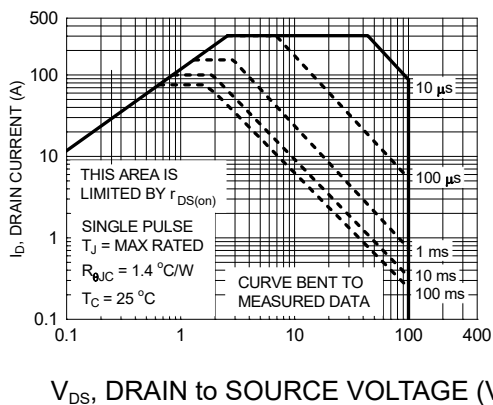


Figure 11: Forward Bias Safe Operating Area for FDP8D5N10C

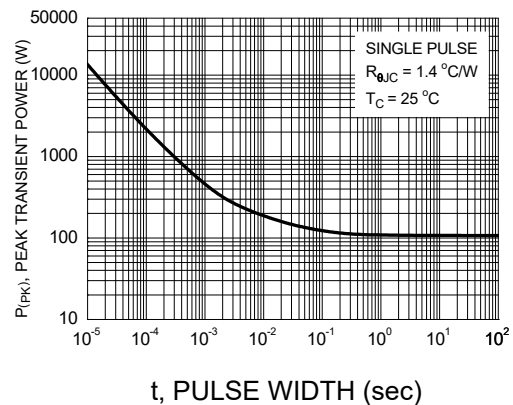


Figure 12: Single Pulse Maximum Power Dissipation for FDP8D5N10C



7.3 Typical characteristic

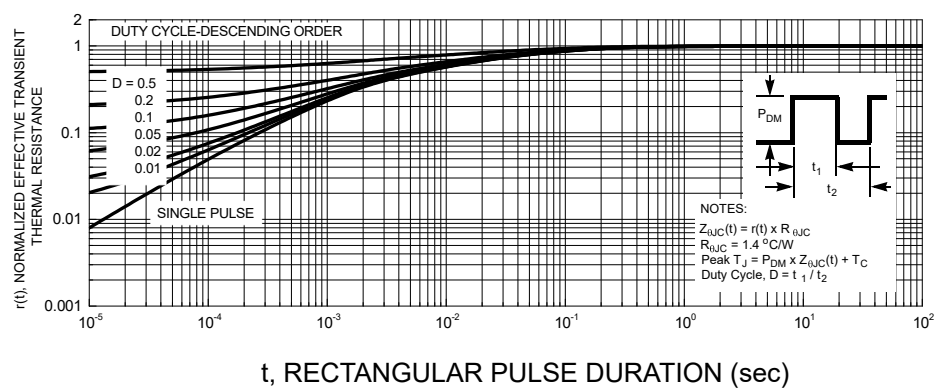


Figure 13: Junction-to-Case Transient Thermal Response Curve for FDP2D3N10C

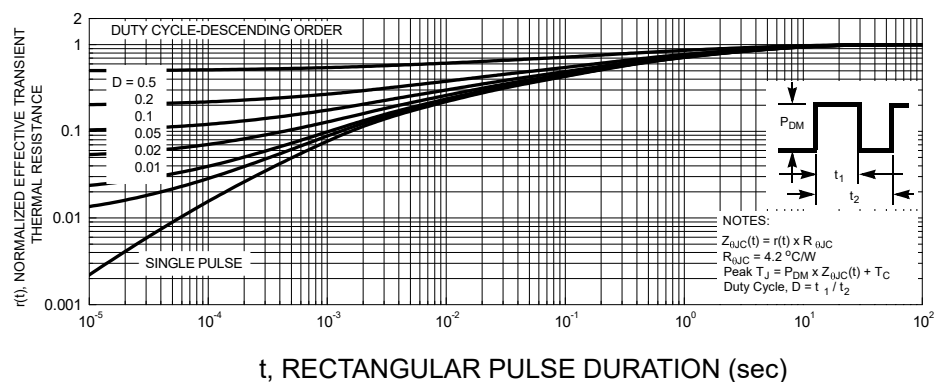
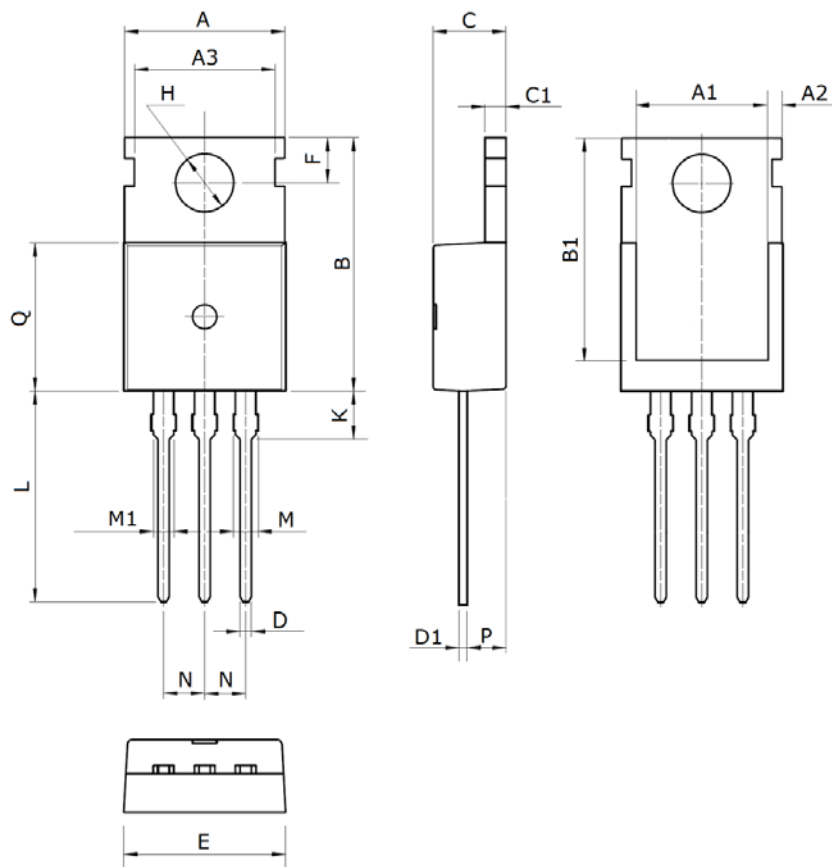


Figure 14: Junction-to-Case Transient Thermal Response Curve for FDPF2D3N10C



8.Package Mechanical Data TO-220

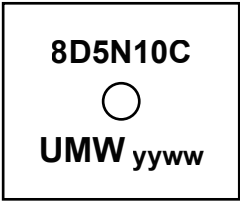


DIMENSIONS (mm are the original dimensions)

Symbol	Dimensions(mm)	Symbol	Dimensions(mm)	Symbol	Dimensions(mm)
A	10.0±0.3	C1	1.3±0.2	L	13.2±0.4
A1	8.0±0.2	D	0.8±0.2	M	1.38±0.1
A2	0.94±0.1	D1	0.5±0.1	M1	1.28±0.1
A3	8.7±0.1	E	10.0±0.3	N	2.54(typ)
B	15.6±0.4	F	2.8±0.1	P	2.4±0.3
B1	13.2±0.2	H	3.6±0.1	Q	9.15±0.25
C	4.5±0.2	K	3.1±0.2		



9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDP8D5N10C	TO-220	1000	Tube and box



10.Disclaimer

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