STK31862

Ambient Light Sensor with I2C interface

Preliminary Datasheet

Version – 0.9.4

Hazardous Substance Free
RoHS / REACH Compliant

Sensortek Technology Corporation

1. OVERVIEW

Description

The STK31862 is an integrated ambient to digital converter with I²C interface. This device provides ambient light sensing to allow robust backlight/display brightness control .

For ambient light sensing, the STK31862 incorporates a photodiode, timing controller and ADC in a single chip. The excellent spectral response is designed to be close-to human eye. The STK31862 is suitable for detecting a wide range of light intensity environment.

The STK31862 has excellent temperature compensation, robust on-chip refresh rate setting without external components. Software shutdown mode control is provided for power saving application. The STK31862 operating voltage range is 1.7V to 2.0V.

Feature

- Integrated ambient light sensor in one package.

Ambient Light Sensor

- Convert ambient light intensity to 16-bit digital data format
- 3rd generation ambient light sensor which closes to human-eye response and suppress IR portion
- Flexible digital settings
  - Long integration time : 8 steps IT
    - 3.125 / 6.25 / 12.5 /... / 200 / 400 ms
  - Short integration time : 20 steps IT
    - 192 / 288 / ... / 2112 us
- Flexible interrupt setting
  - Interrupt while out-of- window
  - Persistence : 1/2/4/8 times
- Clear channel for different light source identification
- FIFO buffer size is 1024 byte
  - FIFO mode
  - Stream mode

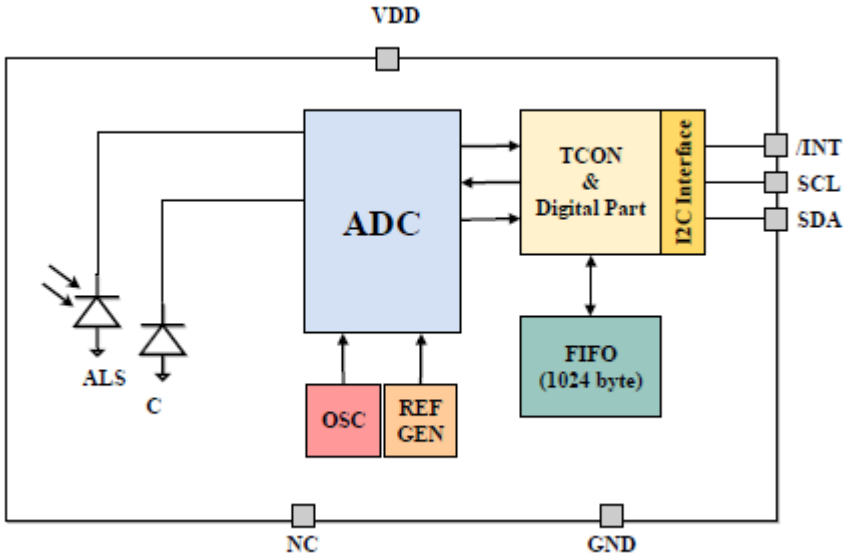
General

- Fully digital control with I²C interface
  - 1.7 ~ 3.6V I²C interface
- Low power design
  - Standby mode
  - Wait mode
- V_{DD} wide operation voltage : 1.7~2.0V
- Excellent temperature compensation: -40 to 85°C
- Available package options: OPLGA
  - STK31862 : 2 x 1 x 0.5 (mm)
- Lead-free package (RoHS compliant)
- Moisture Sensitivity Level 3

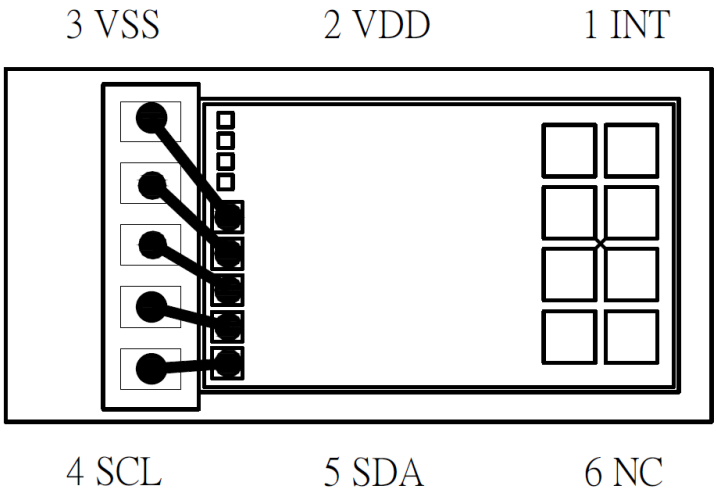
Applications

- Mobile Phone, Smart-phone, PDA

2. FUNCTION BLOCK



3. PINOUT DIAGRAM



Top View

4. PIN DESCRIPTION

Pin No.	Pin Name	Dir.	Pin Function
1	/INT	O	Interrupt pin, LO for interrupt alarming. (Open Drain)
2	VDD	PWR	Power supply: 1.7V to 2.0V.
3	VSS	VSS	Ground. The thermal pad is also connected to the VSS pin.
4	SCL	I	I²C serial clock line.
5	SDA	B	I²C serial data line. (Open Drain)
6	NC	-	No connect

Direction denotation:

O	Output	GND	Ground
I	Input	B	Bi-direction
PWR	Power	NC	Not Connect

5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply voltage	-0.3	2.15	V
Ta	Operation temperature	-40	85	°C

NOTE: All voltages are measured with respect to GND

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply voltage	1.7	2.0	V
f_{I2C}	Clock frequency of I²C	—	400	KHz
Ta	Operation temperature	-40	85	°C

NOTE: All voltages are measured with respect to GND

Symbol	Parameter	Max.	Unit
ESD	Electrostatic discharge protection	2 (HBM)	kV
		200 (MM)	V
		100 (Latch Up)	mA

NOTE: All voltages are measured with respect to GND

5.1 Electrical and Optical Characteristics

V_{DD} = 1.8V , under room temperature 25°C (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Operation Characteristics						
I_{ALS}	ALS only supply current	Note2		200		μA
I_{SD}	Shutdown current	Note2		3	5	μA
V_{IH}	Logic high, I²C	Note6	1.3		V_{DD}	V
V_{IL}	Logic low, I²C	Note7	—		0.4	V
ALS Characteristics						
λp_1	Peak sensitivity wavelength for ALS			550		nm
ALS_{FSCNT}	Full scale ALS counts				65535	counts
ALS_{DARK}	ALS dark offset	Note2,4		10		counts
ALS_{SENSE}	ALS sensing tolerance	Note2,3	-12.5		+12.5	%

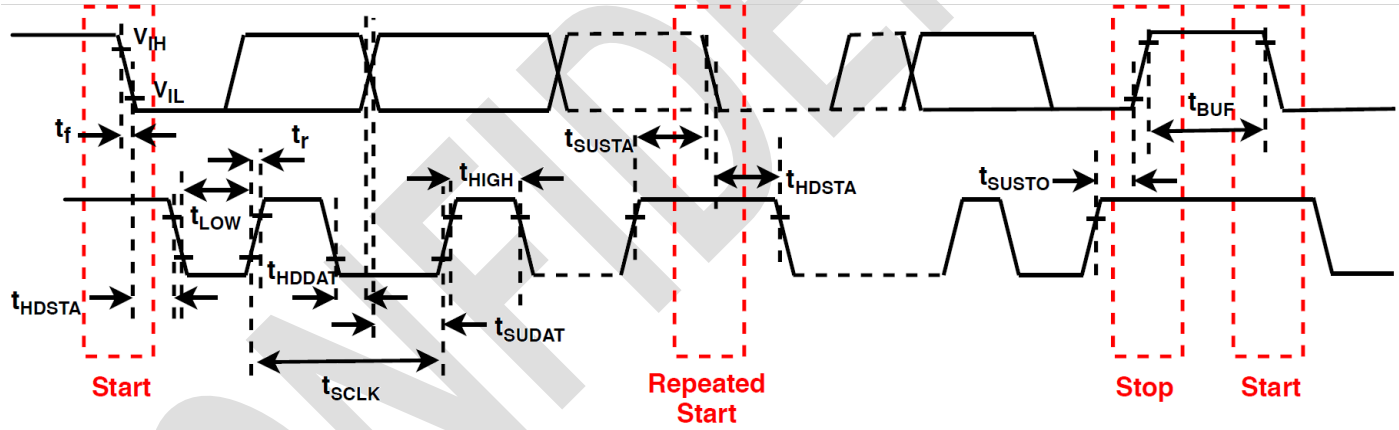
Note 2 : ALS : GAIN_ALS_DX128[0] = 1'b1,IT2_ALS[4:0] = 5'b00101.
Note 3 : White LED parallel light source.
Note 4 : $E_{ambient}$ = 0 Lux.
Note 6 : I²C logical high voltage level is specified as worst-case condition when all of the recommended operation supply voltages (V_{DD}) are taken into consideration. The logical high level is different when different supply voltage is applied.
Note 7 : I²C logical low voltage level is specified as worst-case condition when all of the recommended operation supply voltages (V_{DD}) are taken into consideration. The logical low level is different when different supply voltage is applied.

5.2 Timing Chart

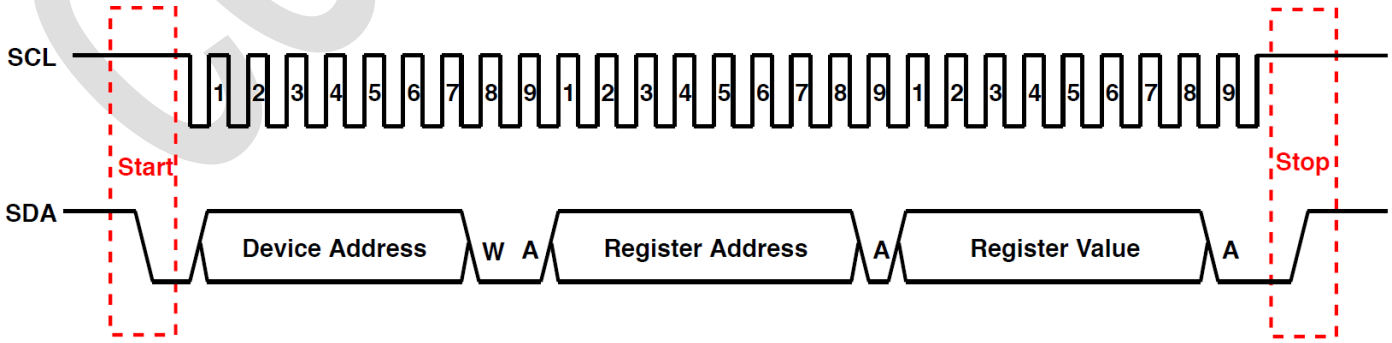
Characteristics of the SDA and SCL I/O

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCLK}	SCL clock frequency	10	100	10	400	KHz
t_{HDSTA}	Hold time after (repeated) start condition. After this period, the first clock is generated	4.0	—	0.6	—	μs
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	μs
t_{HIGH}	HIGH period of the SCL clock	4.0	—	0.6	—	μs
t_{SUSTA}	Set-up time for a repeated START condition	4.7	—	0.6	—	μs
t_{HDDAT}	Data hold time	0	—	0	—	ns
t_{SUDAT}	Data set-up time	250	—	100	—	ns
t_r	Rise time of both SDA and SCL signals	—	1000	—	300	ns
t_f	Fall time of both SDA and SCL signals	—	300	—	300	ns
t_{SUSTO}	Set-up time for STOP condition	4.0	—	0.6	—	μs
t_{BUF}	Bus free time between a STOP and START condition	4.7	—	1.3	—	μs

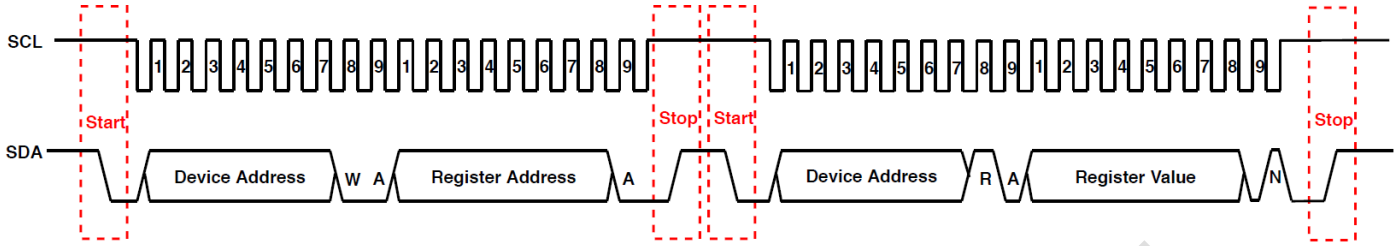
Note 1: f_{SCLK} is the $(t_{SCLK})^{-1}$.



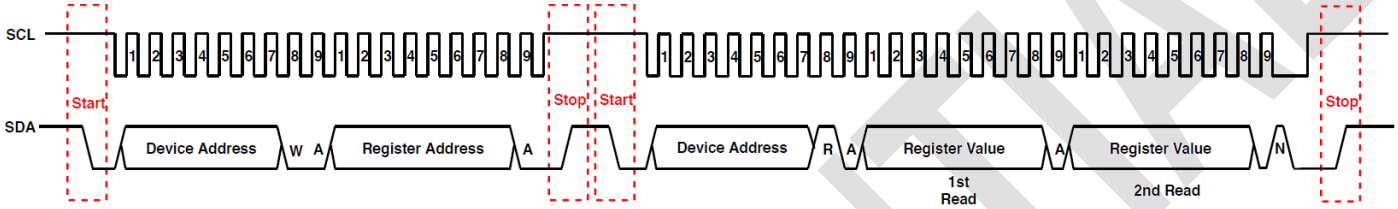
Timing Chart of the SDA and SCL



Write Command



Read Data



Sequential Read Data

6. FUNCTION DESCRIPTION

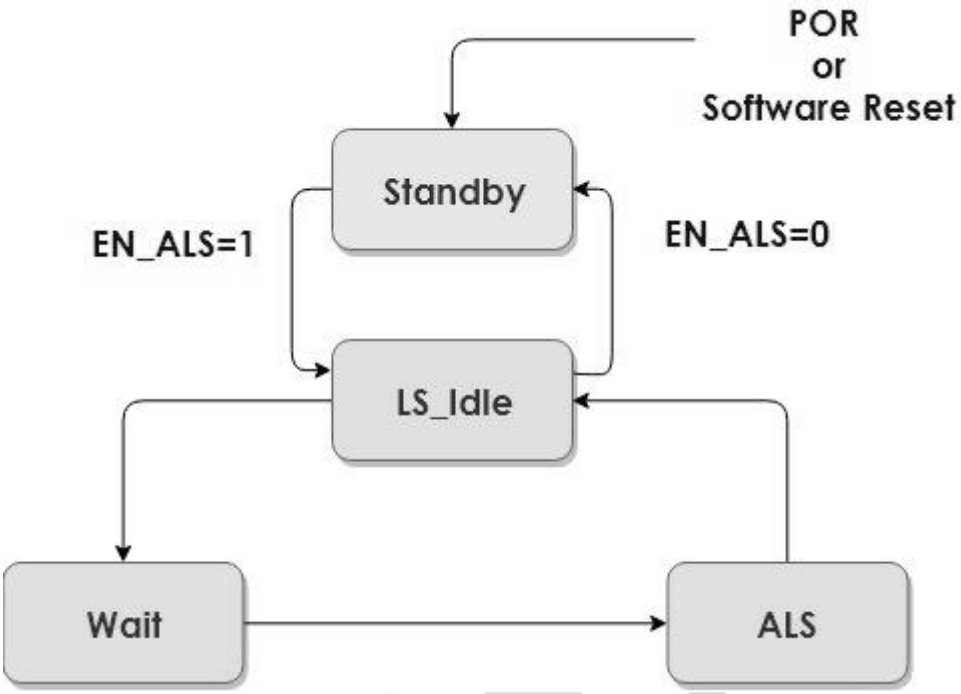
6.1 Digital Interface

STK31862 contains eight-bit registers accessed via the I²C bus. All operations can be controlled by the command register. The simple command structure makes user easy to program the operation setting and latch the output data from STK31862. Section 5.2 Timing chart displays the STK31862 I²C command format for reading and writing operation between host and STK31862.

STK31862 provides fixed I²C slave address using 7 bit addressing protocol.

Slave Address	R/W Command Bit	OPERATION
0x45 (followed by the R/W bit)	0	Write Command to STK31862
	1	Read Data from STK31862

6.2 System Operation



6.3 ALS Operation

6.3.1 ALS General Operation

The related ALS control bits are summarized below.

ALS Control Bits

General Control	
EN_ALS	Enable ALS sensing function
IT_ALS_SEL	Select ALS integration time
IT_ALS[3:0]	ALS long integration time
IT2_ALS[4:0]	ALS short integration time
PRST_ALS[1:0]	ALS persistence number
GAIN_ALS[1:0]	ALS channel gain control
GAIN_C[1:0]	C channel gain control
GAIN_ALS_DX128	ALS gain control specially for 128x
GAIN_C_DX128	C gain control specially for 128x
ALS Interrupt Control	
EN_ALS_INT	Enable ALS function interrupt
EN_ALS_DR_INT	Enable ALS data ready interrupt
THDH_ALS[15:0]	ALS out-of-windows high threshold
THDL_ALS[15:0]	ALS out-of-windows low threshold

ALS Data/Status Bits

Data	
DATA_ALS[15:0]	16-bits ALS channel raw data
DATA_C[15:0]	16-bits C channel raw data

Status	
FLG_ALS_DR	Indicate the ALS data ready event
FLG_ALS_INT	Indicate the ALS channel out-of-windows event

STK31862 uses the coated photodiode array to measure the Lux of the incoming light and also an un-filtered clear photodiode array to improve the ALS sensing accuracy.

The ALS sensing function is enabled by the EN_ALS bit and the gain control bit GAIN_ALS[1:0], GAIN_ALS_DX128, and IT period IT_ALS[3:0] shall be set before the EN_ALS.

The FLG_ALS_DR bit shall be asserted every ADC conversion cycle complete and shall be cleared automatically after one of the DATA_ALS[15:0]/DATA_C[15:0] is be read out through I²C.

The ALS/C data are 16-bit output and are stored in two bytes register. Higher byte register must be read first than lower byte. Data reading word protection is implemented to make sure the conversion data within the same conversion cycle could be read correctly. When the higher byte register is read, the lower 8-bit data will be stored into a shadow register which is read by the following sequential read or another single read to the lower byte register.

6.3.2 ALS Interrupt Description

ALS Out-of-Windows Interrupt

STK31862 provides the ALS data out-of-windows interrupt. Once the EN_ALS_INT is set to 1, then the STK31862 shall issue an ALS interrupt and assert the FLG_ALS_INT bit if the ALS data DATA_ALS[15:0] are outside the user's programmed window defined by THDH_ALS[15:0] and THDL_ALS[15:0]. The FLG_ALS_INT shall be cleared by write the bit 0 and shall be reset to 0 if POR/SWRst or EN_ALS = 0. Clear the EN_ALS_INT will also clear the FLG_ALS_INT bit to 0.

ALS persistence numbers PRST_ALS[1:0] is used to avoid the false alarm of ALS out-of-windows event due to environment noise. If ALS persistence is set larger than 1, then the ALS out-of-windows interrupt will not be issued until continuous persistence numbers of ADC conversion results outside the defined windows.

ALS Data Ready Interrupt

STK31862 also provides the ALS data ready interrupt. Once the EN_ALS_DR_INT is set to 1, then the STK31862 shall issue an ALS data ready interrupt every ADC conversion cycle and assert the FLG_ALS_DR bit. The FLG_ALS_DR shall be cleared automatically after any one of the DATA_ALS/C[15:0] is be read out through I²C and shall be reset to 0 if POR/SWRst or EN_ALS = 0. Clear the EN_ALS_DR_INT will not influence the FLG_ALS_DR status.

6.4 Wait State Operation

6.4.1 Wait State General Operation

The related Wait control bits are summarized below.

Wait Control Bits

General Control	
EN_WAIT	Enable Wait state
WAIT[7:0]	Wait period

Wait state is used for power saving

7. CONTROL REGISTER MAP

ADDR	REG NAME	BIT								Default
		7	6	5	4	3	2	1	0	
0x00	STATE						EN_WAIT	EN_ALS		0x00
0x02	ALSCTRL1	PRST_ALS[1:0]		GAIN_ALS[1:0]		IT_ALS[3:0]				0x05
0x04	INTCTRL1					EN_ALS_INT				0x00
0x05	WAIT	WAIT[7:0]								0x00
0x0A	THDH1_ALS	THDH_ALS[15:8]								0xFF
0x0B	THDH2_ALS	THDH_ALS[7:0]								0xFF
0x0C	THDL1_ALS	THDL_ ALS[15:8]								0x00
0x0D	THDL2_ALS	THDL_ ALS[7:0]								0x00
0x10	FLAG	FLG_ALS_DR		FLG_ALS_INT			FLG_ALS_SAT			0x01
0x13	DATA1_ALS	DATA_ALS[15:8]								0x00
0x14	DATA2_ALS	DATA_ALS[7:0]								0x00
0x15	DATA1_C	DATA_C[15:8]								0x00
0x16	DATA2_C	DATA_C[7:0]								0x00
0x3E	PDT_ID	PDT_ID[7:0]								TBD
0x3F	Reserved	Reserved								
0x4E	GAINCTRL			GAIN_C[1:0]			GAIN_C_DX128	GAIN_ALS_DX128		0x00
0x60	FIFOCTRL1		FIFO_MODE[1:0]					FIFO_DATA_SEL1:0]		0x00
0x61	FIFO1_WM_LV							FIFO_WM_LV[9:8]		0x00
0x62	FIFO2_WM_LV	FIFO_WM_LV[7:0]								0x00
0x63	FIFOCTRL2						FIFO_OVR_EN	FIFO_WM_EN	FIFO_FULL_EN	0x00
0x64	FIFO_FCNT1							FIFO_FCNT[9:8]		0x00
0x65	FIFO_FCNT2	FIFO_FCNT[7:0]								0x00
0x66	FIFO_OUT	FIFO_OUT[7:0]								0x00
0x67	FIFO_FLAG	FLG_FIFO_OVR			FLG_FIFO_WM				FLG_FIFO_FULL	0x00
0x6F	ALSCTRL2	IT_ALS_SEL			IT2_ALS[4:0]					0x00
0x80	SOFT_RESET	Write any to soft reset								0x00
0xA1	PDCTRL1							ALS_PD	C_PD	0x1F
0xA5	INTCTRL2							EN_ALS_DR_INT		0x00
0xFF	FIFOCTRL3	FIFO_PAUSE								0x00

STATE Register (0x00)

Bit	7	6	5	4	3	2	1	0
ITEM						EN_WAIT	EN_ALS	
Access						R/W	R/W	
Default						0	0	

Bit	ITEM	Description
1	EN_ALS	Enable the ALS function. 0 : Disable 1 : Enable
2	EN_WAIT	Enable the Wait state. 0 : Disable 1 : Enable

ALSCTRL1 Register (0x02)

Bit	7	6	5	4	3	2	1	0
ITEM	PRST_ALS[1:0]		GAIN_ALS[1:0]		IT_ALS[3:0]			
Access	R/W		R/W		R/W			
Default	2'b00		2'b00		4'b0101			

Bit	ITEM	Description
3:0	IT_ALS[3:0]	ALS integration time. 4'b0000 : 3.125 ms 4'b0001 : 6.25 ms 4'b0010 : 12.5 ms 4'b0011 : 25 ms 4'b0100 : 50 ms 4'b0101 : 100 ms 4'b0110 : 200 ms 4'b0111 : 400 ms
5:4	GAIN_ALS[1:0]	ALS gain setting. GAIN_ALS[1:0] is used to control of the ALS channels signal gain. The C channel is controlled by GAIN_C[1:0]. 2'b00 : x 1 times 2'b01 : x 4 times 2'b10 : x 16 times 2'b11 : x 64 times
7:6	PRST_ALS[1:0]	ALS persistence setting. The ALS has an interrupt persistence filter. The persistence filter allows user to specify the number of consecutive out-of-windows ALS occurrences before an interrupt is triggered. 2'b00 : x 1 times 2'b01 : x 2 times 2'b10 : x 4 times 2'b11 : x 8 times

BIT[3:0]	REFRESH TIME	Multiple of Base Refresh Time	ALS channel Lux/LSB GAIN_ALS_DX128 =1'b1 (128x)
0000	3.125ms	x1	0.0448
0001	6.25ms	x2	0.0224
0010	12.5ms	x4	0.0112
0011	25ms	x8	0.0028
0100	50ms	x16	0.0014
0101	100ms	x32	0.0007
0110	200ms	x64	0.00035
0111	400ms	X128	0.000175

BIT[3:0]	REFRESH TIME	Multiple of Base Refresh Time	C channel Lux/LSB GAIN_C_DX128 =1'b1 (128x)
0000	3.125ms	x1	0.0064
0001	6.25ms	x2	0.0032
0010	12.5ms	x4	0.0016
0011	25ms	x8	0.0008
0100	50ms	x16	0.0004
0101	100ms	x32	0.0002
0110	200ms	x64	0.0001
0111	400ms	X128	0.00005

INTCTRL1 Register (0x04)

Bit	7	6	5	4	3	2	1	0
ITEM					EN_ALS_INT			
Access					R/W			
Default					0			

Bit	ITEM	Description
3	EN_ALS_INT	Enable the ALS out-of-windows interrupt. 0 : Disable 1 : Enable

WAIT Register (0x05)

Bit	7	6	5	4	3	2	1	0
ITEM	WAIT[7:0]							
Access	R/W							
Default	8'b00000000							

Bit	ITEM	Description
7:0	WAIT[7:0]	ALS wait state period. wait period = (WAIT[7:0] + 1) * 1.54 ms

THDH1_ALS Register (0x0A)

Bit	7	6	5	4	3	2	1	0
ITEM	THDH_ALS[15:8]							
Access	R/W							
Default	8'b11111111							

THDH2_ALS Register (0x0B)

Bit	7	6	5	4	3	2	1	0
ITEM	THDH_ALS[7:0]							
Access	R/W							
Default	8'b11111111							

THDL1_ALS Register (0x0C)

Bit	7	6	5	4	3	2	1	0
ITEM	THDL_ALS[15:8]							
Access	R/W							
Default	8'b00000000							

THDL2_ALS Register (0x0D)

Bit	7	6	5	4	3	2	1	0
ITEM	THDL_ALS[7:0]							
Access	R/W							
Default	8'b00000000							

Bit	ITEM	Description
15:0	THDH_ALS[15:0]	ALS high threshold.
15:0	THDL_ALS[15:0]	ALS low threshold.

FLAG Register (0x10)

Bit	7	6	5	4	3	2	1	0
ITEM	FLG_ALS_DR		FLG_ALS_INT			FLG_ALS_SAT		FLG_NF
Access	R/W		R/W			RO		RO
Default	0		0			0		1

Bit	ITEM	Description
2	FLG_ALS_SAT	Indicate the ALS channel circuit saturation. 0 : No ALS channel circuit saturation, the data is valid. 1 : ALS channel circuit saturation, the data is not valid.
5	FLG_ALS_INT	Indicate if interrupt event is related to ALS_INT. Write bit 0 to clear. 0 : No ALS_INT event 1 : ALS_INT event
7	FLG_ALS_DR	Indicate ALS data conversion complete. Automatically cleared after DATA_ALS[15:0] is read. 0: ALS data is not ready 1: ALS data is ready

DATA1_ALS Register (0x13)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_ALS[15:8]							
Access	RO							
Default	8'b00000000							

DATA2_ALS Register (0x14)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_ALS[7:0]							
Access	RO							
Default	8'b00000000							

DATA1_C Register (0x15)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_C[15:8]							
Access	RO							
Default	8'b00000000							

DATA2_C Register (0x16)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_C[7:0]							
Access	RO							
Default	8'b00000000							

The STK31862 has two 8-bit read-only registers to hold each data from ADC of ALS/C. The registers are updated for every ALS/C integration time (conversion cycle).

Product ID (0x3E)

Read Only; PDT_ID = Product ID(TBD) to indicate the product information.

Reserved (0x3F)

Read Only; RSRVD = Reserved for engineering mode.

GAINCTRL Register (0x4E)

Bit	7	6	5	4	3	2	1	0
ITEM			GAIN_C[1:0]			GAIN_C_DX128	GAIN_ALS_DX128	
Access			R/W			R/W	R/W	
Default			2'b00			0	0	

Bit	ITEM	Description
1	GAIN_ALS_DX128	GAIN_ALS_DX128 is used to control specially for ALS channel 128x gain.
2	GAIN_C_DX128	GAIN_C_DX128 is used to control specially for C channel 128x gain.
5:4	GAIN_C[1:0]	C channel gain setting. GAIN_C[1:0] is used to control of the C channel signal gain. 2'b00 — x 1 times 2'b01 — x 4 times 2'b10 — x 16 times 2'b11 — x 64 times

FIFOCTRL1 Register (0x60)

Bit	7	6	5	4	3	2	1	0
ITEM			FIFO_MODE[1:0]				FIFO_DATA_SEL[2:0]	
Access			R/W				R/W	
Default			2'b00				2'b00	

Bit	ITEM	Description
5:4	FIFO_MODE	00: Mode off 01: Bypass mode 10: FIFO mode 11: Stream mode
1:0	FIFO_DATA_SEL	00: ALS only mode 01: C only mode 10: ALS + C mode

FIFO1_WM_LV Register (0x61)

Bit	7	6	5	4	3	2	1	0
ITEM							FIFO_WM_LV[9:8]	
Access							R/W	
Default							2'b00	

FIFO2_WM_LV Register (0x62)

Bit	7	6	5	4	3	2	1	0
ITEM	FIFO_WM_LV[7:0]							
Access	R/W							
Default	8'b00000000							

Bit	ITEM	Description
9:0	FIFO_WM_LV	FIFO watermark level 0: Disable Others: FIFO watermark interrupt issued if data amount eq to FIFO_WM_LV setting

FIFOCTRL2 Register (0x63)

Bit	7	6	5	4	3	2	1	0
ITEM						FIFO_OVR_EN	FIFO_THD_EN	FIFO_FULL_EN
Access						R/W	R/W	R/W
Default						0	0	0

Bit	ITEM	Description
0	FFULL_EN	Enable FIFO full interrupt
1	FWM_EN	Enable FIFO water mark interrupt
2	FOVR_EN	Enable FIFO overflow interrupt

FIFO_FCNT1 Register (0x64)

Bit	7	6	5	4	3	2	1	0
ITEM							FIFO_FCNT[9:8]	
Access							R	
Default							2'b00	

FIFO_FCNT2 Register (0x65)

Bit	7	6	5	4	3	2	1	0
ITEM	FIFO_FCNT[7:0]							
Access	R							
Default	8'b00000000							

Bit	ITEM	Description
10:0	FIFO_FCNT	Indicate FIFO frame count if FIFO is enabled.

FIFO_OUT Register (0x66)

Bit	7	6	5	4	3	2	1	0
ITEM	FIFO_OUT[7:0]							
Access	R							
Default	8'b00000000							

Bit	ITEM	Description
7:0	FIFO_OUT	FIFO output data

FIFO_FLAG Register (0x67)

Bit	7	6	5	4	3	2	1	0
ITEM	FLG_FIFO_OVR			FLG_FIFO_WM				FLG_FIFO_FULL
Access	R			R				R
Default	0			0				0

Bit	ITEM	Description
0	FLG_FIFO_FULL	Indicate if FIFO_FCNT is full in FIFO mode. Read FIFO_OUT to clear. 0 : No FLG_FIFO_FULL event 1 : FLG_FIFO_FULL event
4	FLG_FIFO_WM	Indicate if FIFO_FCNT is equal FIFO_WM_LV in FIFO/Stream mode. Read FIFO_OUT to clear. 0 : No FLG_FIFO_WM event 1 : FLG_FIFO_WM event
7	FLG_FIFO_OVR	Indicate if FIFO_FCNT is overflow in Stream mode. Read FIFO_OUT to clear. 0 : No FLG_FIFO_ OVR event 1 : FLG_FIFO_ OVR event

ALSCTRL2 Register (0x6F)

Bit	7	6	5	4	3	2	1	0
ITEM	IT_ALS_SEL			IT2_ALS[4:0]				
Access	R/W			R/W				
Default	0			5'b00000				

Bit	ITEM	Description
4:0	IT_ALS2[4:0]	ALS short integration time. Enable by REG_IT_ALS_SEL = 1 5'b00000 192 us 5'b00001 288 us 5'b00010 384 us 5'b0011 480 us ... ... 5'b10010 1920 us 5'b10011 2016 us 5'b10100 2112 us
7	IT_ALS_SEL	0: Use IT_ALS[3:0] to define ALS long integration time. 1: Use IT2_ALS[4:0] to define ALS short integration time.

Soft reset (0x80)

Write any data to this register will reset the chip.

PDCTRL1 Register (0xA1)

Bit	7	6	5	4	3	2	1	0
ITEM							ALS	C
Access							R/W	R/W
Default							1	1

Bit	ITEM	Description
0	ALS_C	Enable the C PD . 0 : Disable 1 : Enable
1	ALS_ALS	Enable the ALS PD . 0 : Disable 1 : Enable

INTCTRL2 Register (0xA5)

Bit	7	6	5	4	3	2	1	0
ITEM							EN_ALS_DR_INT	
Access							R/W	
Default							0	

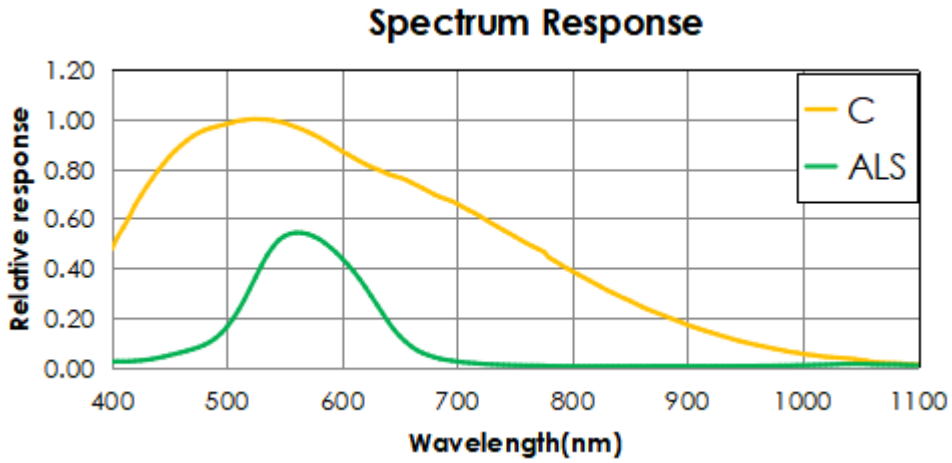
Bit	ITEM	Description
1	EN_ALS_DR_INT	Enable the ALS Data Ready interrupt. 0 : Disable 1 : Enable

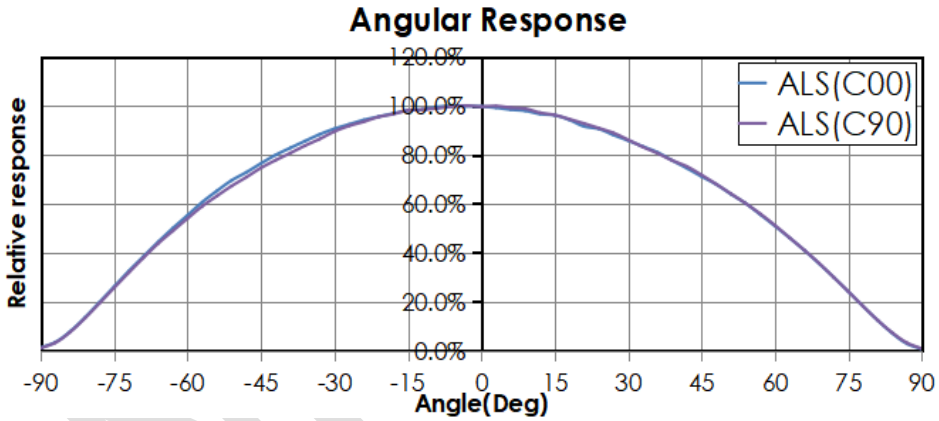
FIFOCTRL3 Register (0xFF)

Bit	7	6	5	4	3	2	1	0
ITEM	FIFO_PAUSE							
Access	R/W							
Default	0							

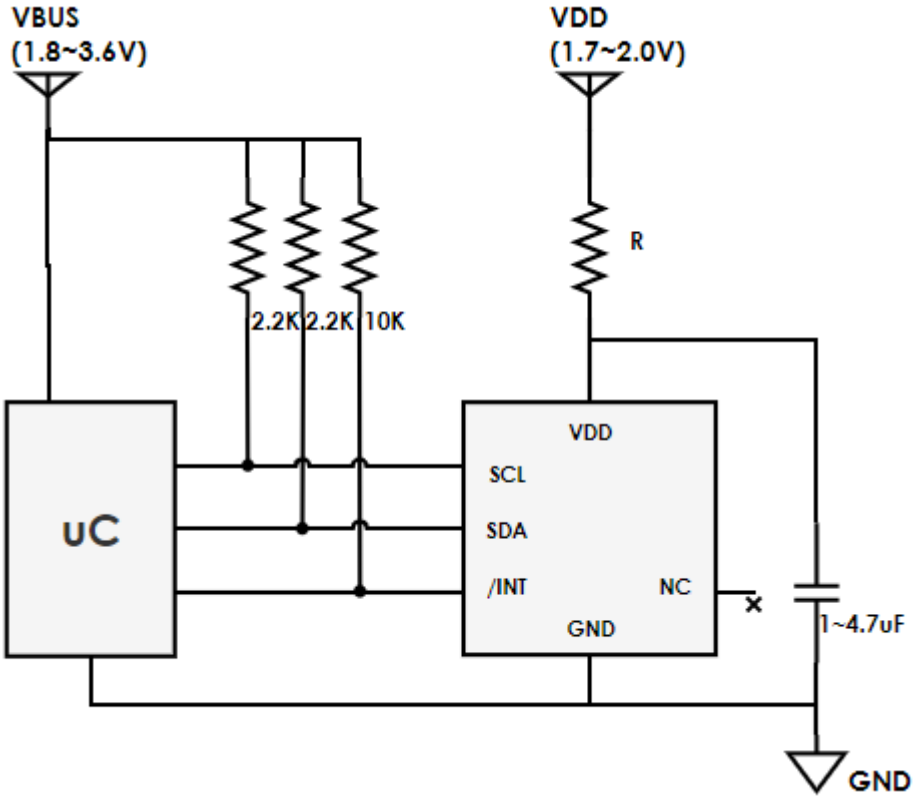
Bit	ITEM	Description
7	FIFO_PAUSE	Enable FIFO Pause. 0 : Run 1 : Pause

8. ALS RESPONSE CHARTS





9. APPLICATION NOTE



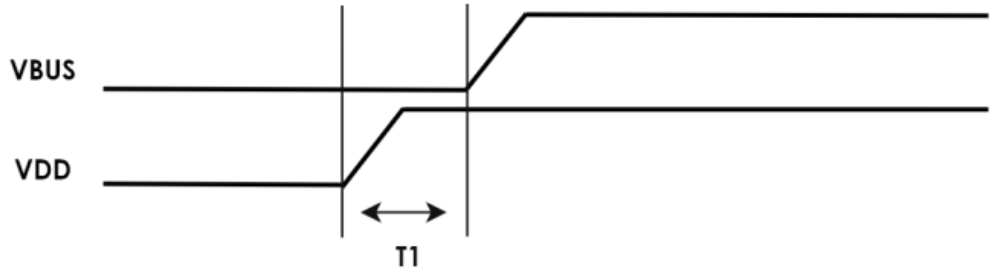
STK31862 Typical Application Circuit with Independent VDD Supply Voltage

9.1 Power Noise Consideration

It is suggested that IC power to get the best performance of STK31862 and an R/C low pass filter is also suggested to be added in the V_{DD} path of STK31862 to reduce the switching noise from whole system. The recommended R value is 22 Ohm.

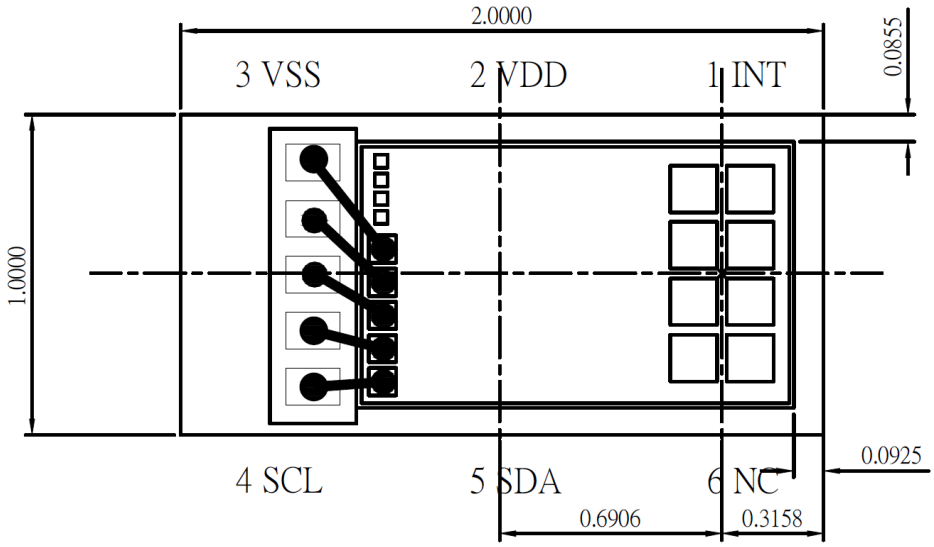
9.2 Power ON Sequence

The **T1** is must > 30ms (VDD is recommended first).
VDD variation peak=100mV (+/-50mV).

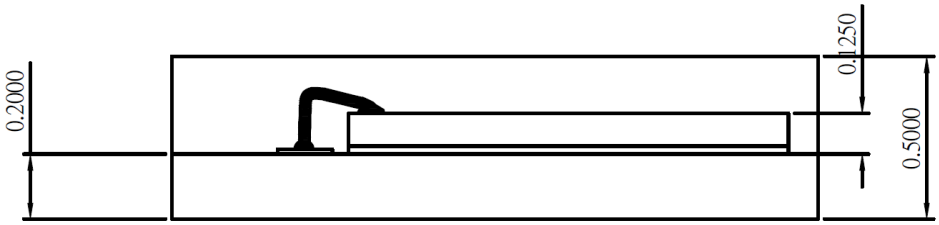


10. PACKAGE OUTLINE

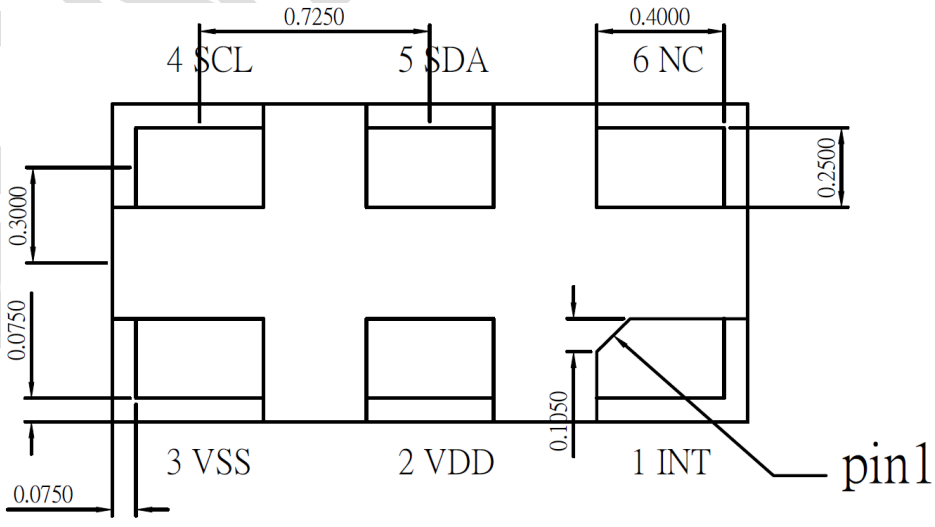
STK31862
Top View



Side View



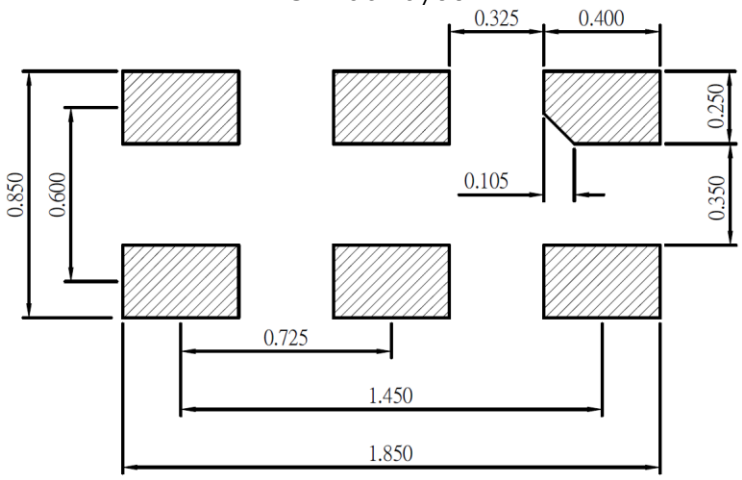
Bottom View



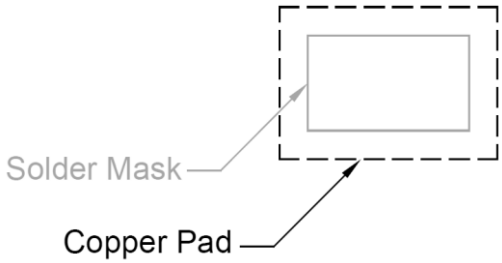
PCB Pad Layout and Solder Mask Define Recommendation

Suggested PCB pad layout guidelines are shown below.

PCB Pad Layout



Solder Mask Define

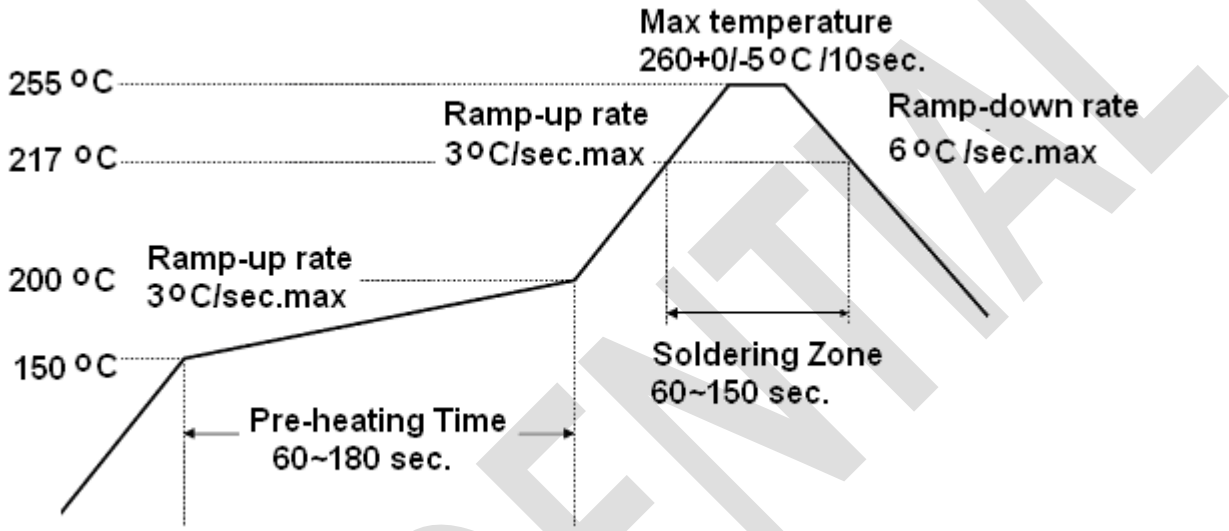


Notes: all linear dimensions are in mm.

11. SOLDERING INFORMATION

11.1 Soldering Condition

0. Pb-free solder temperature profile



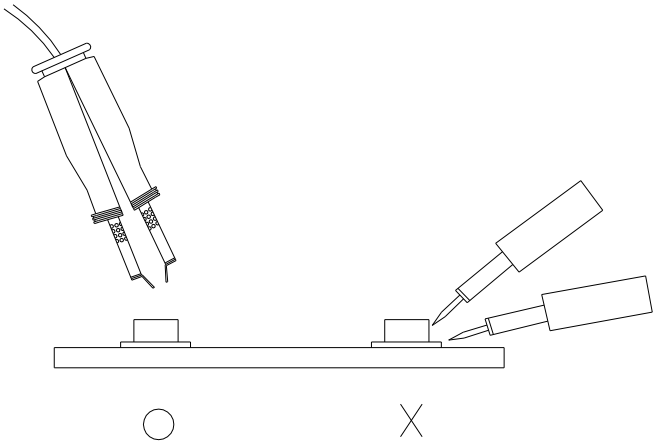
2. Reflow soldering should not be done more than three times.
3. When soldering, do not put stress on the Ics during heating.
4. After soldering, do not warp the circuit board.

11.2 Soldering Iron

Each terminal is to go to the tip of soldering iron temperature less than 350°C for 3 seconds within once in less than the soldering iron capacity 25W. Leave two seconds and more intervals, and do soldering of each terminal. Be careful because the damage of the product is often started at the time of the hand solder.

11.3 Repairing

Repair should not be done after the Ics have been soldered. When repairing is unavoidable, a double-head soldering iron should be used (as below figure). It should be confirmed beforehand whether the characteristics of the Ics will or will not be damaged by repairing.



12. STORAGE INFORMATION

12.1 Storage Condition

1. Devices are packed in moisture barrier bags (MBB) to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.
2. The delivery product should be stored with the conditions shown below:

Storage Temperature	-40 to 85℃
Relatively Humidity	below 60%RH

12.2 Treatment After Unsealed

1. Floor life (time between soldering and removing from MBB) must not exceed the time shown below:

Floor Life	168 Hours
Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

2. When the floor life limits have been exceeded or the devices are not stored in dry conditions, they must be re-baked before reflow to prevent damage to the devices. The recommended conditions are shown below

Temperature	60℃
Re-Baking Time	12 Hours

13. TAPE AND REEL DIMENSION

TBD

Notes: all linear dimensions are in mm.

Revision History

Date	Version	Modified Items
2020/12/30	0.9.1	Initial release.
2021/02/23	0.9.2	Modify Pin description.
2021/03/23	0.9.3	1.Modify FIFO1_WM_LV Register 2. FIFO_FCNT1 Register
2021/10/20	0.9.4	1. Modify the Register 0x61/0x63/0x64/0x67 description. 2. Modify the Register 0x63/0x67 description.

