W1160

Ambient Light Sensor with I2C interface

Preliminary Datasheet

Version – 0.9.1

Hazardous Substance Free
RoHS / REACH Compliant

Sensortek Technology Corporation

1. OVERVIEW

Description

The W1160 is an integrated ambient light to digital converter with I²C interface. This device provides ambient light sensing to allow robust backlight/display brightness control.

For ambient light sensing, the W1160 incorporates a photodiode, timing controller and ADC in a single chip. The excellent spectral response is designed to be close-to human eye. The W1160 is suitable for detecting a wide range of light intensity environment.

Software shutdown mode control is provided for power saving application. The W1160 operating voltage range is 1.7V to 2.0V.

Feature

- Convert ambient light intensity to 16-bit or 12-bit digital data format
- Ambient light sensor which closes to human-eye response and suppress IR portion
- Flexible timing settings
  - Sample time: total 32763 steps sample time and each step 100us
    600us /..... /3276.7ms / 3276.8ms
  - integration time: total 4096 steps IT and each step 99us
    99us / 198us /..... / 405.405ms / 405.504ms
- Flicker reduction
- Wide dynamic range
- Full-range auto-gain control
- FIFO buffer size of 512 bytes
  - Bypass mode
  - FIFO mode
  - Stream mode

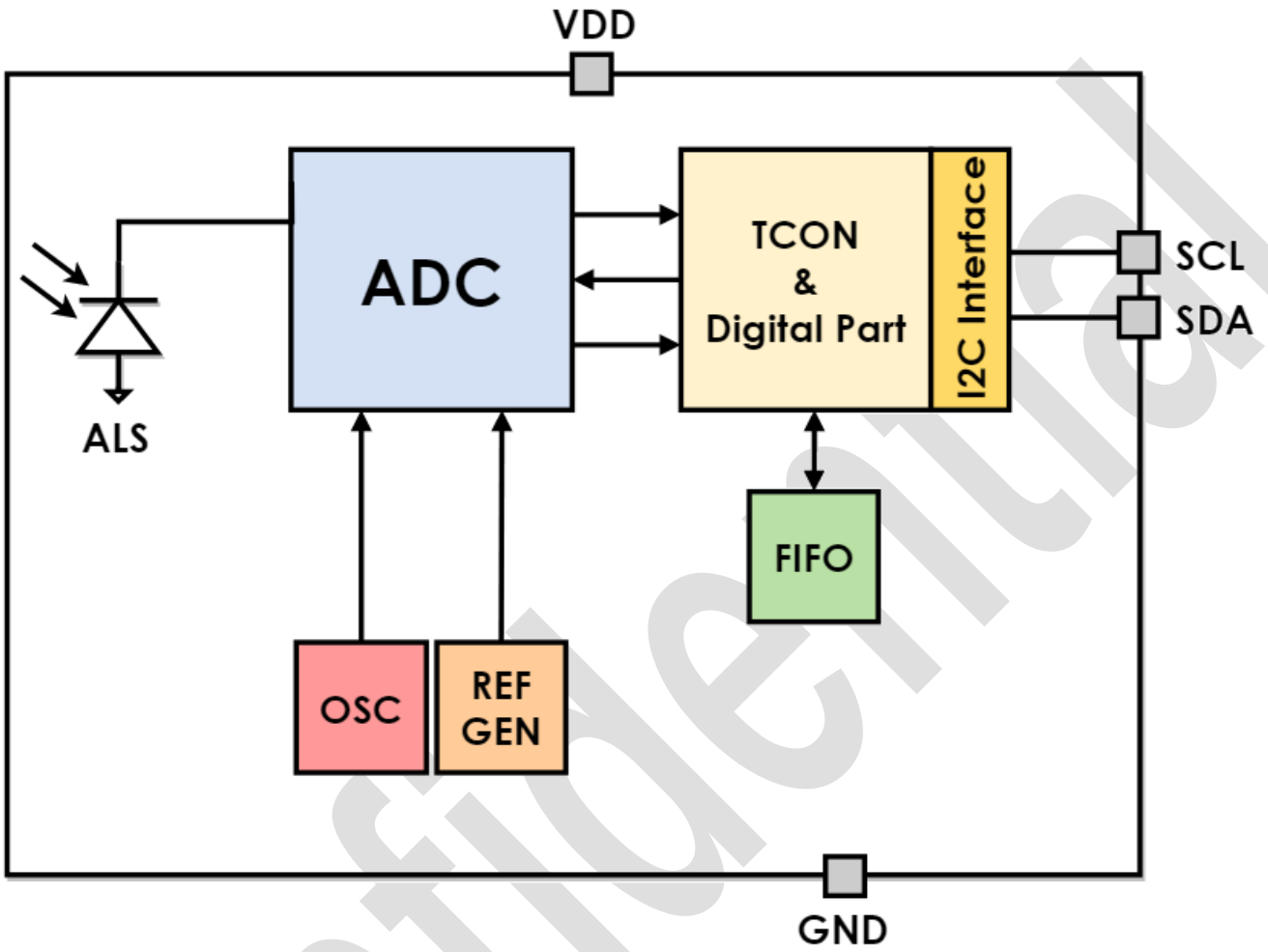
General

- Fully digital control with I²C interface
  - 1.2 ~ 3.6V I²C interface
  - Support Standard Mode, Fast Mode, and Fast Mode Plus (1 MHz)
- Low power design
- V_{DD} wide operation voltage: 1.7 ~ 2.0V
- Excellent temperature compensation: -40 to 85°C
- WLCSP package: 1.1645 x 1.1645 x 0.206 (mm)
- Lead-free package (RoHS compliant)

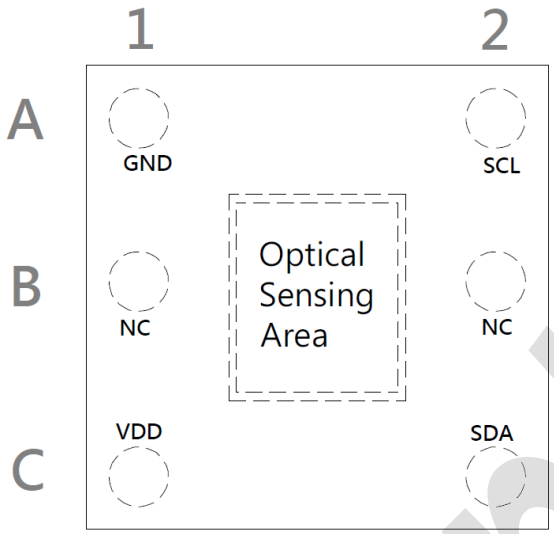
Applications

- Smart Watches
- Smart Bands
- Wearable Devices
- Tablets
- Display Backlight Controls
- IoT Devices

2. FUNCTION BLOCK



3. PINOUT DIAGRAM



Top View

4. PIN DESCRIPTION

Pin No.	Pin Name	Direction	Pin Function
A1	GND	GND	Ground.
B1	NC	I	No connect.
C1	VDD	PWR	Power supply: 1.7V to 2.0V.
A2	SCL	I	I²C serial clock line. Require pull-up resistor.
B2	NC	I	No connect.
C2	SDA	B	I²C serial data line. Require pull-up resistor. (Open Drain)

Direction denotation:

Direction	denotation	Direction	denotation
GND	Ground	B	Bi-direction
I	Input	PWR	Power

5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply voltage	-0.3	2.15	V
Ta	Operation temperature	-40	85	°C

NOTE: All voltages are measured with respect to GND

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply voltage	1.7	2.0	V
f_{I2C}	Clock frequency of I²C	—	1000	kHz
Ta	Operation temperature	-40	85	°C

NOTE: All voltages are measured with respect to GND

Symbol	Parameter	Max.	Unit
ESD	Electrostatic discharge protection	2 (HBM)	kV
		200 (MM)	V
		100 (Latch Up)	mA

NOTE: All voltages are measured with respect to GND

5.1 Electrical and Optical Characteristics

V_{DD} = 1.8V, under room temperature 25°C (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Operation Characteristics						
I_{ALS-1}	ALS only supply current	Note1		145		μA
I_{ALS-2}	ALS only supply current	Note2,13	—	7		μA
I_{ALS-3}	ALS only supply current	Note3	—	4.5		μA
I_{SD}	Shutdown current	Note4	—	1.5		μA
V_{IH}	Logic high, I²C	Note7,9	0.9		V_{DD}	V
V_{IL}	Logic low, I²C	Note8	—		0.4	V
ALS Characteristics						
λp_1	Peak sensitivity wavelength for ALS			550		nm
ALS_{FSCNT1}	Full scale ALS counts	Note10			65535	counts
ALS_{FSCNT2}	Full scale ALS counts	Note11			4095	counts
ALS_{DARK}	ALS dark offset	Note4,6	0		3	counts
ALS_{SENSE}	ALS sensitivity	Note2,13		2330		counts
ALS_{TOLER}	ALS sensitivity tolerance	Note2,5	-12.5		+12.5	%
Full-scale illuminance	Max lux	Note12		80		Klux

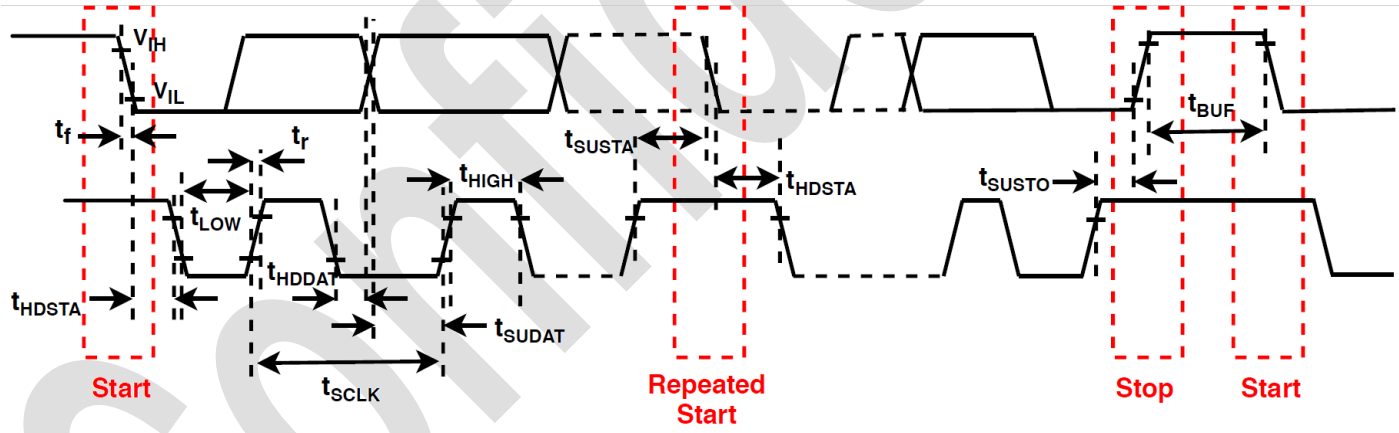
Note 1: Operation. IT_ALS_SLOW [11:0] = 12'h3FF (101.376ms), FIFO_CLKEN=0 and FIFO_PWREN=0.
Note 2: Operation. GAIN_LEVEL [3:0] = 4'b1001 (LV9), SAMPLE_TIME_SLOW [14:0] = 15'h12BF (480ms) and IT_ALS_SLOW [11:0] = 12'h0A9 (16.830ms), FIFO_CLKEN=0 and FIFO_PWREN=0.
Note 3: A light operating at a light source frequency of 120Hz. SAMPLE_TIME_SLOW [14:0] = 15'h03FF (102.4ms) and IT_ALS_SLOW [11:0] = 12'h00A (1.089ms), EN_FLK_REDUCTION=1, SAMPLE_TIME_FLK [10:0] =11'h029 (4.2ms), FIFO_CLKEN=0 and FIFO_PWREN=0.
Note 4: GAIN_LEVEL [3:0] = 4'b1100 (LV12), IT_ALS_SLOW [11:0] = 12'h0A9(16.830ms).
Note 5: White LED parallel light source.
Note 6: $E_{ambient}$ = 0 Lux.
Note 7: I²C logical high voltage level is specified as worst-case condition when all the recommended operation supply voltages (V_{DD}) are taken into consideration. The logical high level is different when different supply voltage is applied.
Note 8: I²C logical low voltage level is specified as worst-case condition when all the recommended operation supply voltages (V_{DD}) are taken into consideration. The logical low level is different when different supply voltage is applied.
Note 9: If $VDD_{I/O}$ =1.2V, VIH (min.) =0.9V.
Note 10: 16-bit digital data format.
Note 11: 12-bit digital data format.
Note 12: 16-bit digital data format, GAIN_LEVEL [3:0] = 4'b0000 (LV0) and IT_ALS_SLOW [11:0] = 12'h0A9(16.830ms) under the LED bulb (color temperature 6500K).
Note 13: 100lux under White LED parallel light source.

5.2 Timing Chart

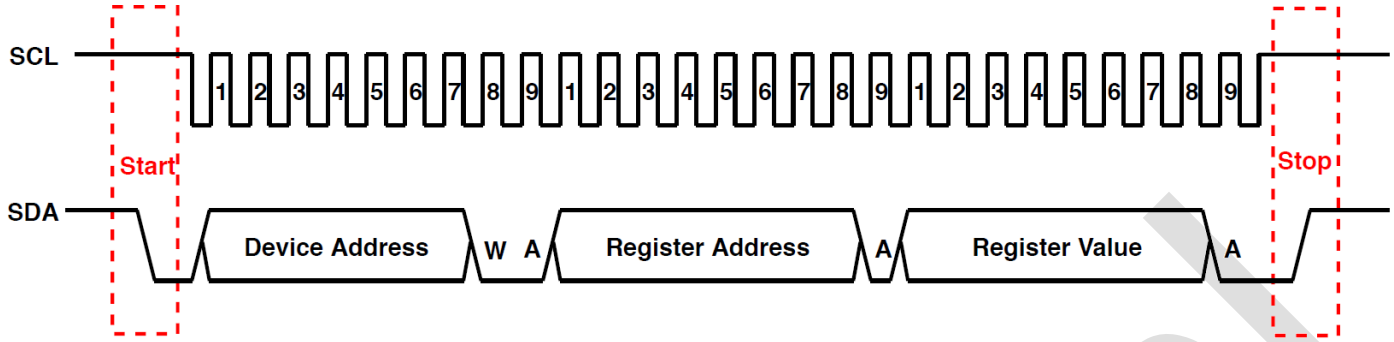
Characteristics of the SDA and SCL I/O

Symbol	Parameter	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCLK}	SCL clock frequency	10	100	10	400	10	1000	KHz
t_{HDSTA}	Hold time after (repeated) start condition. After this period, the first clock is generated	4.0	—	0.6	—	0.26	—	μs
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	0.5	—	μs
t_{HIGH}	HIGH period of the SCL clock	4.0	—	0.6	—	0.26	——	μs
t_{SUSTA}	Set-up time for a repeated START condition	4.7	—	0.6	—	0.26	—	μs
t_{HDDAT}	Data hold time	0	—	0	—	0	—	ns
t_{SUDAT}	Data set-up time	250	—	100	—	50	—	ns
t_r	Rise time of both SDA and SCL signals	—	1000	—	300	—	120	ns
t_f	Fall time of both SDA and SCL signals	—	300	—	300	—	120	ns
t_{SUSTO}	Set-up time for STOP condition	4.0	—	0.6	—	0.26	—	μs
t_{BUF}	Bus free time between a STOP and START condition	4.7	—	1.3	—	0.5	—	μs

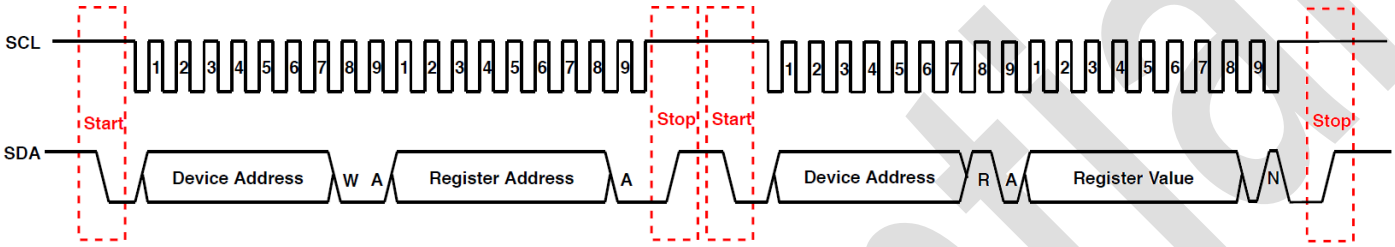
Note 1: f_{SCLK} is the $(t_{SCLK})^{-1}$.



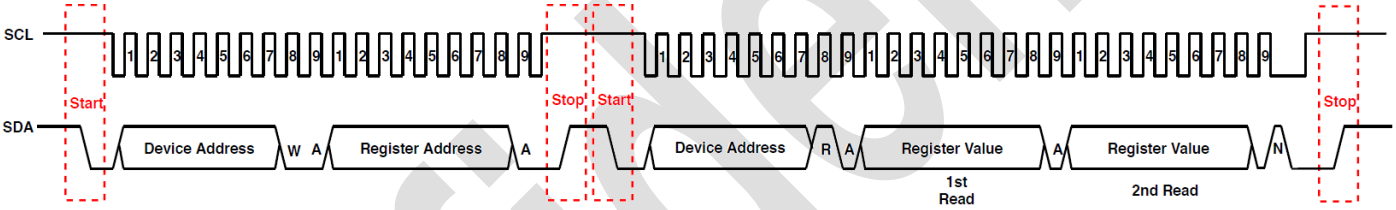
Timing Chart of the SDA and SCL



Write Command



Read Data



Sequential Read Data

6. FUNCTION DESCRIPTION

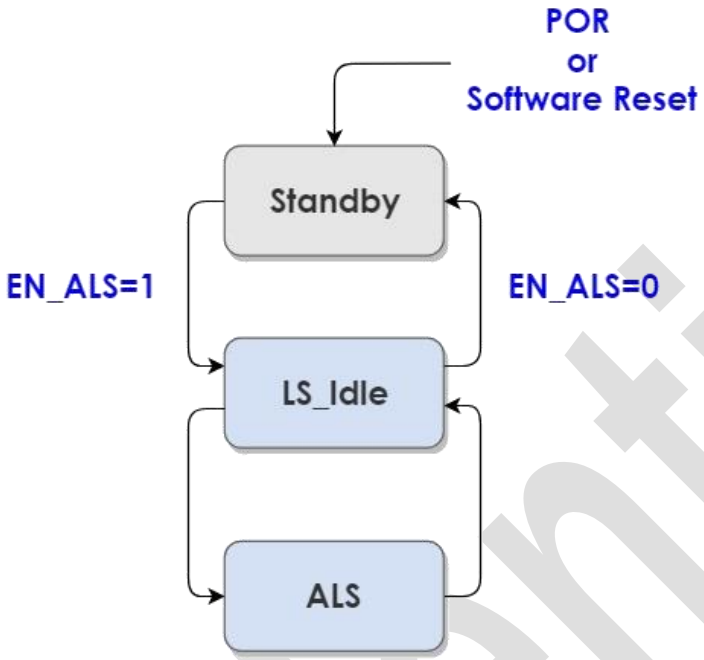
6.1 Digital Interface

W1160 contains eight-bit registers accessed via the I²C bus. All operations can be controlled by the command register. The simple command structure makes user easy to program the operation setting and latch the output data from W1160. Section 5.2 Timing chart displays the W1160 I²C command format for reading and writing operation between host and W1160.

W1160 provides fixed I²C slave address using 7 bit addressing protocol.

Slave Address	R/W Command Bit	OPERATION
0x48 (Followed by the R/W bit)	0	Write Command to W1160
	1	Read Data from W1160

6.2 System Operation



6.3 ALS Operation

6.3.1 ALS General Operation

The related ALS control bits are summarized below.

ALS Control Bits

General Control	
EN_ALS	Enable ALS sensing function
IT_ALS_SLOW [11:0]	Slow mode ALS integration time
SAMPLE_TIME_SLOW [14:0]	Slow mode ALS sample time
MANUNAL_GAIN_MODE	Enable MANUNAL_GAIN_MODE
GAIN_LEVEL [3:0]	ALS Gain Setting

ALS Data/Status Bits

Data	
DATA_ALS [15:0]	16-bits ALS channel raw data
Status	
FLG_ALS_DR	Indicate the ALS data ready event

7. CONTROL REGISTER MAP

ADDR	REG NAME	BIT								Default
		7	6	5	4	3	2	1	0	
0x00	STATE							EN_ALS		0x00
0x02	IT_FAST1					IT_ALS_FAST [11:8]				0x03
0x03	IT_FAST2	IT_ALS_FAST [7:0]								0xFF
0x05	SAMPLE_FAST1		SAMPLE_TIME_FAST [14:8]							0x00
0x06	SAMPLE_FAST2	SAMPLE_TIME_FAST [7:0]								0x00
0x07	SAMPLE_SLOW1		SAMPLE_TIME_SLOW [14:8]							0x00
0x08	SAMPLE_SLOW2	SAMPLE_TIME_SLOW [7:0]								0x00
0x10	FLAG1	FLG_ALS_DR					FLG_ALS_SAT			0x00
0x13	DATA1_ALS	DATA_ALS [15:8]								0x00
0x14	DATA2_ALS	DATA_ALS [7:0]								0x00
0x17	DATA_GC	GAIN LEVEL [3:0]								0x00
0x3D	Power Mode				EN_FLK_REDUCTION				ALS_POWER_MODE	0x00
0x3E	PDT_ID	PDT_ID [7:0]								0xE5
0x3F	Reserved	Reserved								0x00
0x4E	SAMPLE_FLK1						SAMPLE_TIME_FLK [10:8]			0x00
0x4F	SAMPLE_FLK2	SAMPLE_TIME_FLK [7:0]								0x00
0x5F	FSM_RESTART								FSM_RESTART	0x00
0x60	FIFOCTRL1	FIFO_MULTI_I2C_RD		FIFO_MODE [1:0]			FIFO_DATA_SEL [1:0]			0x00
0x61	FIFO1_WM_LV				FIFO_LENGTH_CONFIG				FIFO_WM_LV [8]	0x00
0x62	FIFO2_WM_LV	FIFO_WM_LV [7:0]								0x00
0x63	FIFOCTRL2				FIFO_PAUSE		FIFO_OVR_EN	FIFO_WM_EN	FIFO_FULL_EN	0x00
0x64	FIFO_FCNT1								FIFO_FRAME_CNT [8]	0x00
0x65	FIFO_FCNT2	FIFO_FRAME_CNT [7:0]								0x00
0x66	FIFO_OUT	FIFO_OUT [7:0]								0x00
0x67	FIFO_FLAG	FLG_FIFO_OVR			FLG_FIFO_WM				FLG_FIFO_FULL	0x00
0x68	FIFOCTRL3								FIFO_FLUSH	0x00
0x69	FIFOCTRL4			FIFO_CLKEN	FIFO_PWREN					0x00

0x6A	AGCCTRL1	EN_ALS_AUTO GAIN				PRST_AGC [1:0]		AGC_HIGH_HYST	AGC_LOW_HYST	**0x00**
0x6B	MANUAL_GAIN_CTRL								MANUA_GAIN_MODE	**0x00**
0x6C	AGCCTRL2					AGC_12B_MODE	AGC_SEL_MODE			**0x00**
0x6D	THD_SAT_GC				TH_ALS_SAT_GC [4:0]					**0x10**
0x6E	IT_SLOW1					IT_ALS_SLOW [11:8]				**0x03**
0x6F	IT_SLOW2	IT_ALS_SLOW [7:0]								**0xFF**
0x80	SOFT_RESET	Write any to soft reset								**0x00**
0xA4	ALSCTRL						DATA_FORMAT_SEL	ALS_SAT_EN		**0x03**

STATE Register (0x00)

Bit	7	6	5	4	3	2	1	0
ITEM							EN_ALS	
Access							R/W	
Default							0	

Bit	ITEM	Description
1	EN_ALS	Disable/Enable the ALS function. 0: Disable 1: Enable

IT_FAST1 Register (0x02)

Bit	7	6	5	4	3	2	1	0
ITEM					IT_ALS_FAST [11:8]			
Access					R/W			
Default					4'b0000			

IT_FAST2 Register (0x03)

Bit	7	6	5	4	3	2	1	0
ITEM	IT_ALS_FAST [7:0]							
Access	R/W							
Default	8'b00000000							

Bit	ITEM	Description
11:0	IT_ALS_FAST [11:0]	ALS_FAST integration time setting(99us/step). 12'h000: 99us 12'h001: 198us ⋮ 12'h3FF: 101.376ms ⋮ 12'hFFF: 405.504ms

SAMPLE_FAST1 Register (0x05)

Bit	7	6	5	4	3	2	1	0
ITEM		SAMPLE_TIME_FAST [14:8]						
Access		R/W						
Default		7'b0000000						

SAMPLE_FAST2 Register (0x06)

Bit	7	6	5	4	3	2	1	0
ITEM	SAMPLE_TIME_FAST [7:0]							
Access	R/W							
Default	8'b00000000							

Bit	ITEM	Description
14:0	SAMPLE_TIME_ FAST [14:0]	FAST mode sample time setting. Sample period = (SAMPLE_TIME_FAST [14:0] + 1) * 100us 15'h005: 600us 15'h006: 700us ⋮ ⋮ 15'h3FF: 102.4ms ⋮ ⋮ 15'h7FFF: 3276.8ms *Set SAMPLE_TIME_FAST must over than IT_ALS_FAST 500us.

SAMPLE_SLOW1 Register (0x07)

Bit	7	6	5	4	3	2	1	0
ITEM		SAMPLE_TIME_SLOW [14:8]						
Access		R/W						
Default		7'b0000000						

SAMPLE_SLOW2 Register (0x08)

Bit	7	6	5	4	3	2	1	0
ITEM	SAMPLE_TIME_SLOW [7:0]							
Access	R/W							
Default	8'b00000000							

Bit	ITEM	Description
14:0	SAMPLE_TIME_ SLOW [14:0]	SLOW mode sample time setting. Sample period = (SAMPLE_TIME_SLOW [14:0] + 1) * 100us 15'h005: 600us 15'h006: 700us ⋮ ⋮ 15'h3FF: 102.4ms ⋮ ⋮ 15'h7FFF: 3276.8ms *Set SAMPLE_TIME_SLOW must over than IT_ALS_SLOW 500us.

FLAG1 Register (0x10)

Bit	7	6	5	4	3	2	1	0
ITEM	FLG_ALS_DR					FLG_ALS_SAT		
Access	R					R		
Default	0					0		

Bit	ITEM	Description
2	FLG_ALS_SAT	Indicate the ALS channel circuit saturation. 0: No ALS channel circuit saturation, the data is valid. 1: ALS channel circuit saturation, the data is not valid.
7	FLG_ALS_DR	Indicate ALS data conversion complete. Automatically cleared after DATA_ALS [15:0] is read. 0: ALS data is unready 1: ALS data is ready

DATA1_ALS Register (0x13)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_ALS [15:8]							
Access	R							
Default	8'b00000000							

DATA2_ALS Register (0x14)

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_ALS [7:0]							
Access	R							
Default	8'b00000000							

The W1160 has two 8-bit read-only registers to hold each data from ADC of ALS. The registers are updated for every ALS integration time (conversion cycle).

DATA_GC Register (0x17)

Bit	7	6	5	4	3	2	1	0
ITEM	GAIN_LEVEL [3:0]							
Access	R/W							
Default	4'b0000							

Bit	ITEM	Description
7:4	GAIN_LEVEL [3:0]	Indicate the latest ALS gain level. 4'b1111: LV15(4096) 4'b1110: LV14(2048) 4'b1101: LV13(1024) 4'b1100: LV12(512)

		4'b1011: LV11(256) 4'b1010: LV10(64) 4'b1001: LV9(16) 4'b1000: LV8(4) 4'b0111: LV7(2) 4'b0110: LV6(1) 4'b0101: LV5(0.5) 4'b0100: LV4(0.25) 4'b0011: LV3(0.125) 4'b0010: LV2(0.0625) 4'b0001: LV1(0.015625) 4'b0000: LV0(0.003906)

Power Mode (0x3D)

Bit	7	6	5	4	3	2	1	0
ITEM				EN_FLK_REDUCTION				ALS_POWER_MODE
Access				R/W				R/W
Default				0				0

Bit	ITEM	Description
0	ALS POWER MODE	Select ALS Power Mode 0: Slow mode 1: Fast mode
4	EN_FLK_REDUCTION	Disable/Enable Flicker reduction function 0: Disable 1: Enable

Product ID (0x3E)

Read Only; PDT_ID = Product ID(0xE5) to indicate the product information.

Reserved (0x3F)

Read Only; RSRVD = Reserved for engineering mode.

SAMPLE_FLK1 Register (0x4E)

Bit	7	6	5	4	3	2	1	0
ITEM						SAMPLE_TIME_FLK [10:8]		
Access						R/W		
Default						3'b000		

SAMPLE_FLK2 Register (0x4F)

Bit	7	6	5	4	3	2	1	0
ITEM	SAMPLE_TIME_FLK [7:0]							
Access	R/W							
Default	8'b00000000							

Bit	ITEM	Description
10:0	SAMPLE_TIME_FLK [10:0]	FLICKER reduction mode sample time setting. Flicker period = (SAMPLE_TIME_FLK [10:0] + 1) * 100us *SAMPLE_TIME_FLK > (IT_ALS/2) + 500us *SAMPLE_TIME_SLOW/FAST >(IT_ALS/2) +1ms

FSM_RESTART Register (0x5F)

Bit	7	6	5	4	3	2	1	0
ITEM								FSM_RESTART
Access								R/W
Default								0

Bit	ITEM	Description
0	FSM_RESTART	Force Finite State Machine restart 0: No function 1: Enable FSM restart (auto clear to 0)

FIFOCTRL1 Register (0x60)

Bit	7	6	5	4	3	2	1	0
ITEM	FIFO_MULTI_I2C_RD		FIFO_MODE [1:0]					
Access	R/W		R/W					
Default	0		2'b00					

Bit	ITEM	Description
5:4	FIFO_MODE [1:0]	Set the mode of FIFO data storing. 00: FIFO OFF 01: Bypass mode 10: FIFO mode 11: Stream mode
7	FIFO_MULTI_I2C_RD	0: FIFO will be aligned to next frame if I2C sequential read operation is done (FIFO frame could be updated during a I2C sequential read operation) 1: FIFO will be aligned to next frame if whole frame is read out or read other address (FIFO frame won't be updated during a I2C sequential read operation)

FIFO1_WM_LV Register (0x61)

Bit	7	6	5	4	3	2	1	0
ITEM			FIFO_ LENGTH_ CONFIG					FIFO_ WM_LV [8]
Access			R/W					R/W
Default			0					0

Bit	ITEM	Description
5	FIFO_LENGTH_ CONFIG	FIFO length setting. 0: 256 data 1: 128 data

FIFO2_WM_LV Register (0x62)

Bit	7	6	5	4	3	2	1	0
ITEM	FIFO_WM_LV [7:0]							
Access	R/W							
Default	8'b00000000							

Bit	ITEM	Description
8:0	FIFO_WM_LV [8:0]	The FIFO_WM_LV threshold setting.

FIFOCTRL2 Register (0x63)

Bit	7	6	5	4	3	2	1	0
ITEM				FIFO_ PAUSE		FIFO_ OVR_EN	FIFO_ WM_EN	FIFO_ FULL_EN
Access				R/W		R/W	R/W	R/W
Default				0		0	0	0

Bit	ITEM	Description
0	FIFO_OVR_EN	Disable/Enable FIFO overflow interrupt. 0: Disable 1: Enable
1	FIFO_WM_EN	Disable/Enable FIFO WM interrupt. 0: Disable 1: Enable
2	FIFO_FULL_EN	Disable/Enable FIFO full interrupt. 0: Disable 1: Enable
4	FIFO_PAUSE	Disable/Enable pause FIFO update. 0: Disable 1: Enable

FIFO_FCNT1 Register (0x64)

Bit	7	6	5	4	3	2	1	0
ITEM								FIFO_FRAME_CNT [8]
Access								R
Default								0

FIFO_FCNT2 Register (0x65)

Bit	7	6	5	4	3	2	1	0
ITEM	FIFO_FRAME_CNT [7:0]							
Access	R							
Default	8'b00000000							

Bit	ITEM	Description
8:0	FIFO_FRAME_CNT [7:0]	Indicate that how many data remain in the FIFO.

FIFO_OUT Register (0x66)

Bit	7	6	5	4	3	2	1	0
ITEM	FIFO_OUT [7:0]							
Access	R							
Default	8'b00000000							

Bit	ITEM	Description
7:0	FIFO_OUT	FIFO data output, self-loop if directly read this byte.

FIFO_FLAG Register (0x67)

Bit	7	6	5	4	3	2	1	0
ITEM	FLG_FIFO_OVR			FLG_FIFO_WM				FLG_FIFO_FULL
Access	R			R				R
Default	0			0				0

Bit	ITEM	Description
0	FLG_FIFO_FULL	Indicate if FIFO_FRAME_CNT is full in FIFO mode. Read FIFO_OUT to clear. 0: No FLG_FIFO_FULL event 1: FLG_FIFO_FULL event
4	FLG_FIFO_WM	Indicate the water mark level is reached in FIFO/Stream mode. Read FIFO_OUT to clear. 0: No FLG_FIFO_WM event 1: FLG_FIFO_ WM event

7	FLG_FIFO_OVR	Indicate if FIFO_FRAME_CNT is overflow in Stream mode. Read FIFO_OUT to clear. 0: No FLG_FIFO_OVR event 1: FLG_FIFO_OVR event

FIFOCTRL3 Register (0x68)

Bit	7	6	5	4	3	2	1	0
ITEM								FIFO_ FLUSH
Access								W
Default								0

Bit	ITEM	Description
0	FIFO_FLUSH	0: No function 1: Clear FIFO data

FIFOCTRL4 Register (0x69)

Bit	7	6	5	4	3	2	1	0
ITEM			FIFO_ CLKEN	FIFO_ PWREN				
Access			R/W	R/W				
Default			0	0				

Bit	ITEM	Description
4	FIFO_PWREN	Select FIFO power. 0: Disable FIFO Power 1: Enable FIFO Power
5	FIFO_CLKEN	Select FIFO clock. 0: Disable FIFO Power 1: Enable FIFO Power

AGCCTRL1 Register (0x6A)

Bit	7	6	5	4	3	2	1	0
ITEM	EN_ALS_A UTOGAIN				PRST_AGC [1:0]		AGC_HIG H_HYST	AGC_LO W_HYST
Access	R/W				R/W		R/W	R/W
Default	0				2'b00		0	0

Bit	ITEM	Description
0	AGC_LOW_HYST	Select ALS auto-gain low threshold percentage. 0: 25% x THDH_ALS_SAT 1: 12.5% x THDH_ALS_SAT
1	AGC_HIGH_HYST	Select ALS auto-gain high threshold percentage. 0: 75% x THDH_ALS_SAT 1: 87.5% x THDH_ALS_SAT

3:2	PRST_AGC [1:0]	ALS AGC persistence setting. 00: x1 time 01: x2 times 10: x4 times 11: x8 times
7	EN_ALS_ AUTOGAIN	Disable/Enable ALS auto-gain. 0: Disable ALS auto-gain 1: Enable ALS auto-gain

MANUAL_GAIN_CTRL Register (0x6B)

Bit	7	6	5	4	3	2	1	0
ITEM								MANUAL _GAIN_ MODE
Access								R/W
Default								0

Bit	ITEM	Description
0	MANUAL_ GAIN_MODE	Select GAIN_LEVEL: 0: Disable (set if EN_ALS_AUTOGAIN (AGCCTRL1 Register 0x6A[7]) is 1) 1: Enable (set if EN_ALS_AUTOGAIN (AGCCTRL1 Register 0x6A[7]) is 0)

AGCCTRL2 Register (0x6C)

Bit	7	6	5	4	3	2	1	0
ITEM					AGC_12B _MODE	AGC_SEL _MODE		
Access					R/W	R/W		
Default					0	0		

Bit	ITEM	Description
2	AGC_SEL_ MODE	This bit must be set to 1.
3	AGC_12B_ MODE	Disable/Enable AGC_12B mode. 0: Disable (set if DATA_FORMAT_SEL (ALSCTRL Register 0xA4[2]) is 0) 1: Enable (set if DATA_FORMAT_SEL (ALSCTRL Register 0xA4[2]) is 1)

THD_SAT_GC Register (0x6D)

Bit	7	6	5	4	3	2	1	0
ITEM				TH_ALS_SAT_GC [4:0]				
Access				R/W				
Default				5'b10000				

Bit	ITEM	Description
4:0	TH_ALS_SAT_GC [4:0]	This register is used for internal analog frontend calibration. Set to 0x0A if not otherwise advised.

ITSLOW1 Register (0x6E)

Bit	7	6	5	4	3	2	1	0
ITEM					IT_ALS_SLOW [11:8]			
Access					R/W			
Default					4'b0011			

ITSLOW2 Register (0x6F)

Bit	7	6	5	4	3	2	1	0
ITEM	IT_ALS_SLOW [7:0]							
Access	R/W							
Default	8'b11111111							

Bit	ITEM	Description
11:0	IT_ALS_SLOW [11:0]	ALS_SLOW integration time setting(99us/step). 12'h000: 99us 12'h001: 198us ⋮ 12'h3FF: 101.376ms ⋮ 12'hFFF: 405.504ms

Soft reset (0x80)

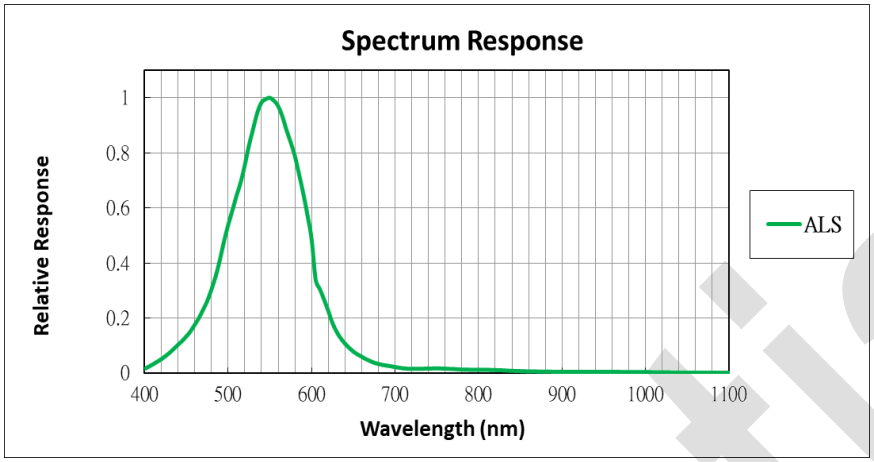
Write any data to this register will reset the chip.

ALSCTRL Register (0xA4)

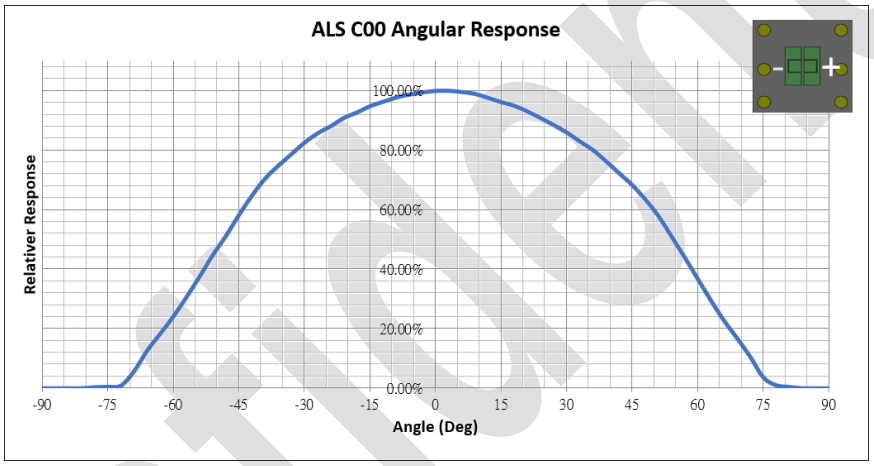
Bit	7	6	5	4	3	2	1	0
ITEM						DATA_FORMAT_SEL	ALS_SAT_EN	
Access						R/W	R/W	
Default						0	1	

Bit	ITEM	Description
1	ALS_SAT_EN	Disable/Enable ALS saturating function 0: Disable 1: Enable
2	DATA_ FORMAT_SEL	Select ALS data format. 0: 16 bits data 1: 4 bits GAIN_LEVEL+12 bits DATA_ALS

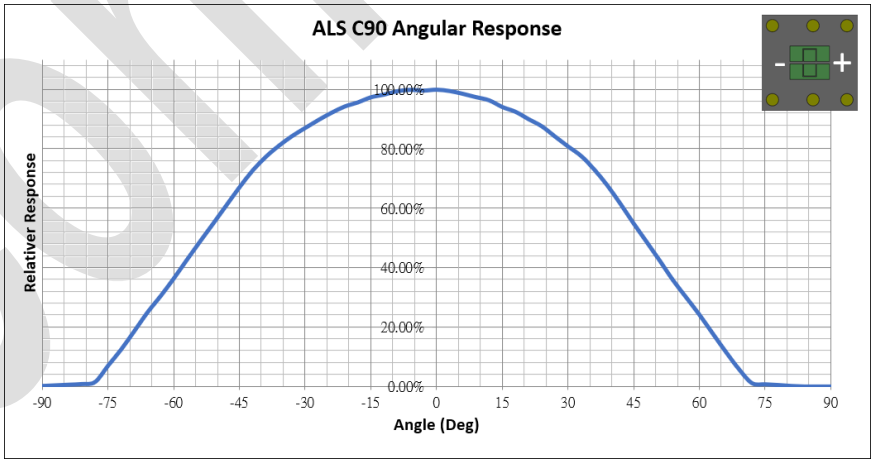
8. ALS RESPONSE CHARTS



ALS Spectrum

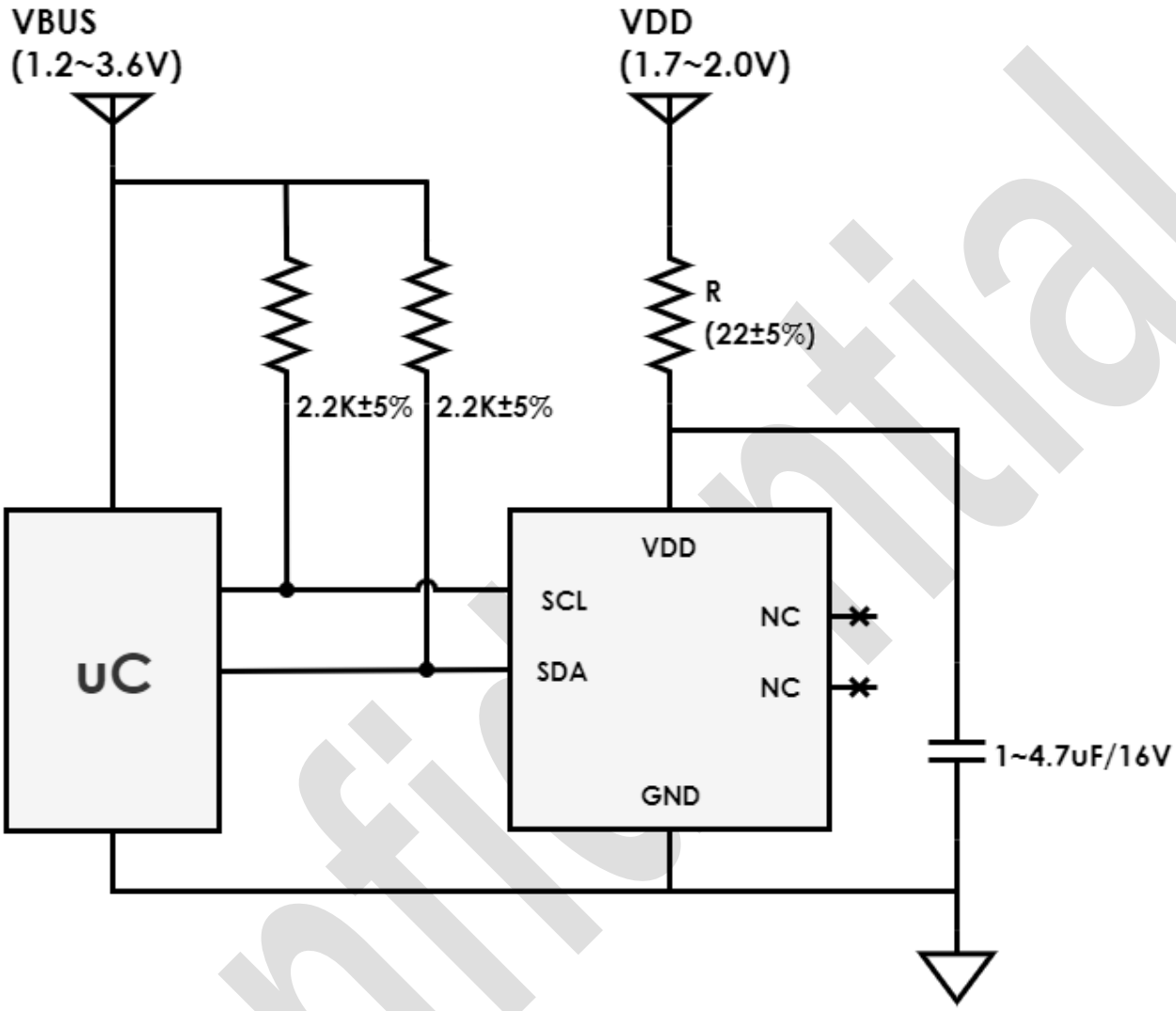


ALS C00 Angular Response



ALS C90 Angular Response

9. APPLICATION NOTE



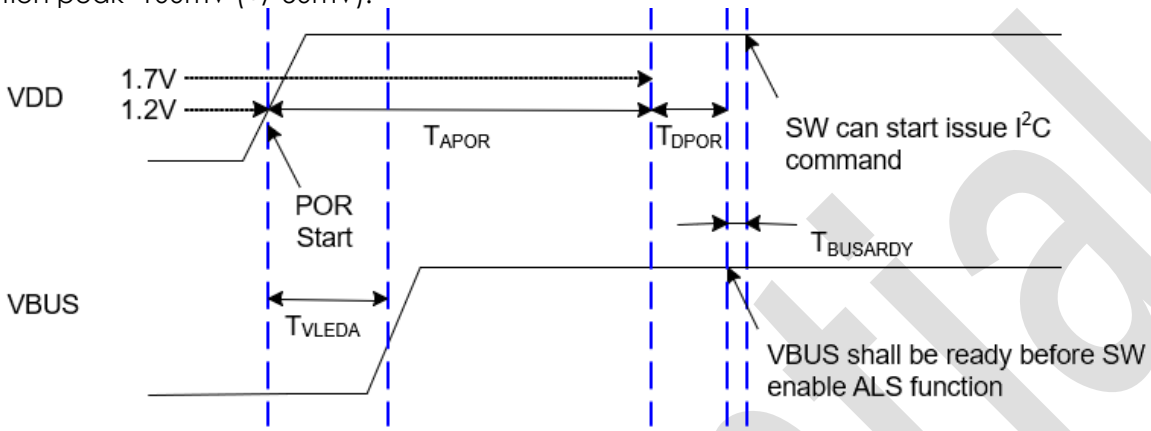
Typical Application Circuit with Independent VDD Supply Voltage

9.1 Power Noise Consideration

It is suggested that IC power to get the best performance of W1160 and an R/C low pass filter is also suggested to be added in the V_{DD} path of W1160 to reduce the switching noise from whole system. The recommended R value is 22 Ohm.

9.2 Power ON Sequence

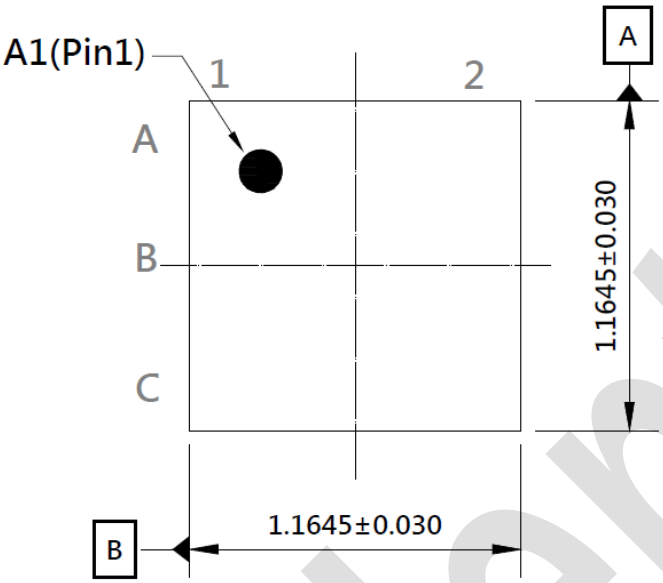
VDD variation peak=100mV (+/-50mV).



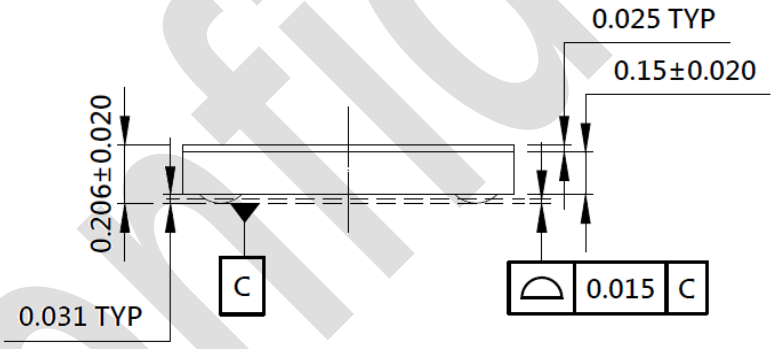
Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{APOR}	Power on reset procedure start once VDD exceed 1.2V.	30			ms
T_{VBUS}	VBUS turn on time related to VDD.	≥0			ms
T_{DPOR}	Logic circuit initialization timing and VDD shall exceed 1.7V.	5			ms
$T_{BUSARDY}$	VBUS ready before SW enable ALS function.	0			ms

10. PACKAGE OUTLINE

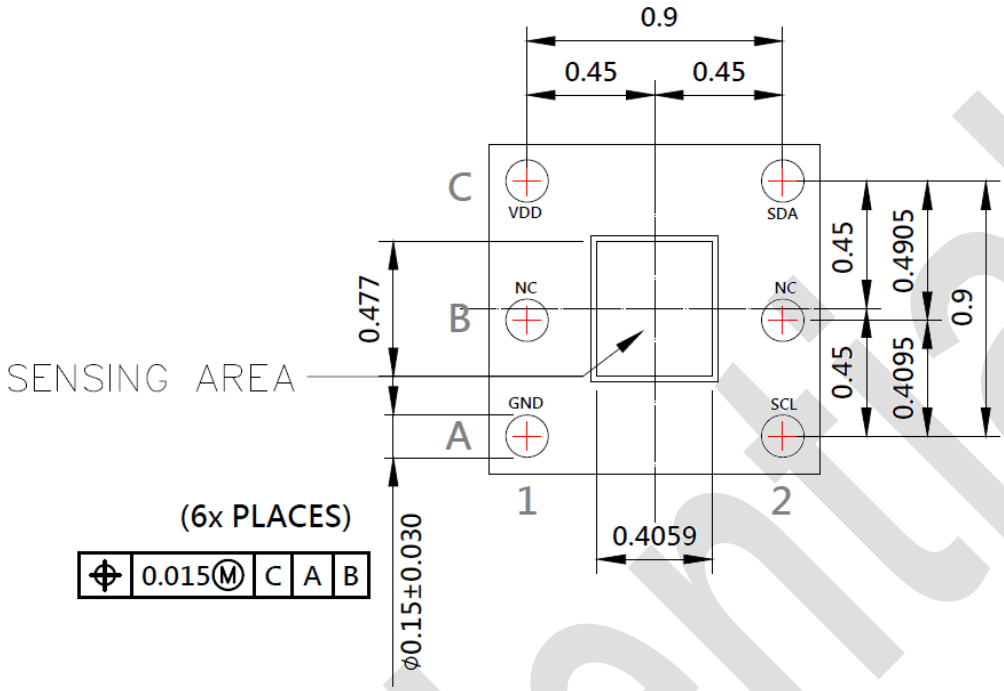
Top View



Side View



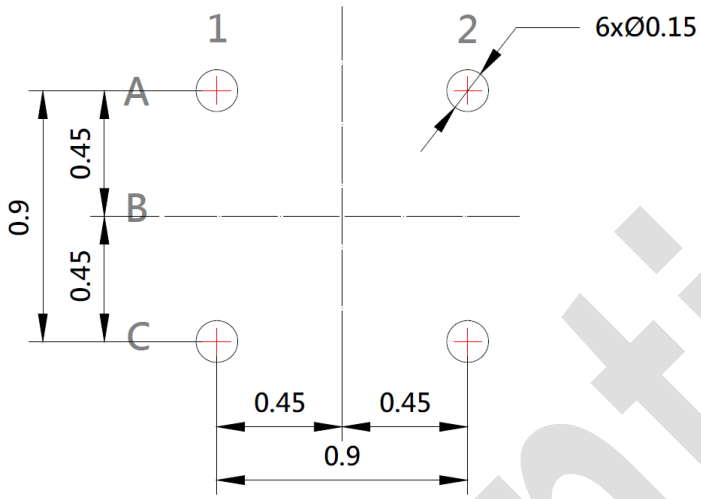
Bottom View



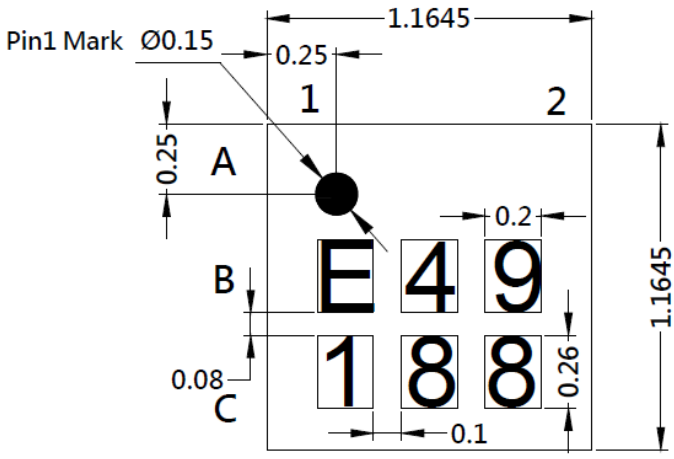
Notes: all linear dimensions are in mm.

PCB Pad Layout Recommendation

Top Perspective



Marking Rule (Topside)



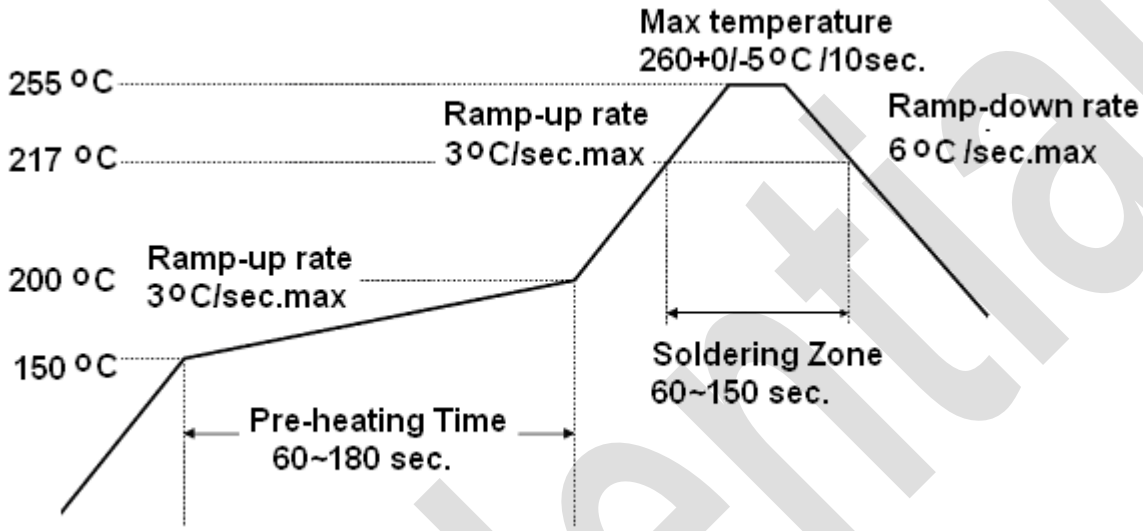
E: Device Code/W1160
49: Week Code/Ex. wk49=49, wk50=50
188: Wafer Lot Code/Ex. D6A188.02=188

1. UNIT: mm
2. TOLERANCE: ±0.1mm

11. SOLDERING INFORMATION

11.1 Soldering Condition

1. Pb-free solder temperature profile



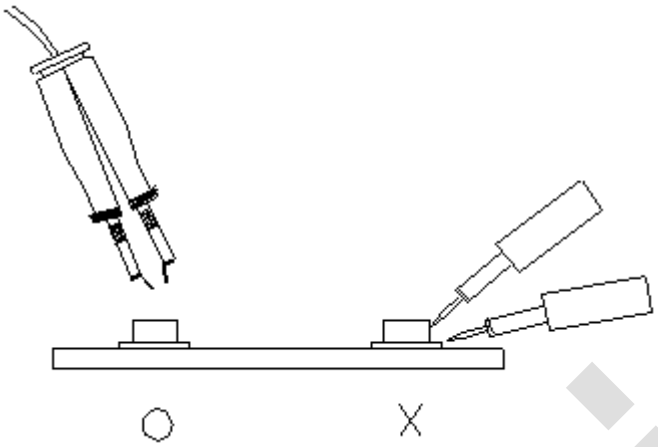
2. Reflow soldering should not be done more than three times.
3. When soldering, do not put stress on the Ics during heating.
4. After soldering, do not warp the circuit board.

11.2 Soldering Iron

Each terminal is to go to the tip of soldering iron temperature less than 350°C for 3 seconds within once in less than the soldering iron capacity 25W. Leave two seconds and more intervals and do soldering of each terminal. Be careful because the damage of the product is often started at the time of the hand solder.

11.3 Repairing

Repair should not be done after the Ics have been soldered. When repairing is unavoidable, a double-head soldering iron should be used (as below figure). It should be confirmed beforehand whether the characteristics of the Ics will or will not be damaged by repairing.



12. STORAGE INFORMATION

12.1 Storage Condition

1. Devices are packed in moisture barrier bags (MBB) to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.
2. The delivery product should be stored with the conditions shown below:

Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

12.2 Treatment After Unsealed

1. Floor life (time between soldering and removing from MBB) must not exceed the time shown below:

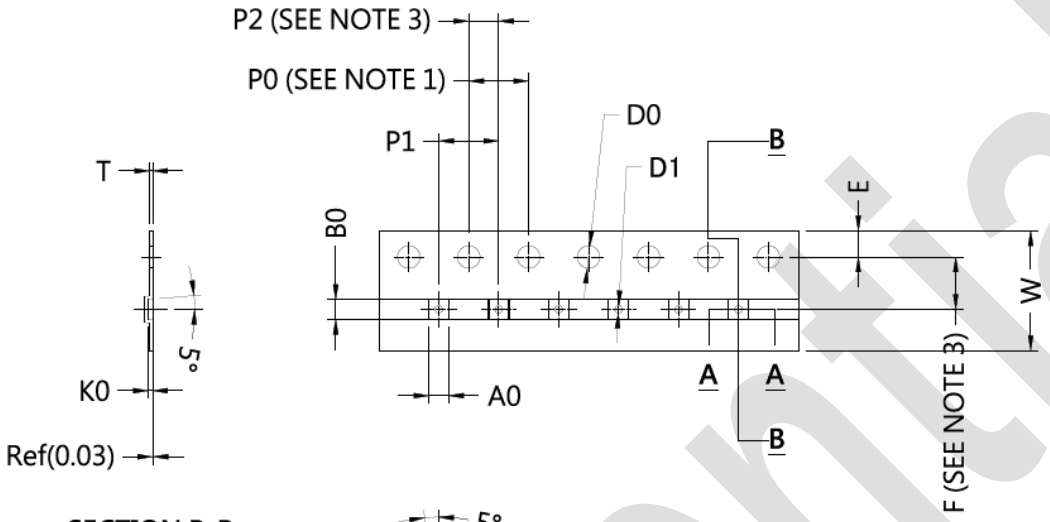
Floor Life	168 Hours
Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

2. When the floor life limits have been exceeded or the devices are not stored in dry conditions, they must be re-baked before reflowing to prevent damage to the devices. The recommended conditions are shown below

Temperature	60℃
Re-Baking Time	12 Hours

13. TAPE AND REEL DIMENSION

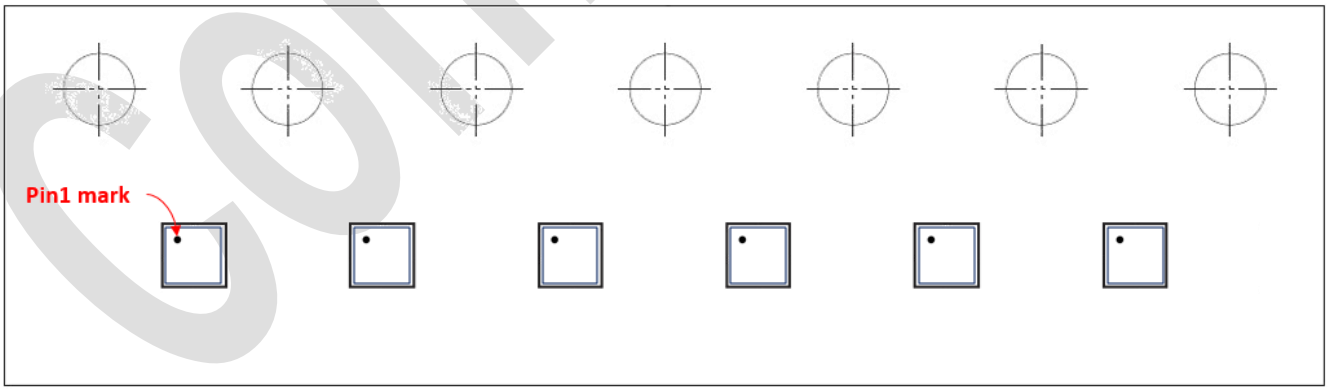
Tape Dimension



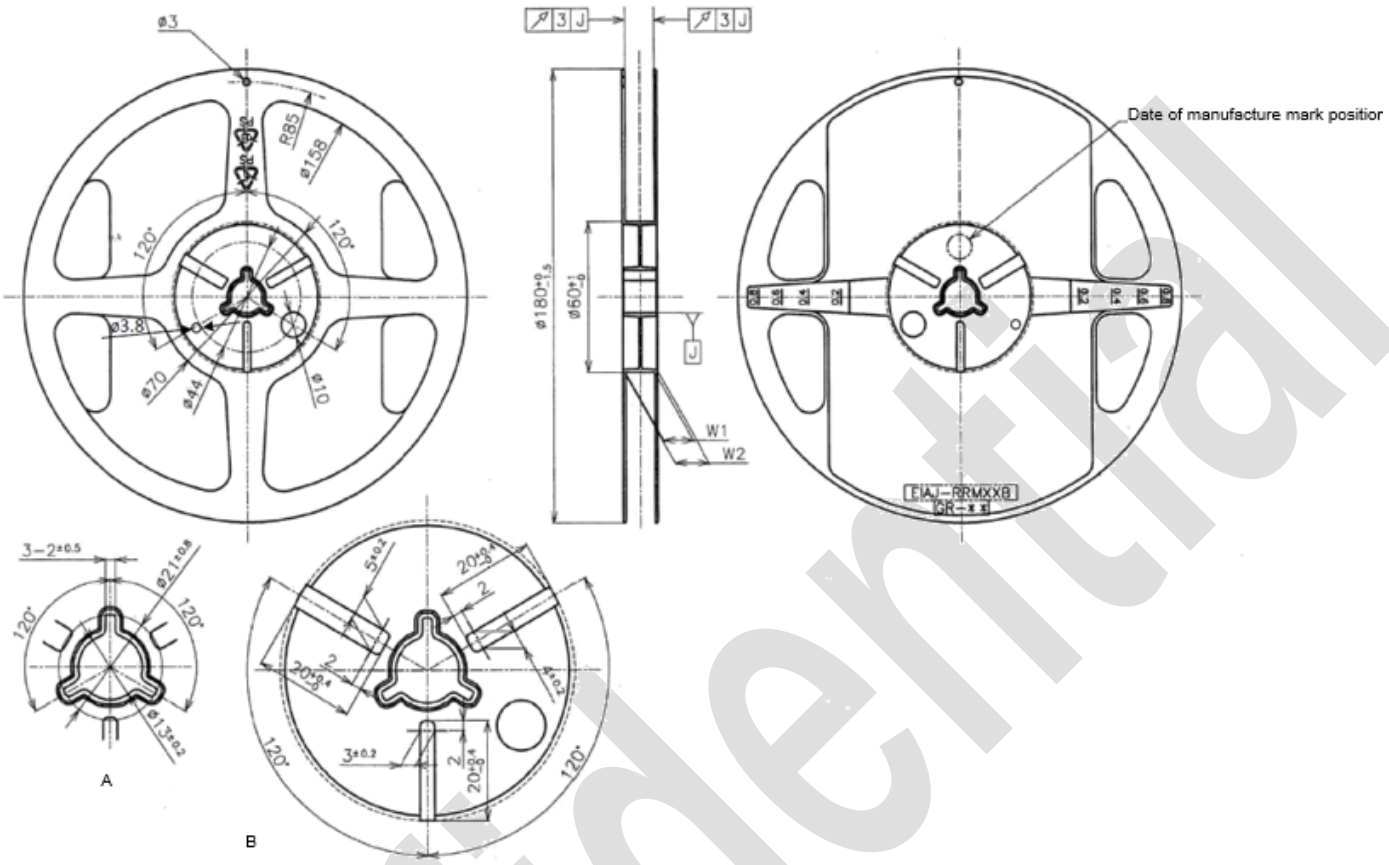
NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Item	Specification	Tol. (+/-)	Item	Specification	Tol. (+/-)
W	8.00	±0.20	A0	1.32	±0.05
E	1.75	±0.10	B0	1.32	±0.05
F	3.50	±0.05	K0	0.30	±0.05
D0	1.50	+0.1/-0.0	T	0.23	±0.05
D1	0.50	±0.10			
P0	4.00	±0.10			
P1	4.00	±0.10			
P2	2.00	±0.05			

Relative Position for Tape and IC



Reel Dimension



Notes: all linear dimensions are in mm.

Revision History

Date	Version	Modified Items
2022/8/12	0.9	Initial release.
2022/8/19	0.9.1	Modify Storage Condition

