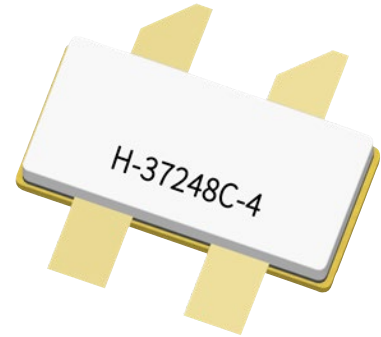


GTRA364002FC

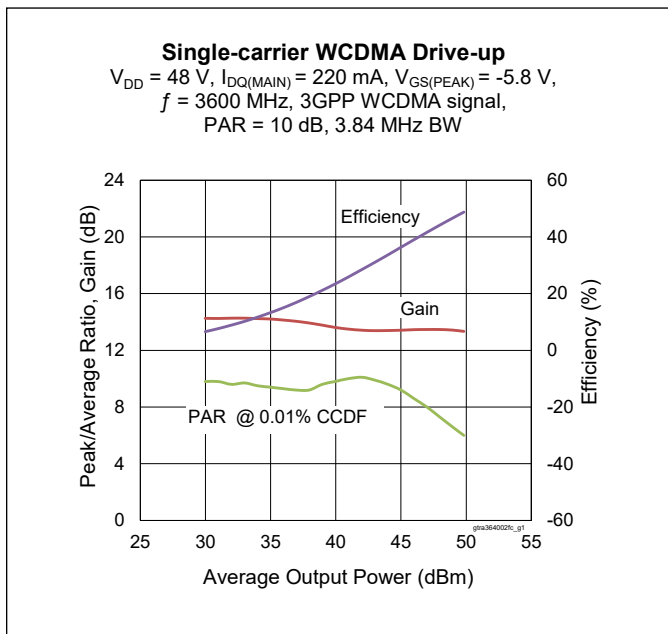
Thermally-Enhanced High Power RF GaN on SiC Amplifier, 400 W, 48 V, 3400 – 3600 MHz

Description

The GTRA364002FC is a 400-watt (P_{3dB}) GaN on SiC HEMT D-mode amplifier designed for use in multi-standard cellular power amplifier applications. It features input matching, high efficiency, and a thermally-enhanced package with earless flange.



Package Types: H-37248C-4



Features

- GaN on SiC HEMT technology
- Input matched
- Asymmetrical Doherty design
 - Main: $P_{3dB} = 170\text{ W Typ}$
 - Peak: $P_{3dB} = 230\text{ W Typ}$
- Typical Pulsed CW performance, 3400 to 3600 MHz, 48 V, combined outputs, Doherty @ P_{3dB} , 10 μs , 10% duty cycle
 - Output power = 400 W
 - Efficiency = 60 %
 - Gain = 14 dB
- Capable of handling 10:1 VSWR @ 48 V, 50 W (WCDMA) output power
- Human Body Model Class 1A, (per ANSI/ESDA/JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in the Doherty production test fixture)

$V_{DD} = 48\text{ V}$, $I_{DQ} = 220\text{ mA}$, $P_{OUT} = 50\text{ W avg}$, $V_{GS(PEAK)} = V_{GS} @ I_{DQ} = 200\text{ mA} - 2.7\text{ V}$, $f = 3600\text{ MHz}$, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Gain	G_{ps}	12	13	—	dB
Drain Efficiency	η_D	36	40	—	%
Adjacent Channel Power Ratio	ACPR	—	-30	-27	dBc
Output PAR @ 0.01% CCDF	OPAR	6.4	7.7	—	dB

Note:

All published data at $T_{CASE} = 25^\circ\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!



DC Characteristics

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source Breakdown Voltage (Main)	$V_{BR(DSS)}$	150	—	—	V	$V_{GS} = -8\text{ V}, I_D = 3\text{ mA}$
Drain-source Breakdown Voltage (Peak)						$V_{GS} = -8\text{ V}, I_D = 4\text{ mA}$
Drain-source Leakage Current	I_{DSS}	—	—	5	mA	$V_{GS} = -8\text{ V}, V_{DS} = 10\text{ V}$
Gate Threshold Voltage (main)	$V_{GS(th)}$	-3.8	-3.0	-2.3	V	$V_{DS} = 10\text{ V}, I_D = 21.6\text{ mA}$
Gate Threshold Voltage (peak)						$V_{DS} = 10\text{ V}, I_D = 28.8\text{ mA}$

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	0	—	50	V	$V_{DS} = 48\text{ V}, I_D = 220\text{ mA}$
Gate Quiescent Voltage	$V_{GS(Q)}$	-3.7	-2.9	-2.1		

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	125	V
Gate-source Voltage	V_{GS}	-10 to +2	
Operating Voltage	V_{DD}	55	
Gate Current (main)	I_G	21.6	mA
Gate Current (peak)		28.8	
Drain Current (main)	I_D	8.1	A
Drain Current (peak)		10.8	
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	-65 to +150	

Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range (V_{DD}) specified above.

Thermal Characteristics

Characteristics	Symbol	Value	Unit	Conditions
Thermal Resistance (main)	$R_{\theta JC}$	1.55	°C/W	$T_{CASE} = 70\text{ °C}, 101\text{ W DC}$
Thermal Resistance (peak)		1.20		$T_{CASE} = 70\text{ °C}, 130\text{ W DC}$

Ordering Information

Type and Version	Order Code	Package	Shipping
GTRA364002FC V1 R0	GTRA364002FC-V1-R0	H-37248C-4	Tape & Reel, 50 pcs
GTRA364002FC V1 R2	GTRA364002FC-V1-R2	H-37248C-4	Tape & Reel, 250 pcs

Typical Performance (data taken in test fixture)

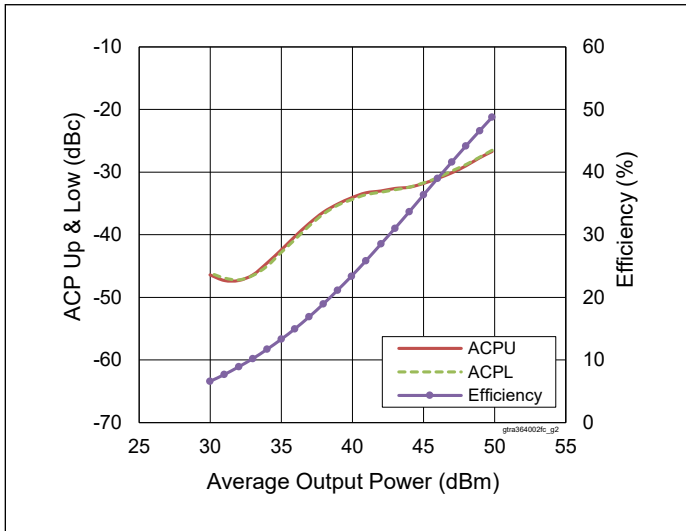


Figure 1. Single-carrier WCDMA Drive-up

$V_{DD} = 48\text{ V}$, $I_{DQ(MAIN)} = 220\text{ mA}$, $V_{GS(PEAK)} = -5.8\text{ V}$,
 $f = 3600\text{ MHz}$, 3GPP WCDMA signal,
 $PAR = 10\text{ dB}$, $BW = 3.84\text{ MHz}$

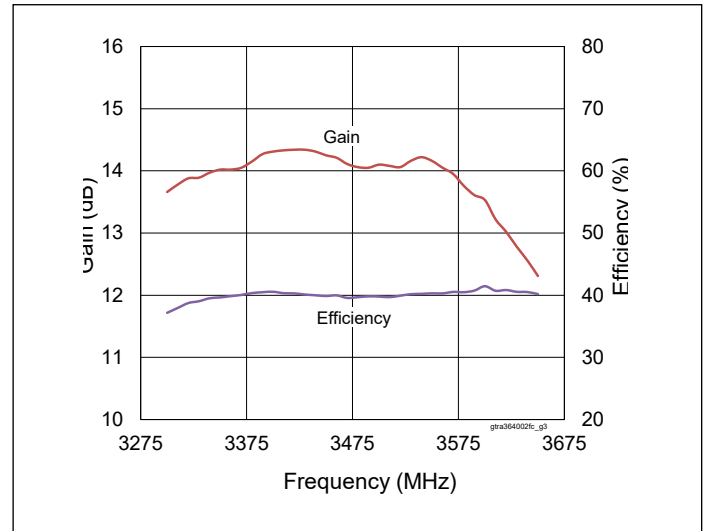


Figure 2. Single-carrier WCDMA Broadband Performance

$V_{DD} = 48\text{ V}$, $I_{DQ(MAIN)} = 220\text{ mA}$, $V_{GS(PEAK)} = -5.8\text{ V}$,
 $P_{OUT} = 47\text{ dBm}$, 3GPP WCDMA signal,
 $PAR = 10\text{ dB}$

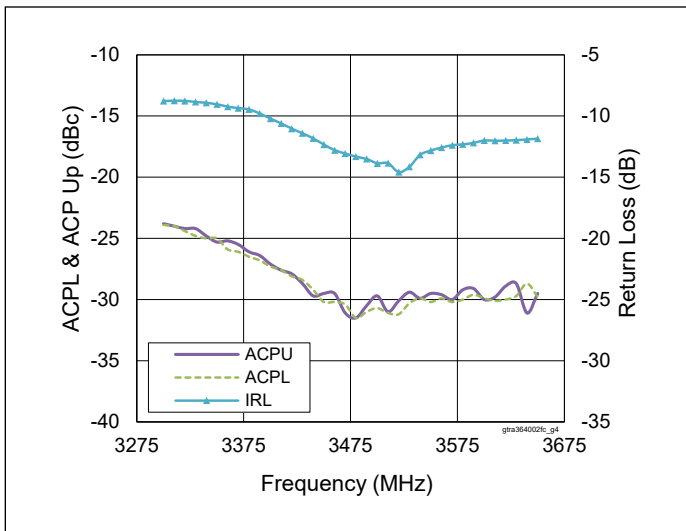


Figure 3. Single-carrier WCDMA Broadband Performance

$V_{DD} = 48\text{ V}$, $I_{DQ(MAIN)} = 220\text{ mA}$, $V_{GS(PEAK)} = -5.8\text{ V}$,
 $P_{OUT} = 47\text{ dBm}$, 3GPP WCDMA signal,
 $PAR = 10\text{ dB}$

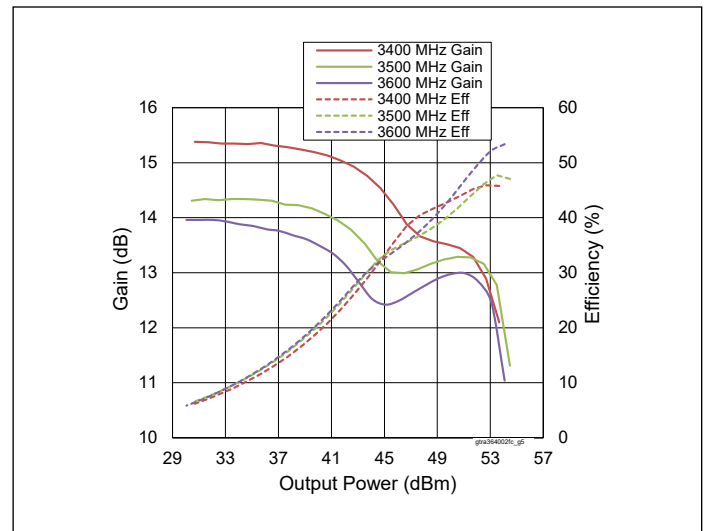


Figure 4. CW Performance

$V_{DD} = 48\text{ V}$, $I_{DQ(MAIN)} = 220\text{ mA}$,
 $V_{GS(PEAK)} = -5.8\text{ V}$

Typical Performance (cont.)

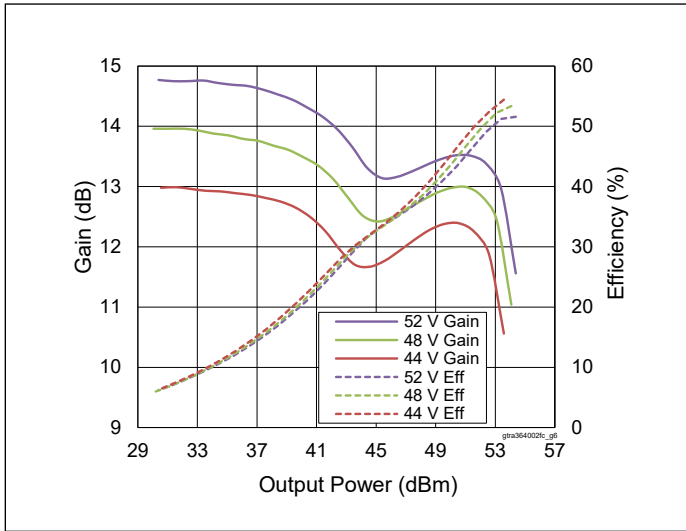


Figure 5. CW Performance at various V_{DD}
 $I_{DQ(MAIN)} = 220 \text{ mA}$, $V_{GS(PEAK)} = -5.8 \text{ V}$,
 $f = 3600 \text{ MHz}$

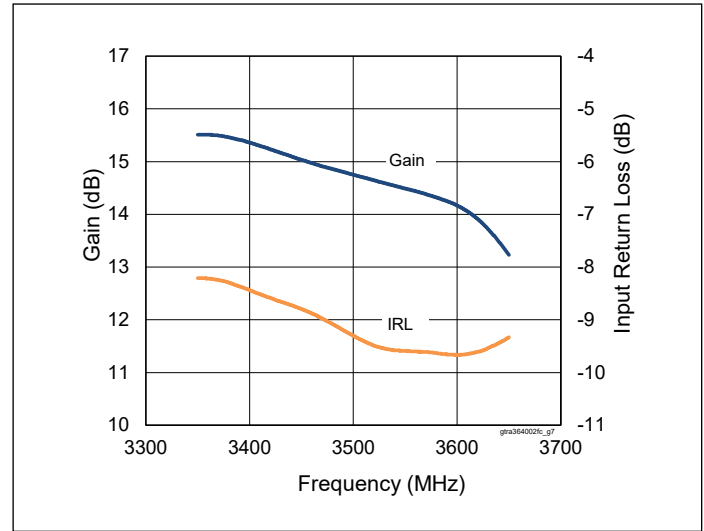


Figure 6. CW Performance Small Signal
 Gain & Input Return Loss

$V_{DD} = 48 \text{ V}$, $I_{DQ(MAIN)} = 220 \text{ mA}$, $V_{GS(PEAK)} = -5.8 \text{ V}$

Load Pull Performance

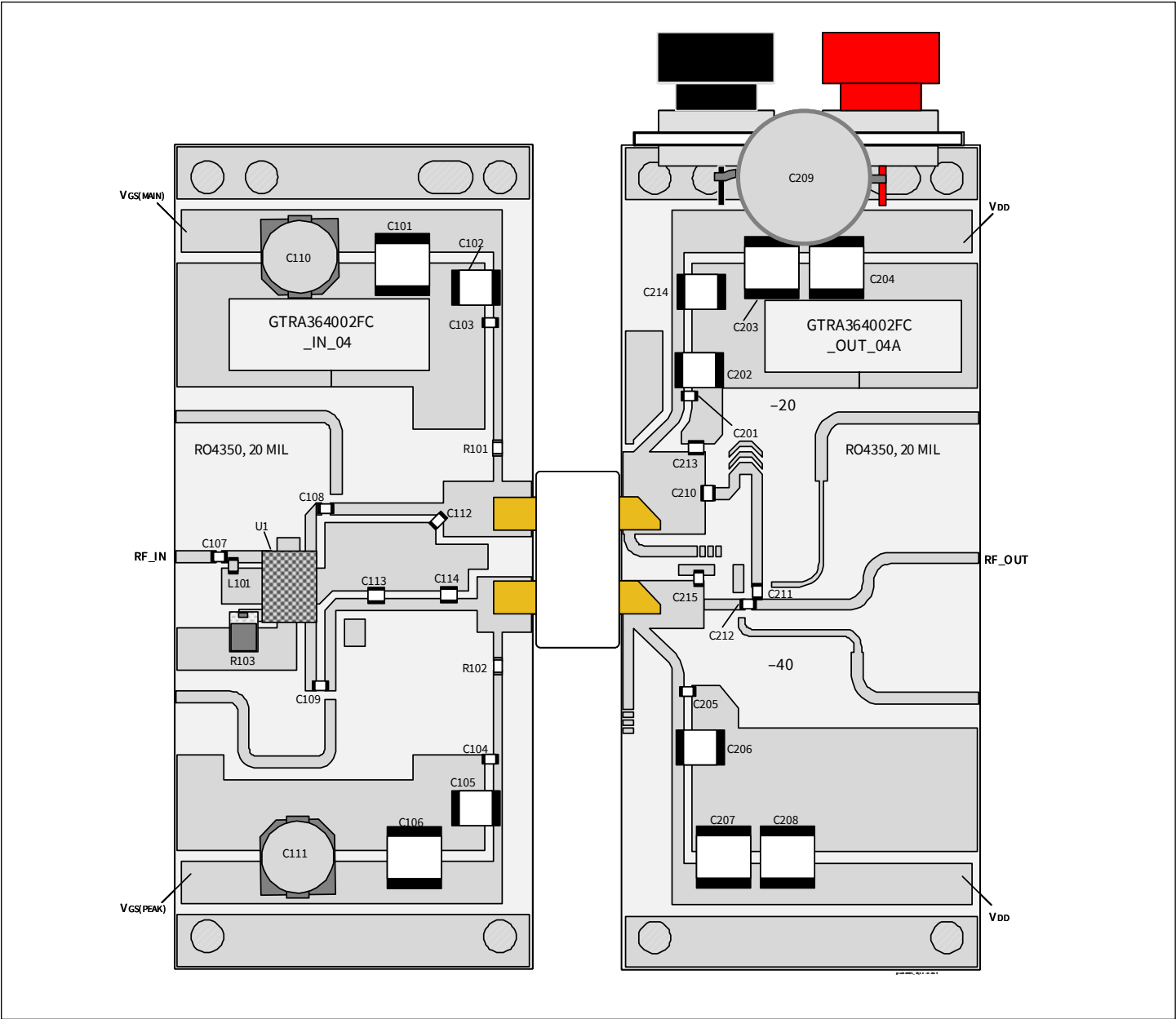
Main Side Load Pull Performance – Pulsed CW signal: 10 μs , 10% duty cycle, 48 V, $I_{DQ} = 220 \text{ mA}$, class AB

P_{3dB}											
Max Output Power							Max Drain Efficiency				
Freq [MHz]	$Z_s [\Omega]$	$Z_L [\Omega]$	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	η_D [%]	$Z_L [\Omega]$	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	η_D [%]
3400	9.0-j3.4	4.3-j6.5	15.3	53.90	245	62.5	1.7-j3.5	17.3	52.40	174	74.0
3500	5.0-j5.2	3.8-j7.0	15.4	54.00	251	63.9	2.2-j5.0	17.4	52.10	162	76.0
3600	3.5-j7.0	4.4-j7.1	14.9	53.80	240	61.2	2.4-j5.2	16.8	52.10	162	74.0

Peak Side Load Pull Performance – Pulsed CW signal: 10 μs , 10% duty cycle, 48 V, $I_{DQ} = 280 \text{ mA}$, class AB

P_{3dB}											
Max Output Power							Max Drain Efficiency				
Freq [MHz]	$Z_s [\Omega]$	$Z_L [\Omega]$	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	η_D [%]	$Z_L [\Omega]$	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	η_D [%]
3400	16.5-j22	3.1-j6.2	15.6	55.10	324	59.0	2.1-j4.4	17.8	53.70	234	70.0
3500	20-j13	2.8-j6.6	15.8	55.10	324	59.5	1.9-j4.7	18.3	53.00	200	69.0
3600	15.7-j7.4	3.7-j6.8	15.3	54.90	309	56.0	2.0-j4.8	17.5	53.00	200	66.0

Evaluation Board, 3400 – 3600 MHz



Reference circuit assembly diagram (not to scale)

Evaluation Board Part Number	LTA/GTRA364002FC-V1
PCB Information	Rogers 4350, 0.508 mm [0.020"] thick, 2 oz. copper, $\epsilon_r = 3.66$, $f = 3400 - 3600$ MHz

Components Information

Component	Description	Manufacturer	P/N
Input			
C101, C106	Capacitor, 10 μ F, 100 V	TDK Corporation	C5750X7S2A106M230KB
C102, C105	Capacitor, 1 μ F	TDK Corporation	C4532X7R2A105M230KA
C103, C104, C107, C108, C109	Capacitor, 10 pF	ATC	ATC800A100JT250T
C110, C111	Capacitor, 100 μ F, 35 V	Panasonic Electronic Components	EEE-FT1V101AP
C112, C114	Capacitor, 0.2 pF	ATC	ATC800A0R2BT250T
C113	Capacitor, 0.8 pF	ATC	ATC800A0R8CT250T
L101	Inductor, 4.7 nH	EPCOS (TDK)	B82496C3479J000
R101, R102	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-3GEYJ100V
R103	Resistor, 50 ohms	Richardson	C8A50Z4A
U1	Hybrid Coupler	Anaren	XC3500P-03S
Output			
C201, C205, C211, C212	Capacitor, 10 pF	ATC	ATC800A100JT250T
C202, C206, C214	Capacitor, 1 μ F	TDK Corporation	C4532X7R2A105M230KA
C203, C204, C207, C208	Capacitor, 10 μ F, 100 V	TDK Corporation	C5750X7S2A106M230KB
C209	Capacitor, 220 μ F, 100 V	Panasonic Electronic Components	ECA-2AHG221
C210	Capacitor, 1 pF	ATC	ATC800A1R0CT250T
C213	Capacitor, 0.2 pF	ATC	ATC800A0R2BT250T
C215	Capacitor, 0.6 pF	ATC	ATC800A0R6CT250T

Bias Sequencing

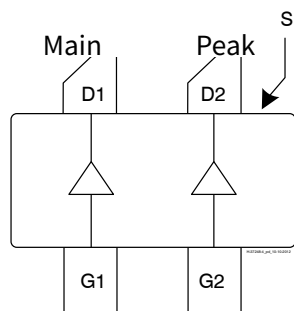
Bias ON

1. Ensure RF is turned off
2. Apply pinch-off voltage of -5 V to the gate
3. Apply nominal drain voltage
4. Bias gate to desired quiescent drain current
5. Apply RF

Bias OFF

1. Turn RF off
2. Apply pinch-off voltage to the gate
3. Turn-off drain voltage
4. Turn-off gate voltage

Pinout Diagram (top view)



Pin	Description
D1	Drain Device 1 (Main)
D2	Drain Device 2 (Peak)
G1	Gate Device 1 (Main)
G2	Gate Device 2 (Peak)
S	Source (flange)

Technical drawing of a mechanical part showing two views: a top view and a side view.

Top View Dimensions:

- Overall width: 12.70 [0.500]
- Overall height: 19.43 [0.765]
- Distance from top edge to centerline: 4.83 ± 0.51 [0.190 ± 0.020]
- Distance from bottom edge to centerline: 9.78 [0.385]
- Distance from centerline to D1/D2 holes: 8.89 [0.350]
- Distance from centerline to G1/G2 holes: 3.81 [0.150]
- Distance from centerline to D1/D2 holes (alternative): 5.08 [0.200]
- Radius of D1/D2 holes: R0.51 ^{+0.38}/_{-0.13} [R.020 ^{+0.015}/_{-0.005}]
- Angle of D1/D2 holes: Δ 45° X 2.72 [0.107]

Side View Dimensions:

- Overall thickness: 1.02 [0.040]
- Distance from top edge to centerline: 3.78 ± 0.25 [0.149 ± 0.010]
- Distance from centerline to D1/D2 holes: 19.81 ± 0.20 [0.780 ± 0.008]
- Distance from centerline to G1/G2 holes: 20.57 [0.810]
- Surface finish symbol: SPH 1.57 [0.062]

1. Interpret dimensions and tolerances per ASME Y14.5M-1994
2. Primary dimensions are mm, alternate dimensions are inches
3. All tolerances ± 0.127 [0.005]
4. Pins: D1, D2 – drain, G1, G2 – gate, S – source (flange)
5. Lead thickness: 0.13 ± 0.05 [0.005 $\pm$ 0.002]
6. Gold plating thickness: 1.14 ± 0.38 micron [45 $\pm$ 15 microinch]

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