

N-Channel Power MOSFET

30V, 129A, 3.3mΩ

FEATURES

- Low $R_{DS(ON)}$ to minimize conductive loss
- Low gate charge for fast power switching
- 100% UIS and R_g tested
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

KEY PERFORMANCE PARAMETERS

PARAMETER		VALUE	UNIT
V_{DS}		30	V
$R_{DS(ON)}$ (max)	$V_{GS} = 10V$	3.3	mΩ
	$V_{GS} = 4.5V$	4.4	
Q_g		16	nC

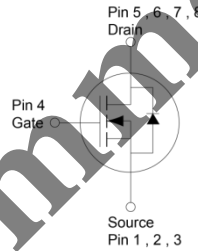
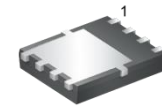
APPLICATION

- DC-DC Converters
- Battery Power Management
- ORing FET/Load Switching


 RoHS
COMPLIANT

 HALOGEN
FREE

PDFN56



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (Note 1)	$T_C = 25^\circ\text{C}$	I_D	129	A
	$T_A = 25^\circ\text{C}$		21	
Pulsed Drain Current		I_{DM}	516	A
Single Pulsed Avalanche Current (Note 2)		I_{AS}	29	A
Single Pulsed Avalanche Energy (Note 2)		E_{AS}	126	mJ
Total Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	96	W
	$T_C = 125^\circ\text{C}$		19	
Total Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	2.6	W
	$T_A = 125^\circ\text{C}$		0.5	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	1.3	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	48	$^\circ\text{C/W}$

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	30	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$	$V_{GS(TH)}$	1.2	1.6	2.5	V
Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = 30V$	I_{DSS}	--	--	1	μA
	$V_{GS} = 0V, V_{DS} = 30V$ $T_J = 125^{\circ}C$		--	--	100	
	Drain-Source On-State Resistance (Note 3)		$V_{GS} = 10V, I_D = 21A$	$R_{DS(on)}$	--	
	$V_{GS} = 4.5V, I_D = 21A$	--	3.6		4.4	
Forward Transconductance (Note 3)	$V_{DS} = 5V, I_D = 21A$	g_{fs}	--	69	--	S
Dynamic (Note 4)						
Total Gate Charge	$V_{GS} = 10V, V_{DS} = 15V,$ $I_D = 21A$	Q_g	--	31	--	nC
Total Gate Charge	$V_{GS} = 4.5V, V_{DS} = 15V,$ $I_D = 21A$	Q_g	--	16	--	
Gate-Source Charge		Q_{gs}	--	5.6	--	
Gate-Drain Charge		Q_{gd}	--	5.5	--	
Input Capacitance	$V_{GS} = 0V, V_{DS} = 15V$ $f = 1.0MHz$	C_{iss}	--	1850	--	pF
Output Capacitance		C_{oss}	--	418	--	
Reverse Transfer Capacitance		C_{rss}	--	189	--	
Gate Resistance	$f = 1.0MHz$	R_g	0.4	1.4	2.8	Ω
Switching (Note 4)						
Turn-On Delay Time	$V_{GS} = 10V, V_{DS} = 15V,$ $I_D = 12A, R_G = 10\Omega,$ $R_L = 1.25\Omega$	$t_{d(on)}$	--	16.3	--	ns
Turn-On Rise Time		t_r	--	7.8	--	
Turn-Off Delay Time		$t_{d(off)}$	--	47	--	
Turn-Off Fall Time		t_f	--	11.5	--	
Source-Drain Diode						
Forward Voltage (Note 3)	$V_{GS} = 0V, I_S = 21A$	V_{SD}	--	--	1.2	V
Reverse Recovery Time	$I_S = 21A,$	t_{rr}	--	32	--	ns
Reverse Recovery Charge	$di/dt = 100A/\mu s$	Q_{rr}	--	26	--	nC

Notes:

- Silicon limited current only.
- $L = 0.3\text{mH}, V_{GS} = 10V, V_{DS} = 25V, R_G = 25\Omega, I_{AS} = 29A$, Starting $T_J = 25^\circ\text{C}$
- Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- Switching time is essentially independent of operating temperature.

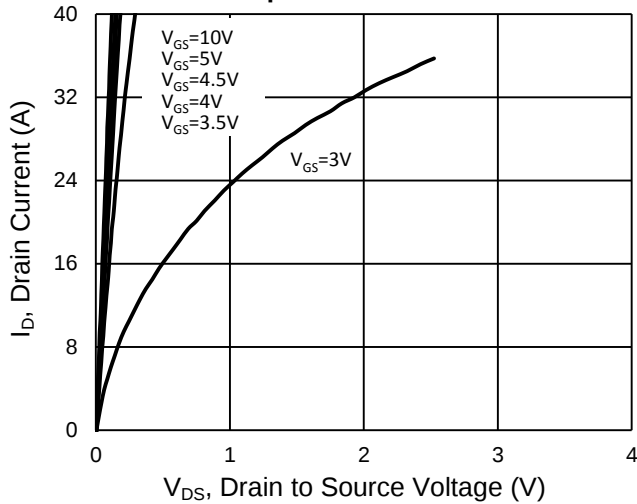
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM033NA03CR RLG	PDFN56	2,500pcs / 13" Reel

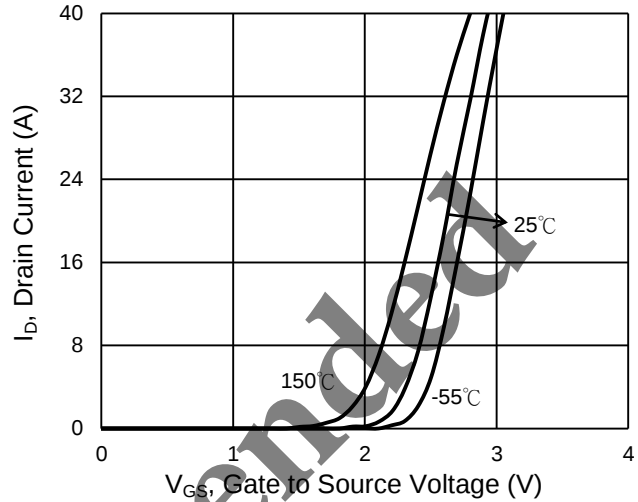
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

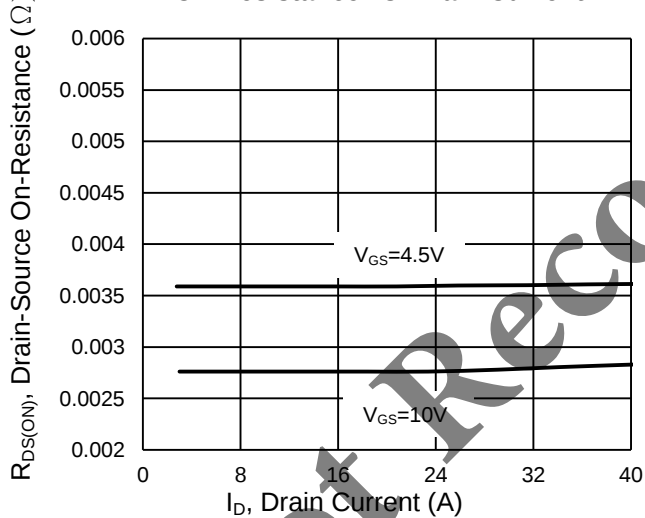
Output Characteristics



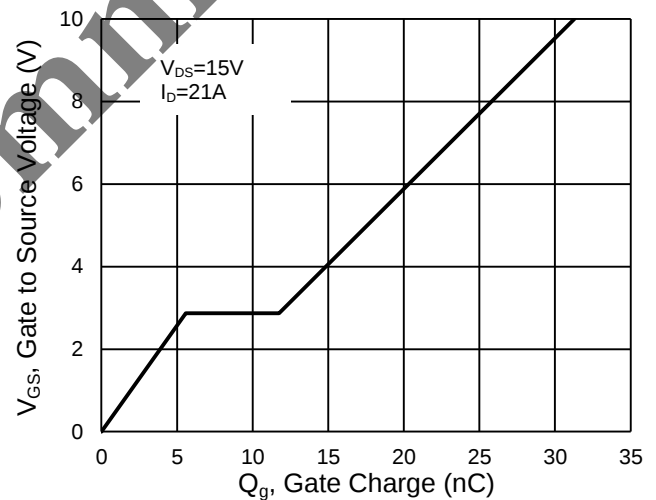
Transfer Characteristics



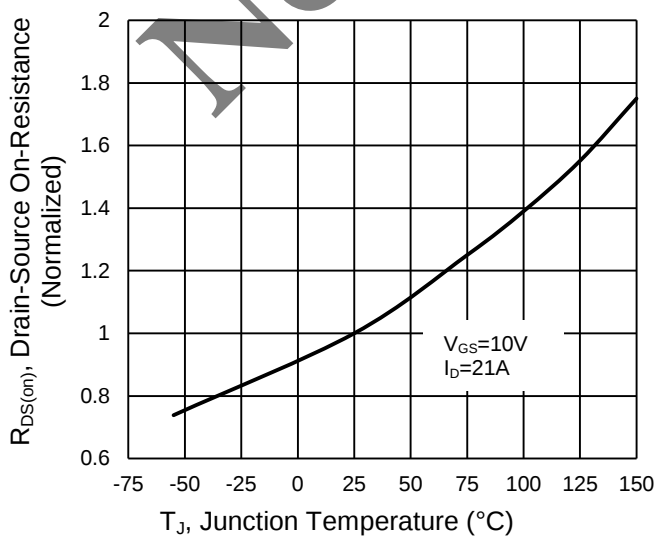
On-Resistance vs. Drain Current



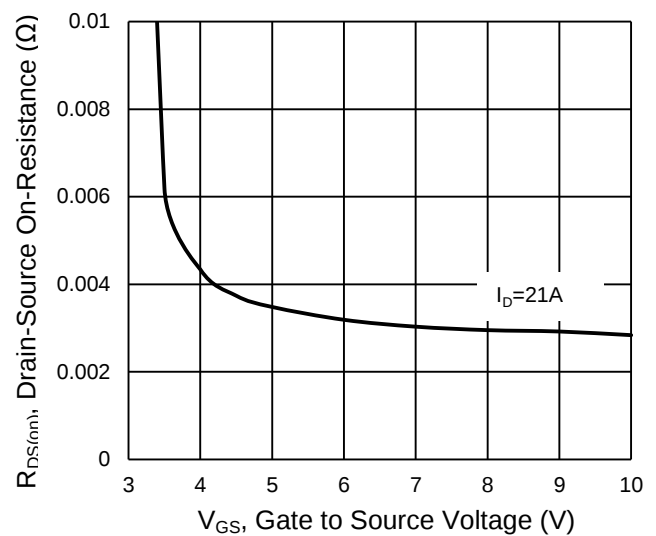
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature

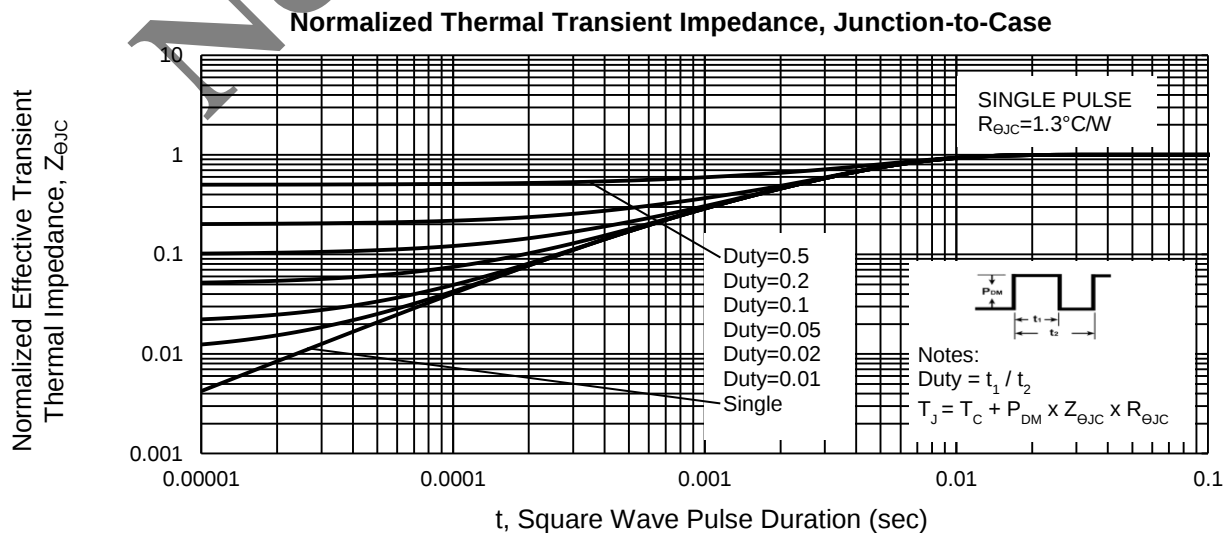
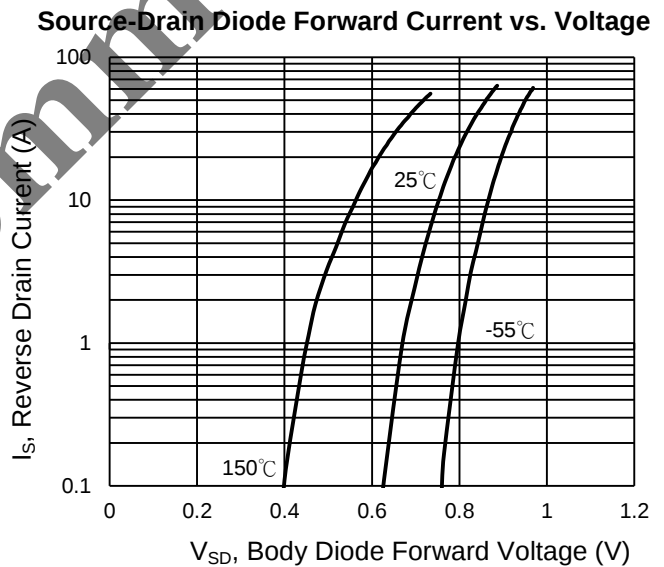
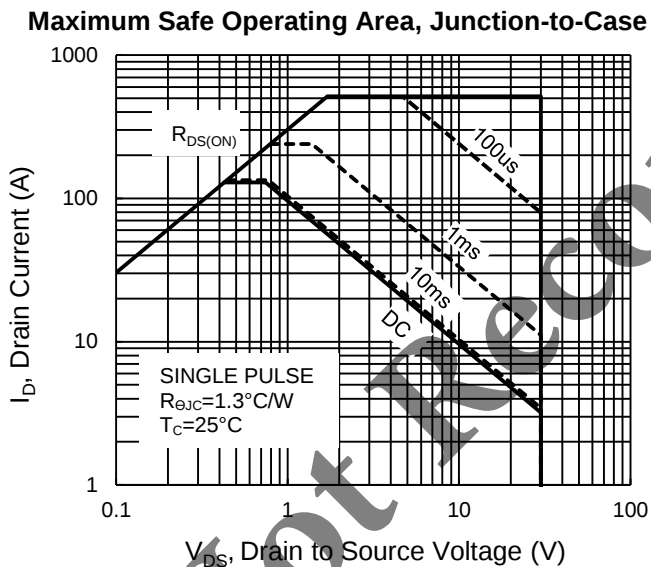
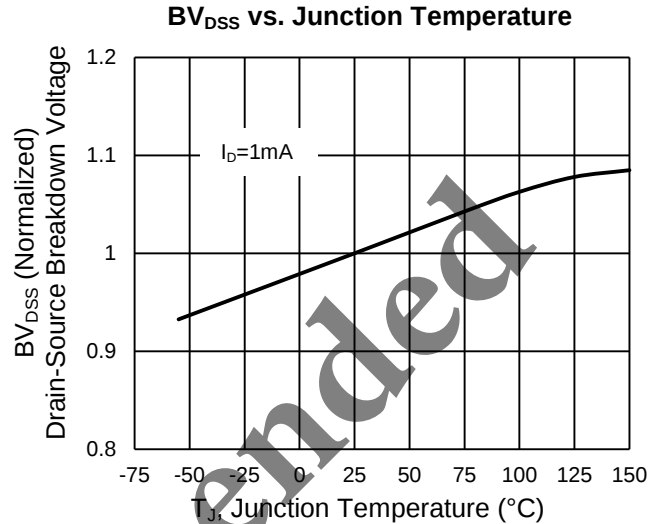
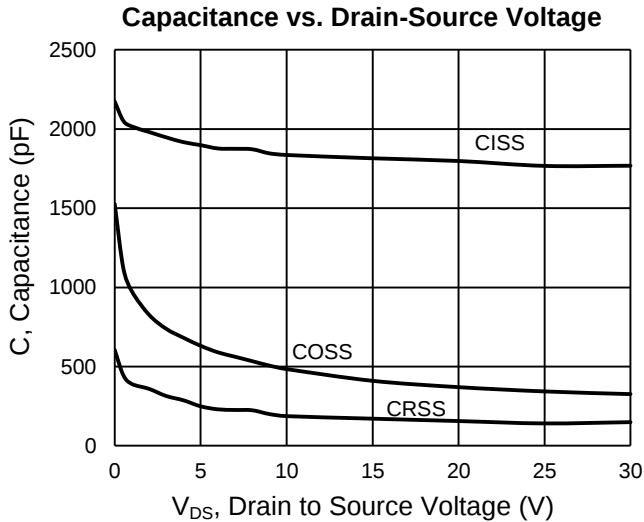


On-Resistance vs. Gate-Source Voltage



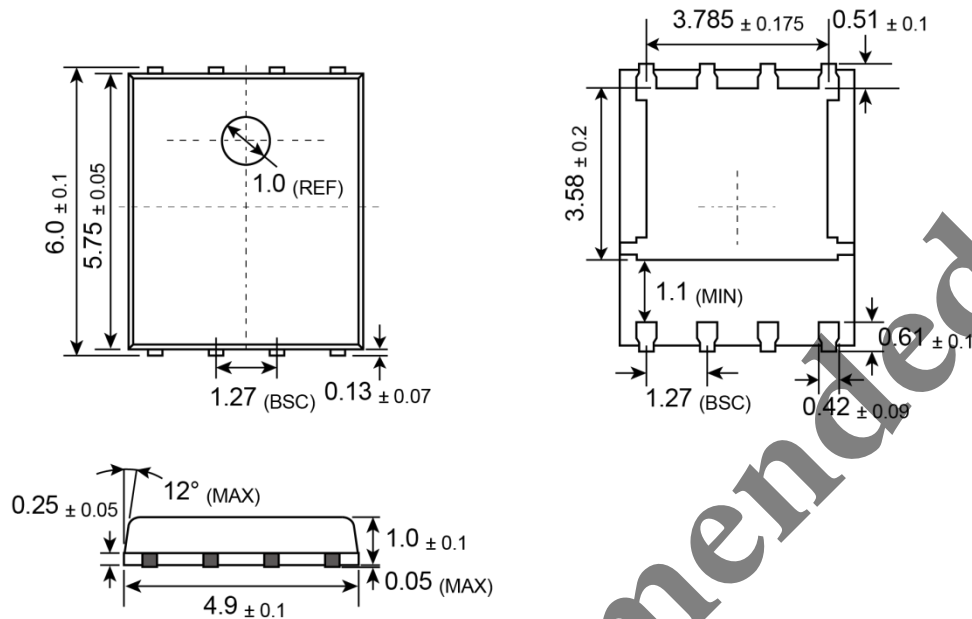
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

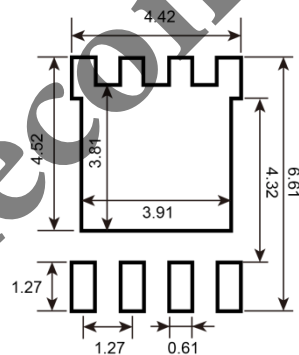


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

Not Recommended

Notice

Specifications of the products displayed herein are subject to change without notice. TSC or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, to any intellectual property rights is granted by this document. Except as provided in TSC's terms and conditions of sale for such products, TSC assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of TSC products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify TSC for any damages resulting from such improper use or sale.