RAA214250

500mA 20V Wide Input Voltage Range LDO Linear Regulator

The RAA214250 is a low-dropout linear voltage regulator that operates from 2.5V to 20V and provide up to 500mA of output current with a typical dropout of 269mV. The output voltage is adjustable with external feedback resistors anywhere from 1.224V to 18V.

The ground current is typically 68µA at no-load and drops to 2.4µA typical when in shutdown making it great for battery powered and USB devices.

The LDO features excellent line and load regulation, input UVLO with hysteresis, enable control, short-circuit current limit with foldback, and over-temperature shutdown protection with hysteresis.

The LDO is stable with a minimum 2.2µF MLCC output capacitor and is available in 8 Ld 3mm×3mm DFN or a 8 Ld SOIC package.

Features

- Wide input voltage range: 2.5V to 20V
- Maximum output current: 500mA
- Low dropout voltage: 269mV typical at 500mA
- Low ground current
- Output voltage adjustable: 1.224V to 18V
- Excellent line and load regulation
- Stable with 1µF - 200µF MLCC output capacitor
- Short-circuit current limit with foldback
- Over-temperature shutdown protection
- 8 Ld DFN (3mm×3mm) and SOIC package

Applications

- Battery-powered equipment
- MCU power supply
- Electric meters
- USB devices
- Laptop computers and tablets
- Portable modules and appliances

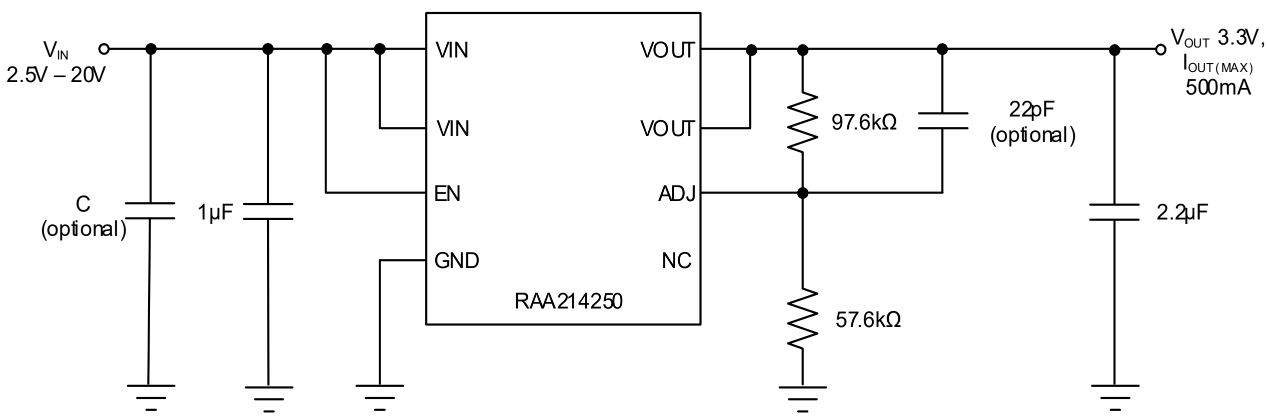


Figure 1. Typical Application Circuit

Contents

1. Overview

1.1 Block Diagram

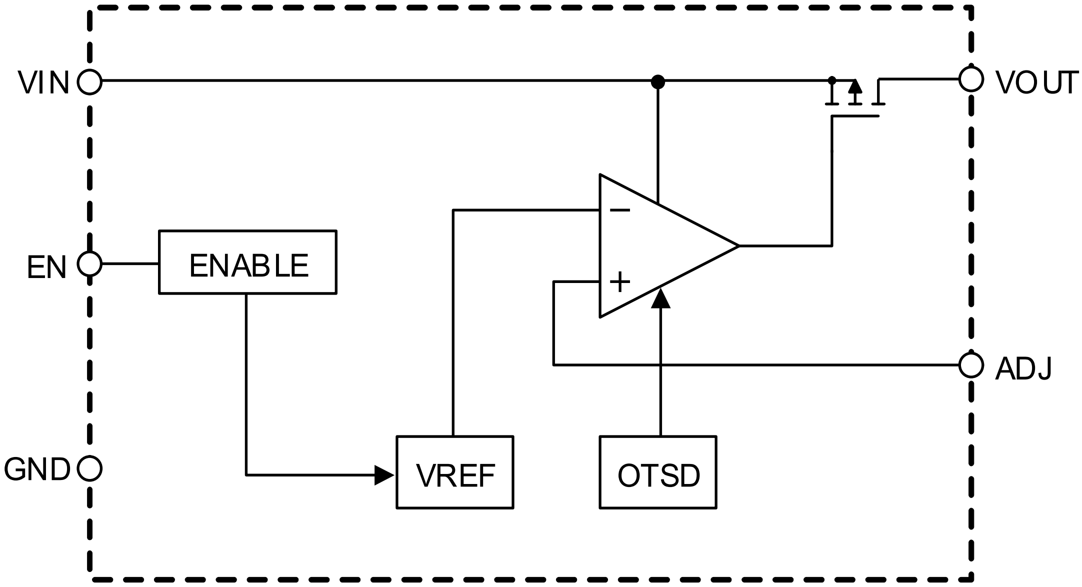
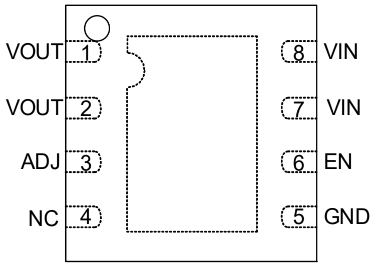


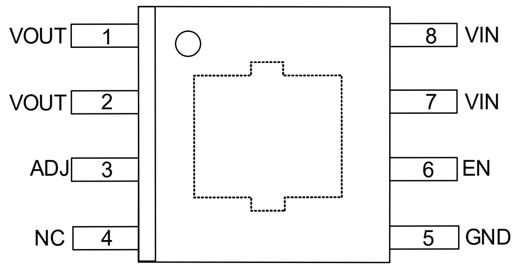
Figure 2. RAA214250 Block Diagram

2. Pin Information

2.1 Pin Assignments



3mm×3mm DFN
Top View



SOIC
Top View

2.2 Pin Descriptions

Pin Name	Pin Number	Description
VOUT	1, 2	VOUT are the regulated output voltage pins that supply power to the load. For stable operation across the full temperature range, input range, output range, and load extremes, a minimum 2.2µF X5R/X7R output capacitor is required between this pin and GND.
ADJ	3	ADJ is the adjustable pin. The ADJ pin is internally set to 1.224V via the band-gap circuitry. The external voltage divider formed around this pin sets the LDO output voltage. When the pin is shorted to VOUT, the output voltage is set to the minimum 1.224V. See Adjusting the Output Voltage for more information on setting the output voltage.
GND	5	GND is the ground pin. This pin must be tied to GND.
EN	6	EN is the ENABLE input. Setting this pin LOW turns OFF the LDO and setting it HIGH turns ON the LDO. **IMPORTANT:** This pin should not be left floating. Instead tie it to the VIN pins for automatic enabling.
VIN	7, 8	VIN are the input voltage pins that supply power to the LDO. Renesas recommends placing a 10µF and 1µF input capacitor from this pin to GND. Place the 1µF as close as possible to the VIN pins.
EPAD		EPAD is the exposed pad on the bottom of the package. To ensure proper electrical and thermal performance, solder the exposed pad to the PCB ground plane and tie it directly to the ground Pin 5. See Layout Guidelines for more layout guidelines for this pin.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Parameter[1]	Minimum	Maximum	Unit
Supply Voltage, VIN	-0.3	+22	V
Enable Input Voltage, EN	-0.3	+22	V
Output Voltage, VOUT	-0.3	+22	V
Adjustable Pin Voltage, ADJ	-0.3	+6	V
Output Current, IOUT	-	500	mA
Maximum Junction Temperature	-40	+125	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2017)	-	2	kV
Charged Device Model (Tested per JS-002-2018)	-	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

1. All voltages referenced to VSS unless otherwise specified.

3.2 Thermal Information

Thermal Resistance (Typical)[1]	θ_{JA} (°C/W)[2]	θ_{JC} (°C/W)[3]
8 Ld EPSOIC	58	16
8 Ld DFN 3×3	56	14

1. Specified at published junction to ambient thermal resistance for a junction temperature of +150°C. See [2] for test conditions to establish junction to ambient thermal resistance.
2. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
3. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.3 Recommended Operating Conditions

Parameter[1]	Minimum	Maximum	Units
Supply Voltage, V_{IN}	+2.5	+20	V
Enable Input Voltage, EN	0	+20	V
Output Voltage, V_{OUT}	0	+18	V
Adjustable Pin Voltage, ADJ	0	+5	V
Output Current, I_{OUT}	0	500	mA
Output Capacitor, C_{OUT}	1	200	µF
Junction Temperature	-40	+125	°C

1. All voltages referenced to VSS unless otherwise specified.

3.4 Electrical Specifications

I_{OUT} = 1mA, C_{OUT} = 2.2µF, C_{IN} = 10µF, V_{IN} = 2.5V, V_{OUT} = V_{ADJ}, V_{EN} = 5V unless otherwise specified. Typical values are at T_A = 25C. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

Parameters	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Output Voltage	V_{OUT}		**1.2**		**18**	V
Input Voltage	V_{IN}		**2.5**		**20**	V
Reference Voltage Accuracy	V_{REF}	V_{IN} = 2.5V to 20V, T = 25°C	-1.7		+1.7	%
		T = -40°C to 125°C	**-2**		**+2**	%
Reference Voltage	V_{REF}			1.224		V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = V_{OUT}+1V to 20V		0.02	**0.05**	%/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{IN} = 5V, I_{OUT} = 100µA to 500mA		0.0002		%/mA
Dropout Voltage[2]	V_{DO}	I_{OUT} = 10mA, V_{OUT} = 3.3V		5		mV
		I_{OUT} = 50mA, V_{OUT} = 3.3V		25		mV
		I_{OUT} = 500mA, V_{OUT} = 3.3V		269	**450**	mV
Shutdown Current	I_{SHDN}	V_{EN} = 0, V_{IN} = 2.5V		2.4		µA
		V_{EN} = 0, V_{IN} = 20V		5.8	**13**	µA
Ground Current	I_{GND}	I_{OUT} = 0mA, V_{IN} = 2.5V, V_{EN} = 5V		68		µA
		I_{OUT} = 10mA, V_{IN} = 2.5V, V_{EN} = 5V		104		µA
		I_{OUT} = 50mA, V_{IN} = 2.5V, V_{EN} = 5V		110		µA
		I_{OUT} = 500mA, V_{IN} = 2.5V, V_{EN} = 5V		140	**225**	µA
Power Supply Rejection Ratio	PSRR	FREQ = 100Hz, V_{RIPPLE} = 1V_{P-P}, I_{OUT} = 50mA, V_{IN} = 6V, V_{OUT} = 5V		87		dB
		FREQ = 10kHz, $V_{RIPPLE = 200mVP-P}$, I_{OUT} = 50mA, V_{IN} = 6V, V_{OUT} = 5V		63		dB
Output Voltage Noise		BW = 10Hz to 100kHz, I_{OUT} = 10mA, C_{OUT} = 10µF		167		μV_{RMS}
EN Rising Threshold			**1.35**	1.5	**1.65**	V
EN Falling Threshold				1.3		V
EN Leakage Current		V_{EN} = 20V		0.83		uA
VIN UVLO Rising Threshold				2.08		V
VIN UVLO Hysteresis				220		mV
Short Circuit Current Limit		No Foldback	**550**			mA
		With Foldback, V_{IN} - V_{OUT} = 10V	**550**			mA
		With Foldback, V_{IN} - V_{OUT} = 18V	**240**		**600**	mA
Thermal Shutdown				150		°C
Hysteresis				20		°C

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its normal value.

4. Typical Performance Graphs

4.1 Load Transient

C_{IN} = 10µF, unless otherwise stated.

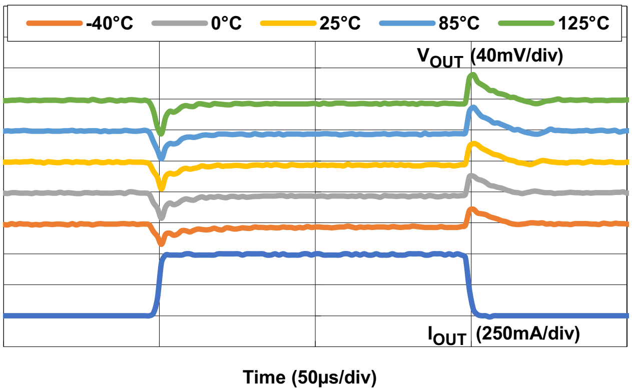


Figure 3. Load Transient Response for Various Junction Temperatures (V_{IN} = 2.5V, V_{OUT} = V_{ADJ}, C_{OUT} = 4.7µF, C_{FF} = None, ΔI_{OUT} = 1mA to 500mA at 100mA/µs)

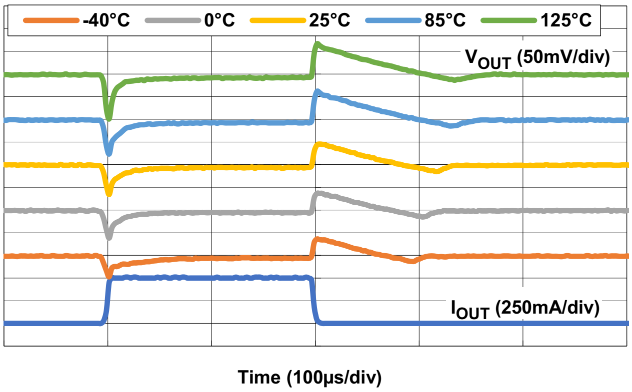


Figure 4. Load Transient Response for Various Junction Temperatures (V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 2.2µF, C_{FF} = 22pF, ΔI_{OUT} = 1mA to 500mA at 100mA/µs)

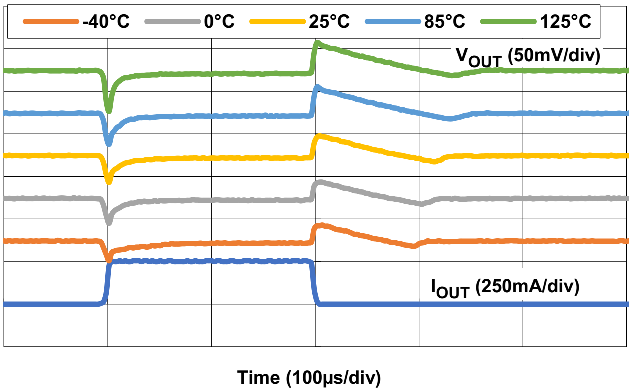


Figure 5. Load Transient Response for Various Junction Temperatures (V_{IN} = 5V, V_{OUT} = 3.3V, C_{OUT} = 2.2µF, C_{FF} = 22pF, ΔIOUT = 1mA to 500mA at 100mA/µs)

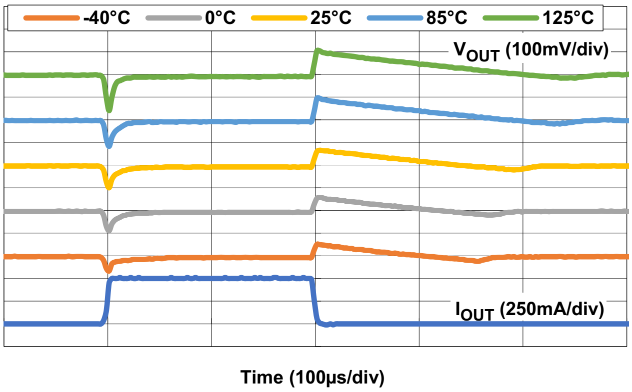


Figure 6. Load Transient Response for Various Junction Temperatures (V_{IN} = 6V, V_{OUT} = 5V, C_{OUT} = 2.2µF, C_{FF} = 15pF, ΔI_{OUT} = 1mA to 500mA at 100mA/µs)

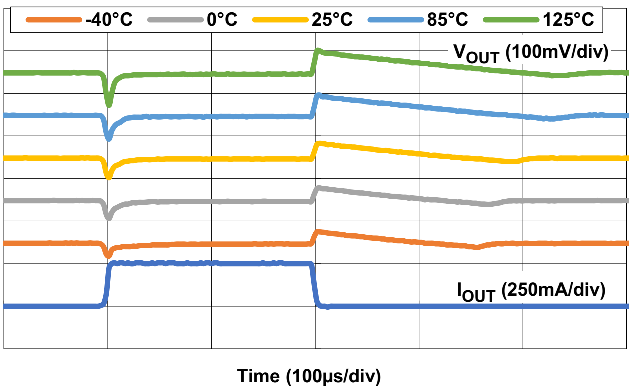


Figure 7. Load Transient Response for Various Junction Temperatures (V_{IN} = 7V, V_{OUT} = 5V, C_{OUT} = 2.2µF, C_{FF} = 15pF, ΔI_{OUT} = 1mA to 500mA at 100mA/µs)

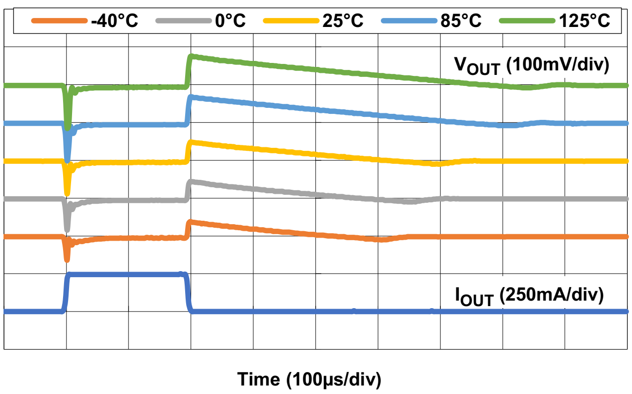


Figure 8. Load Transient Response for various Junction Temperatures (V_{IN} = 13V, V_{OUT} = 12V, C_{OUT} = 2.2µF, C_{FF} = None, ΔI_{OUT} = 1mA to 500mA at 100mA/µs)

C_{IN} = 10µF, unless otherwise stated. (Cont.)

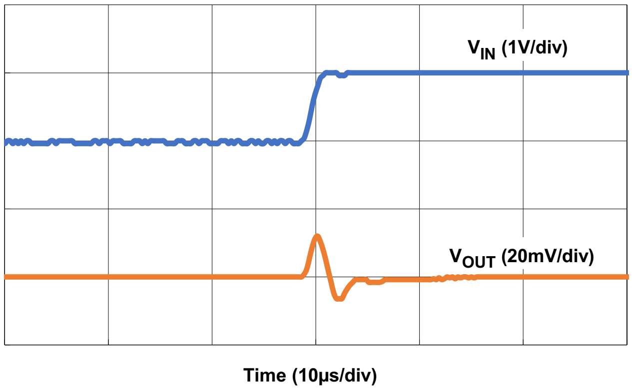


Figure 9. Line Transient Response (ΔV_{IN} = 4V to 5V in 1V/µs, V_{OUT} = V_{ADJ}, I_{OUT} = 500mA, C_{FF} = None, C_{OUT} = 2.2µF)

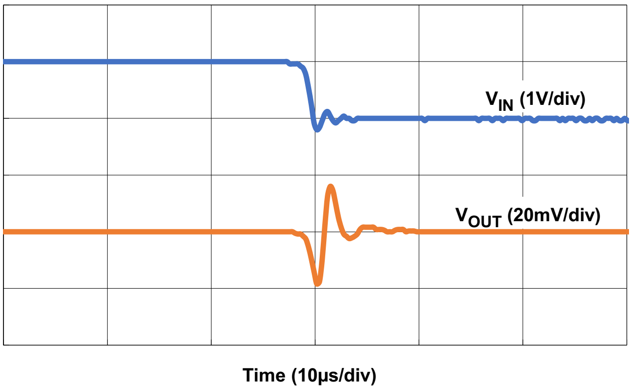


Figure 10. Line Transient Response (ΔV_{IN} = 5V to 4V in 1V/µs, V_{OUT} = V_{ADJ}, I_{OUT} = 500mA, C_{FF} = None, C_{OUT} = 2.2µF)

4.2 Dropout Voltage

C_{IN} = 10µF, unless otherwise stated.

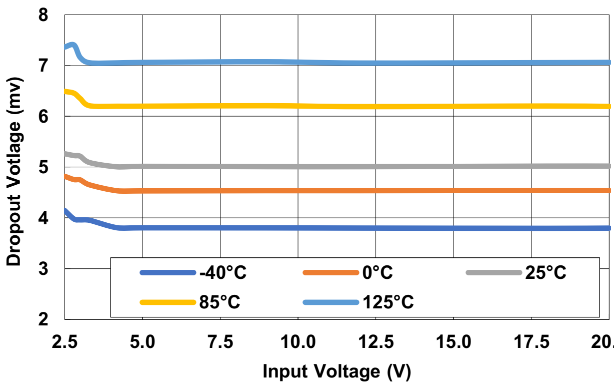


Figure 11. Dropout Voltage vs Input Voltage for Various Junction Temperatures (I_{OUT} = 10mA)

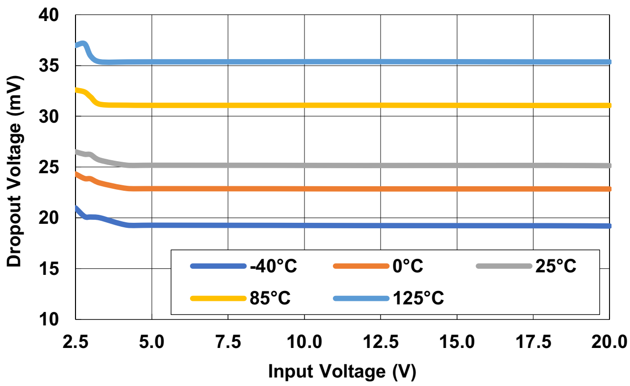


Figure 12. Dropout Voltage vs Input Voltage for Various Junction Temperatures (I_{OUT} = 50mA)

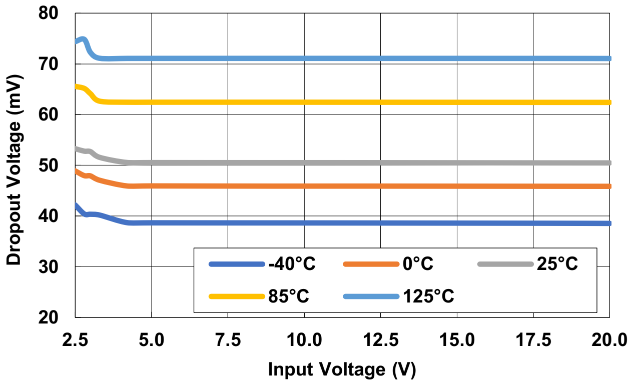


Figure 13. Dropout Voltage vs Input Voltage for Various Junction Temperatures (I_{OUT} = 100mA)

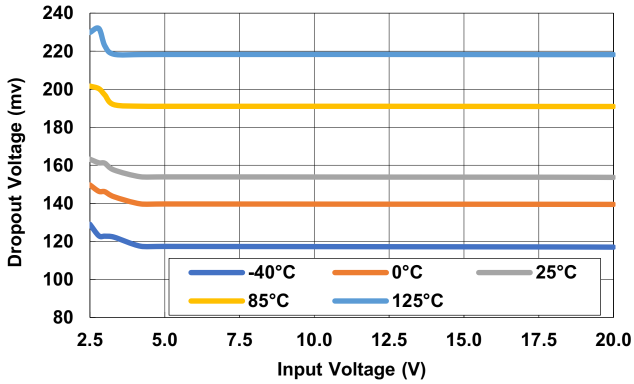


Figure 14. Dropout Voltage vs Input Voltage for Various Junction Temperatures (I_{OUT} = 300mA)

C_{IN} = 10µF, unless otherwise stated. (Cont.)

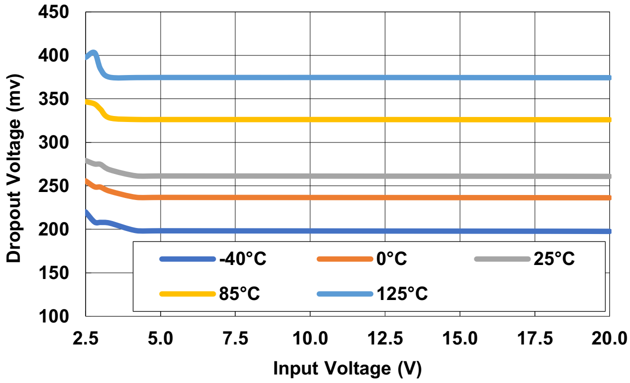


Figure 15. Dropout Voltage vs Input Voltage for Various Junction Temperatures (I_{OUT} = 500mA)

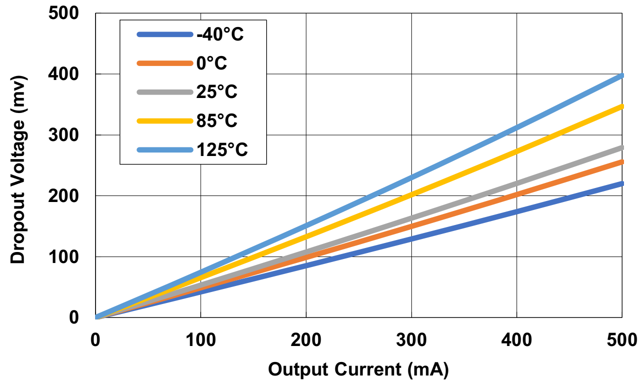


Figure 16. Dropout Voltage vs Output Current for Various Junction Temperatures (V_{IN} = 2.5V)

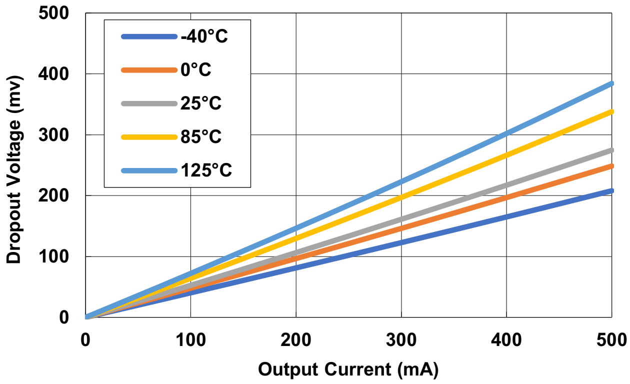


Figure 17. Dropout Voltage vs Output Current for Various Junction Temperatures (V_{IN} = 3V)

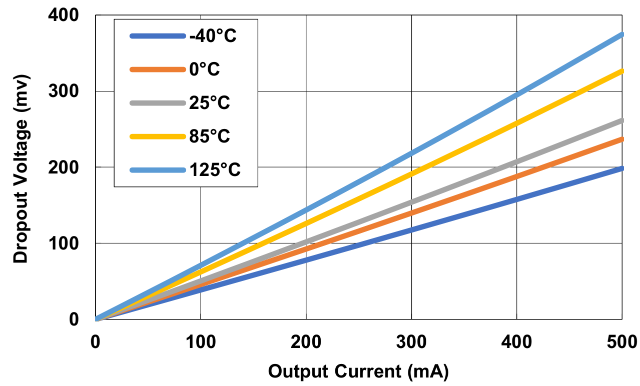


Figure 18. Dropout Voltage vs Output Current for Various Junction Temperatures (V_{IN} = 4.2V)

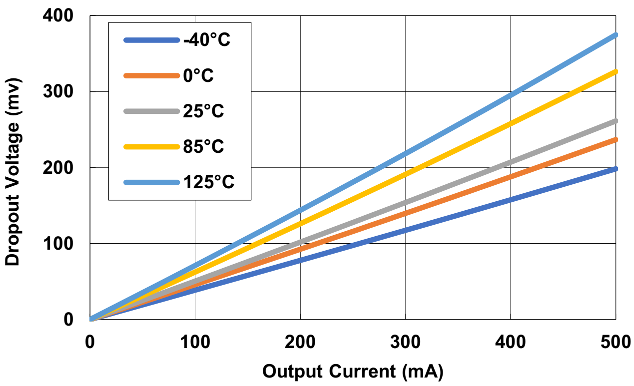


Figure 19. Dropout Voltage vs Output Current for Various Junction Temperatures (V_{IN} = 5V)

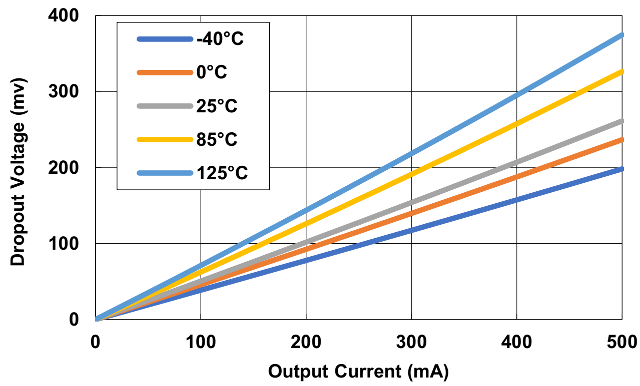


Figure 20. Dropout Voltage vs Output Current for Various Junction Temperatures (V_{IN} = 9V)

C_{IN} = 10µF, unless otherwise stated. (Cont.)

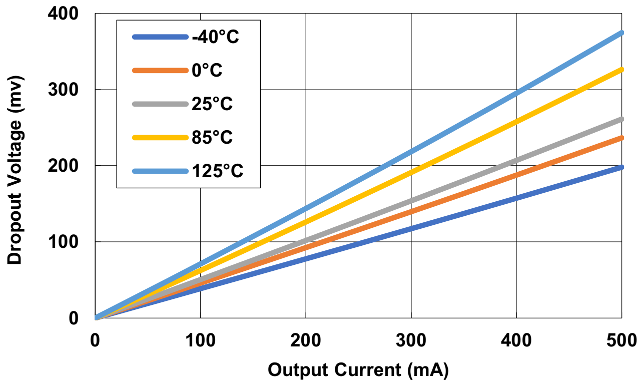


Figure 21. Dropout Voltage vs Output Current for Various Junction Temperatures (V_{IN} = 12V)

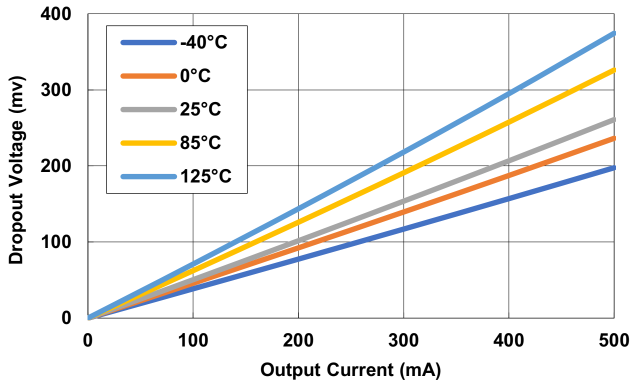


Figure 22. Dropout Voltage vs Output Current for Various Junction Temperatures (V_{IN} = 20V)

4.3 Start-Up

C_{IN} = 10µF, unless otherwise stated.

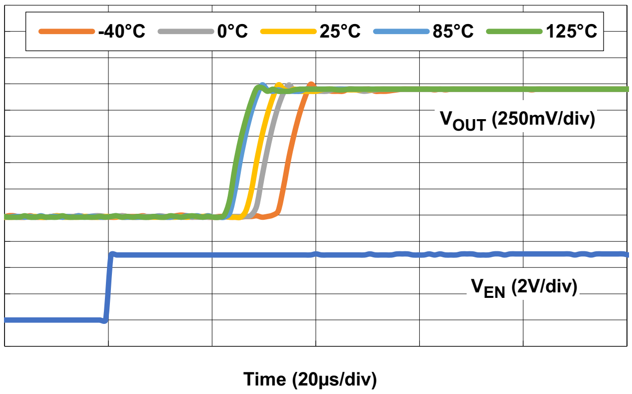


Figure 23. Start-Up Time for Various Junction Temperatures (V_{IN} = 2.5V, V_{OUT} = V_{ADJ}, I_{OUT} = 500mA, C_{FF} = None, C_{OUT} = 2.2µF)

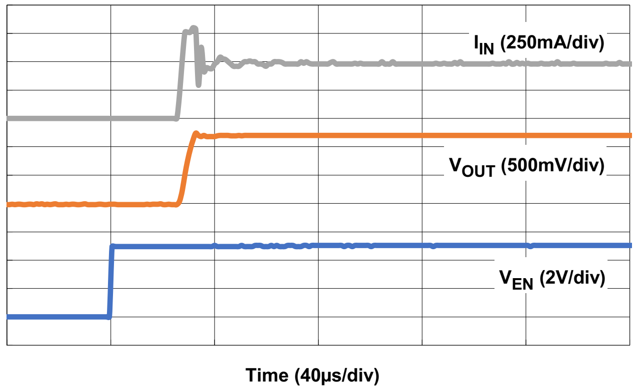


Figure 24. Start-Up and In-Rush Current (V_{IN} = 2.5V, V_{OUT} = V_{ADJ}, I_{OUT} = 500mA, C_{FF} = None, C_{OUT} = 2.2µF)

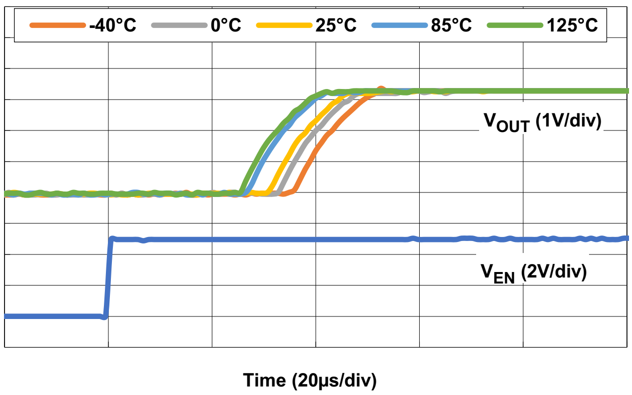


Figure 25. Start-Up Time for Various Junction Temperatures (V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 500mA, C_{FF} = 22pF, C_{OUT} = 2.2µF)

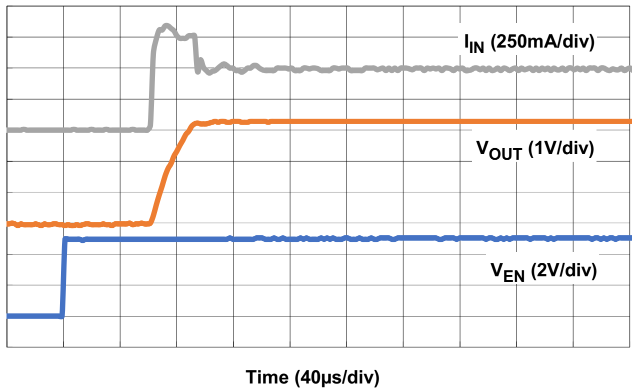


Figure 26. Start-Up and In-Rush Current (V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 500mA, C_{FF} = 22pF, C_{OUT} = 2.2µF)

C_{IN} = 10µF, unless otherwise stated. (Cont.)

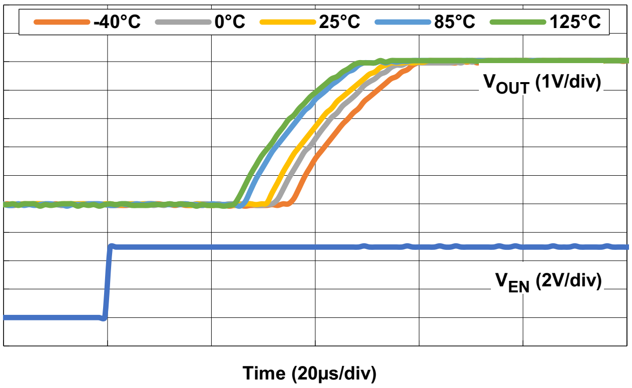


Figure 27. Start-Up Time for Various Junction Temperatures (V_{IN} = 6V, V_{OUT} = 5V, I_{OUT} = 500mA, C_{FF} = 15pF, C_{OUT} = 2.2µF)

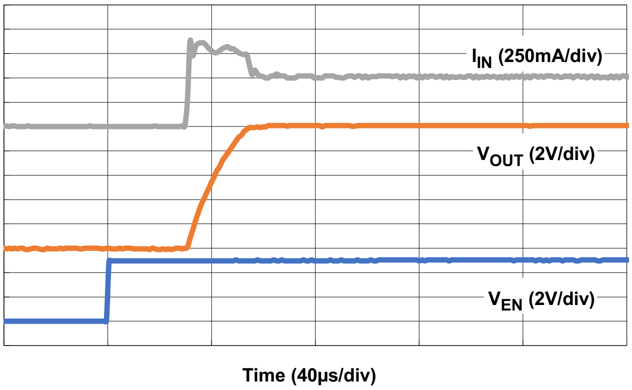


Figure 28. Start-Up and In-Rush Current (V_{IN} = 6V, V_{OUT} = 5V, I_{OUT} = 500mA, C_{FF} = 15pF, C_{OUT} = 2.2µF)

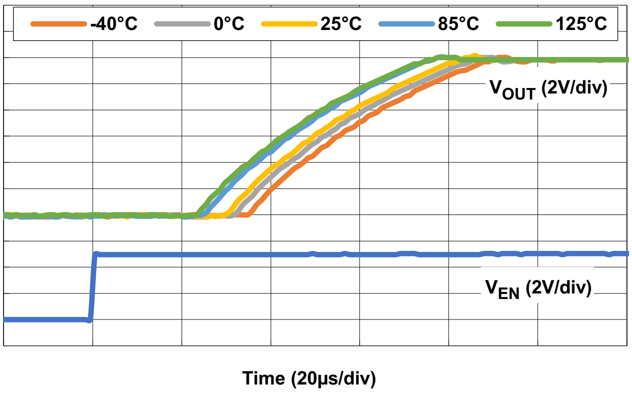


Figure 29. Start-Up Time for Various Junction Temperatures (V_{IN} = 13V, V_{OUT} = 12V, I_{OUT} = 500mA, C_{FF} = 0pF, C_{OUT} = 2.2µF)

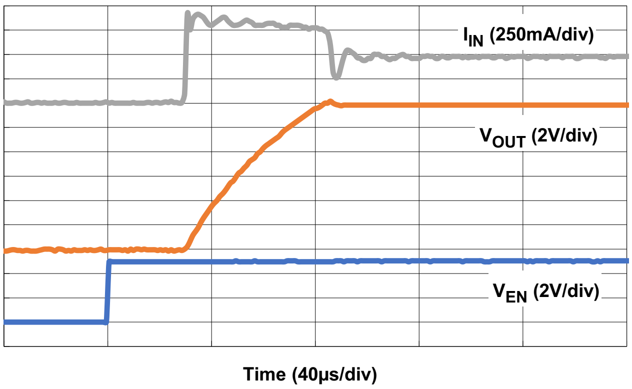


Figure 30. Start-Up and In-Rush Current (V_{IN} = 13V, V_{OUT} = 12V, I_{OUT} = 500mA, C_{FF} = 0pF, C_{OUT} = 2.2µF)

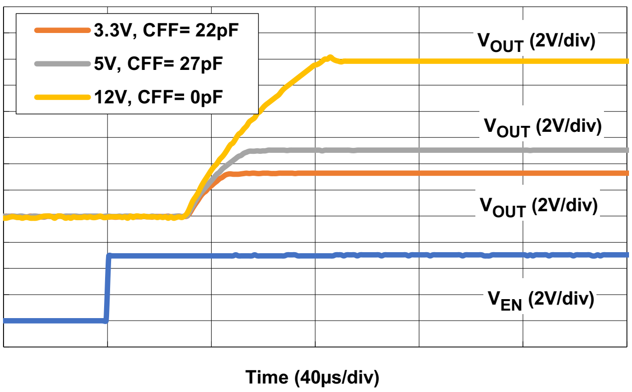


Figure 31. Start-Up Time for Various Output Voltages (V_{IN} = V_{OUT} + 1V, I_{OUT} = 500mA, C_{OUT} = 2.2µF)

4.4 General Performance

C_{IN} = 10µF, unless otherwise stated.

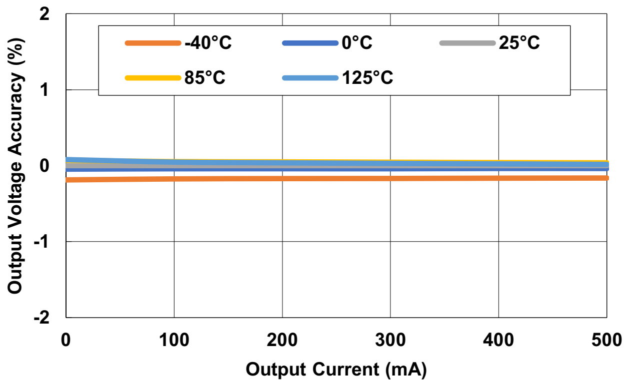


Figure 32. Output Voltage vs Output Current for Various Junction Temperatures (V_{IN} = 2.5V, V_{OUT} = V_{ADJ})

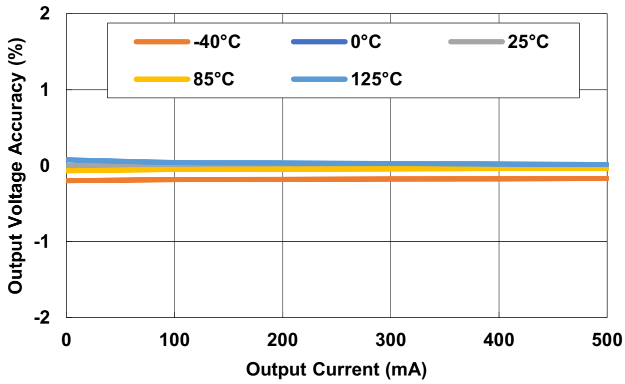


Figure 33. Output Voltage vs Output Current for Various Junction Temperatures (V_{IN} = 5V, V_{OUT} = V_{ADJ})

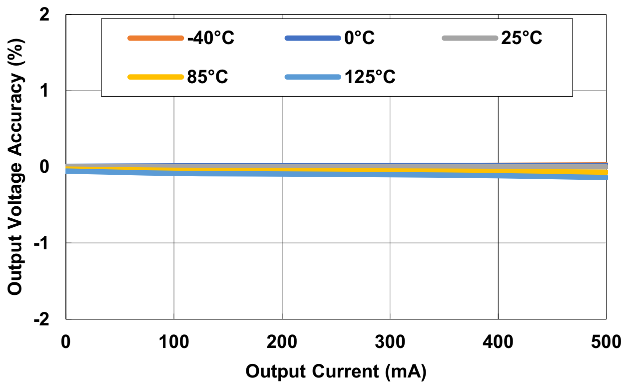


Figure 34. Output Voltage vs Output Current for Various Junction Temperatures (V_{IN} = 3.8V, V_{OUT} = 3.3V)

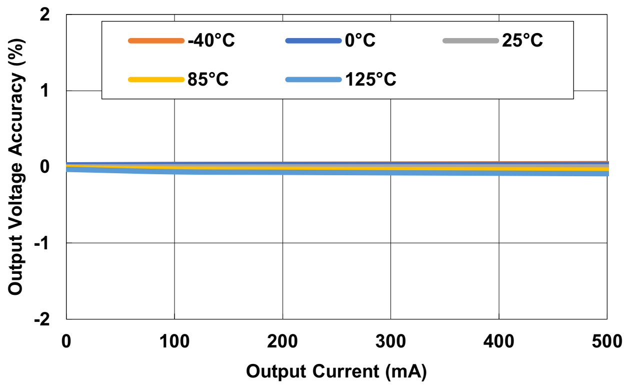


Figure 35. Output Voltage vs Output Current for Various Junction Temperatures (V_{IN} = 4.3V, V_{OUT} = 3.3V)

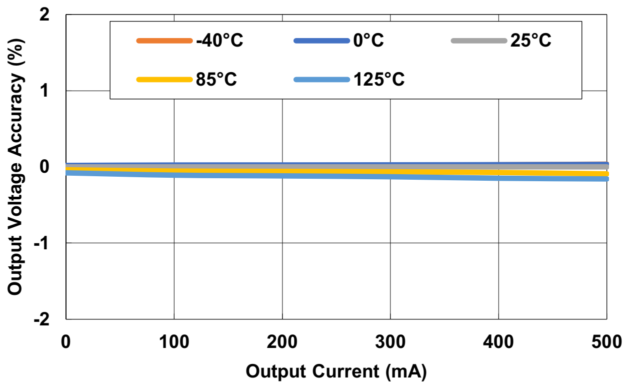


Figure 36. Output Voltage vs Output Current for Various Junction Temperatures (V_{IN} = 5.5V, V_{OUT} = 5V)

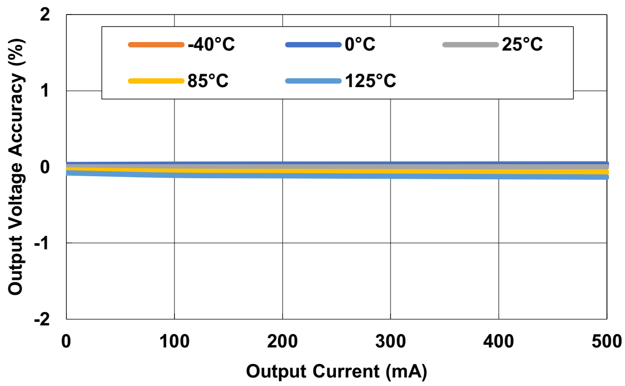


Figure 37. Output Voltage vs Output Current for Various Junction Temperatures (V_{IN} = 6V, V_{OUT} = 5V)

C_{IN} = 10µF, unless otherwise stated. (Cont.)

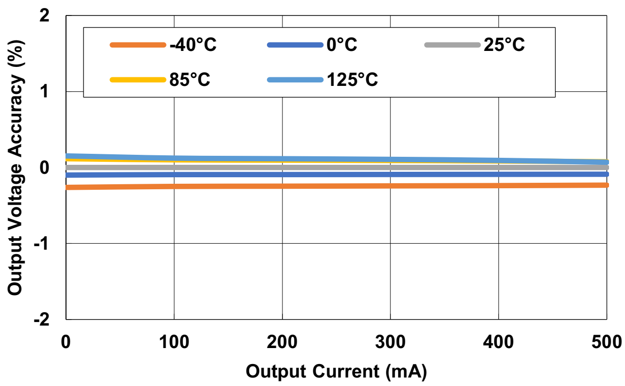


Figure 38. Output Voltage vs Output Current for Various Junction Temperatures (V_{IN} = 12.5V, V_{OUT} = 12V)

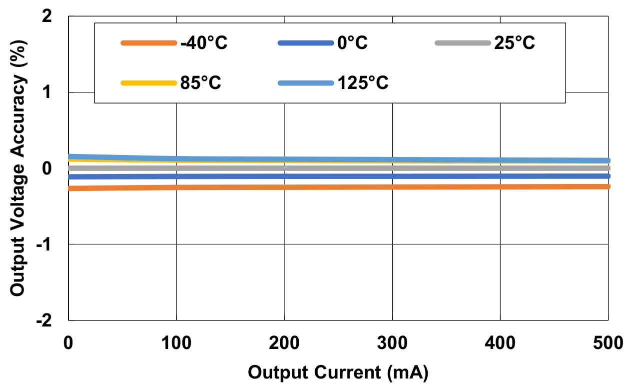


Figure 39. Output Voltage vs Output Current for Various Junction Temperatures (V_{IN} = 13V, V_{OUT} = 12V)

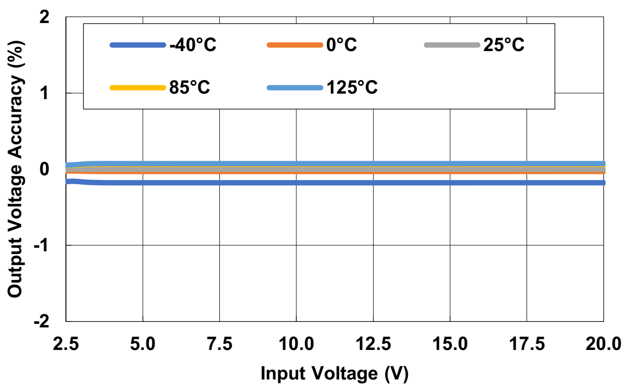


Figure 40. Output Voltage vs Input Voltage for Various Junction Temperatures (V_{OUT} = V_{ADJ}, I_{OUT} = 1mA)

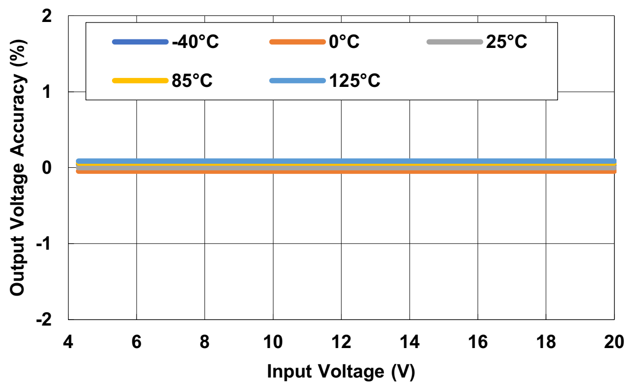


Figure 41. Output Voltage vs Input Voltage for Various Junction Temperatures (V_{OUT} = 3.3V, I_{OUT} = 1mA)

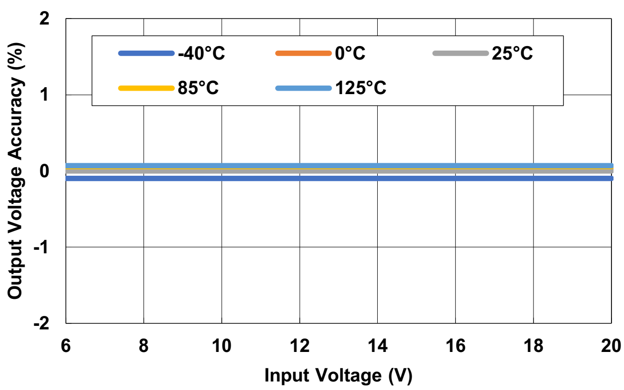


Figure 42. Output Voltage vs Input Voltage for Various Junction Temperatures (V_{OUT} = 5V, I_{OUT} = 1mA)

C_{IN} = 10µF, unless otherwise stated. (Cont.)

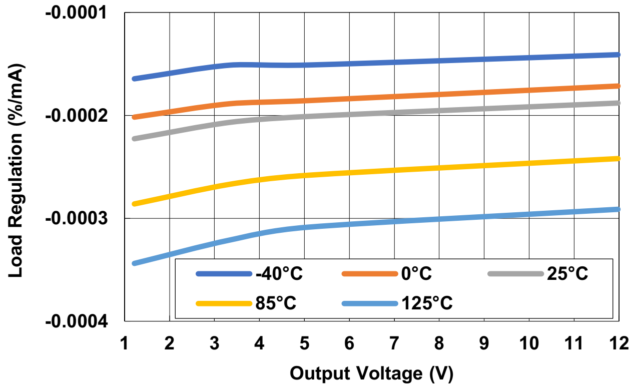


Figure 43. Load Regulation vs Output Voltage (V_{IN} = V_{OUT} + 1V, ΔI_{OUT} = 100µA to 500mA)

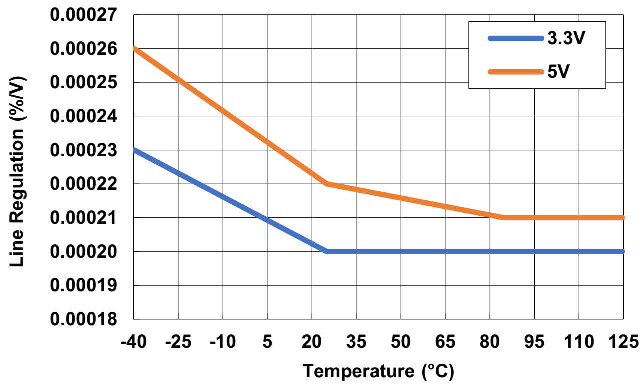


Figure 44. Line Regulation vs Temperature for Various V_{OUT} (ΔV_{IN} = V_{OUT} + 1V to 20V, I_{OUT} = 1mA)

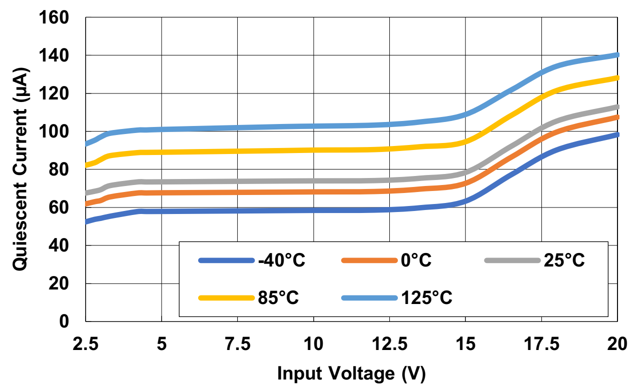


Figure 45. Quiescent Current vs Input Voltage for Various Junction Temperatures (V_{OUT} = V_{ADJ}, I_{OUT} = 0A)

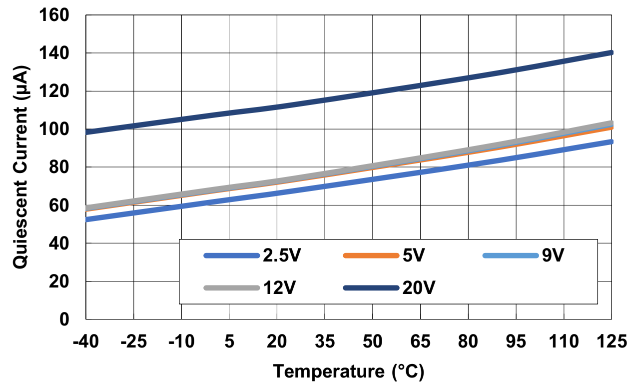


Figure 46. Quiescent Current vs Junction Temperature for Various Input Voltages (V_{OUT} = V_{ADJ}, I_{OUT} = 0A)

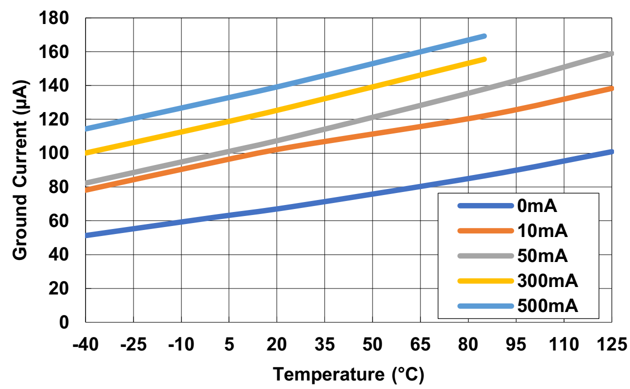


Figure 47. Ground Current vs Junction Temperature for Various I_{OUT} (V_{IN} = 2.5V, V_{EN} = 5V, V_{OUT} = V_{ADJ})

Note: Power dissipation limited to 250mW at 125°C, 750mW at 85°C and 2W at 25°C, 0°C, and -40°C.

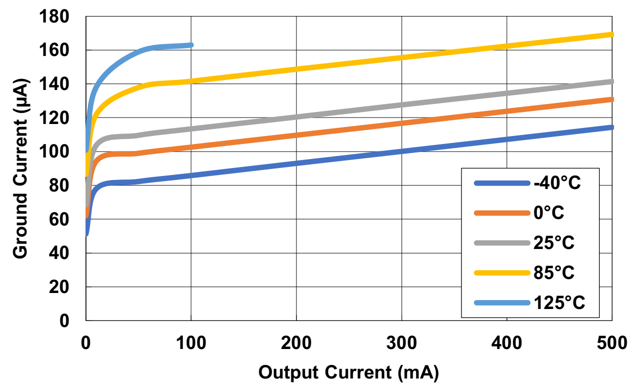


Figure 48. Ground Current vs Output Current for Various Junction Temperatures (V_{IN} = 2.5V, V_{EN} = 5V, V_{OUT} = V_{ADJ})

Note: Power dissipation limited to 250mW at 125°C, 750mW at 85°C and 2W at 25°C, 0°C, and -40°C.

C_{IN} = 10µF, unless otherwise stated. (Cont.)

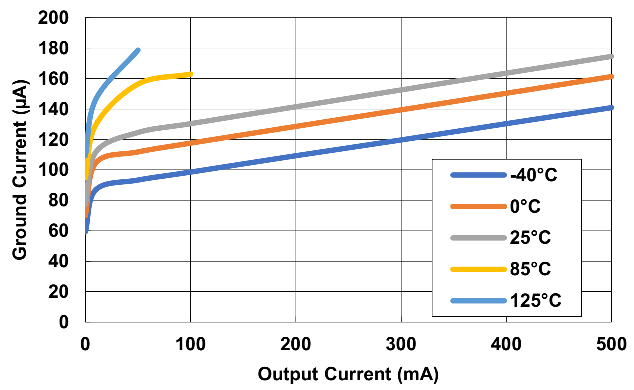


Figure 49. Ground Current vs Output Current for Various Junction Temperatures (V_{IN} = 5V, V_{EN} = 5V, V_{OUT} = V_{ADJ})

Note: Power dissipation limited to 250mW at 125°C, 750mW at 85°C and 2W at 25°C, 0°C, and -40°C.

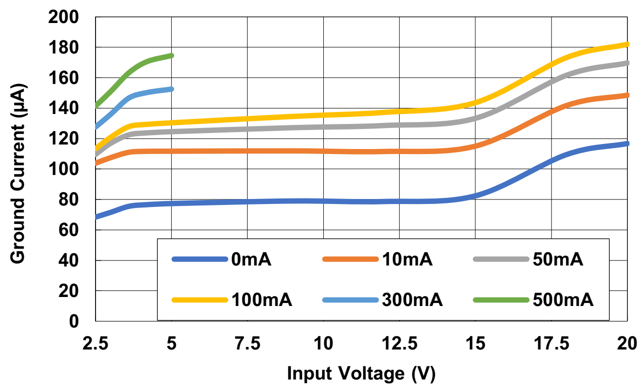


Figure 50. Ground Current vs Input Voltage for Various I_{OUT} (V_{EN} = 5V, V_{OUT} = V_{ADJ})

Note: Power dissipation limited to 250mW at 125°C, 750mW at 85°C and 2W at 25°C, 0°C, and -40°C.

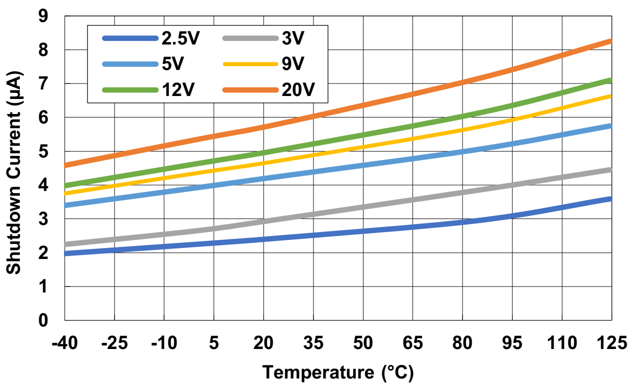


Figure 51. Shutdown Current vs Junction Temperature for Various Input Voltages (V_{EN} = 0V)

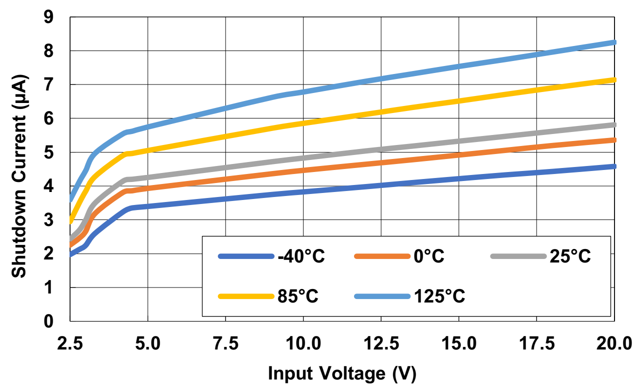


Figure 52. Shutdown Current vs Input Voltage for Various Junction Temperatures (V_{EN} = 0V)

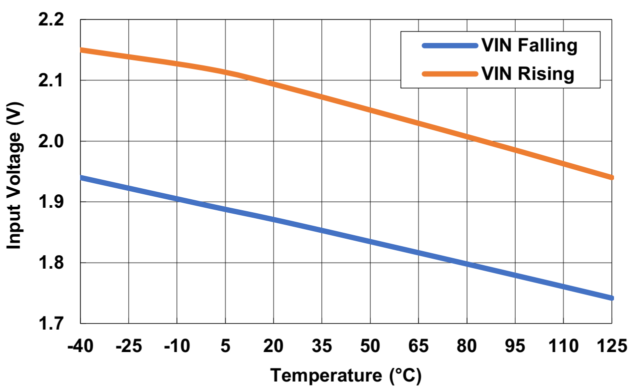


Figure 53. Input Voltage UVLO Thresholds vs Junction Temperature

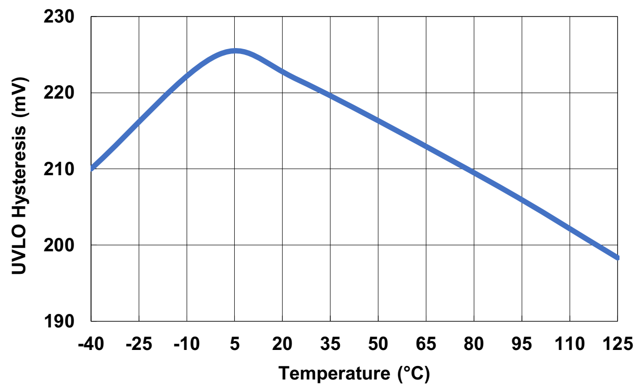


Figure 54. Input Voltage UVLO Hysteresis vs Junction Temperature

C_{IN} = 10µF, unless otherwise stated. (Cont.)

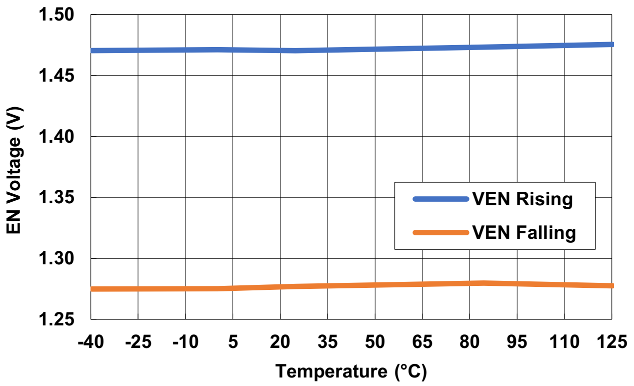


Figure 55. EN Voltage Thresholds vs Junction Temperature (V_{IN} = 2.5V)

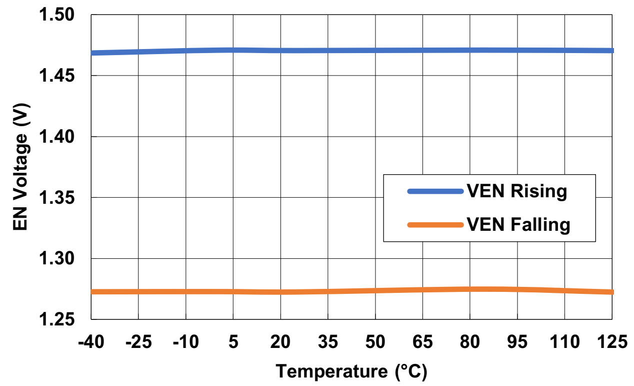


Figure 56. EN Voltage Thresholds vs Junction Temperature (V_{IN} = 20V)

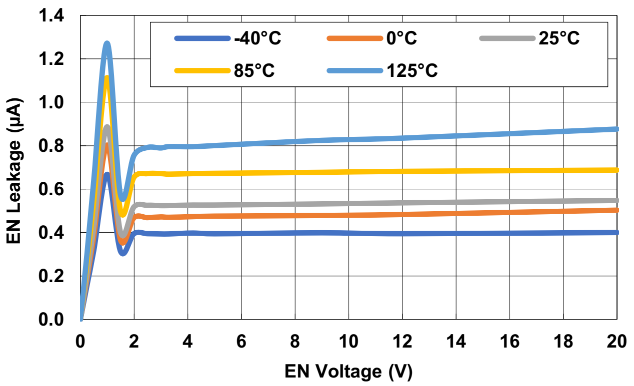


Figure 57. EN Leakage vs EN Voltage for Various Junction Temperatures (V_{IN} = 2.5V)

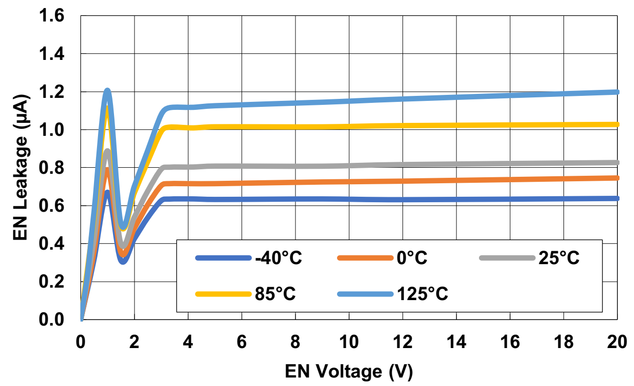


Figure 58. EN Leakage vs EN Voltage for Various Junction Temperatures (V_{IN} = 20V)

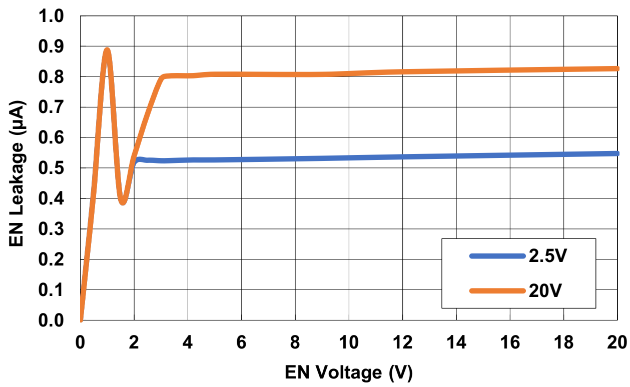


Figure 59. EN Leakage vs EN Voltage for Various Input Voltages

C_{IN} = 10µF, unless otherwise stated. (Cont.)

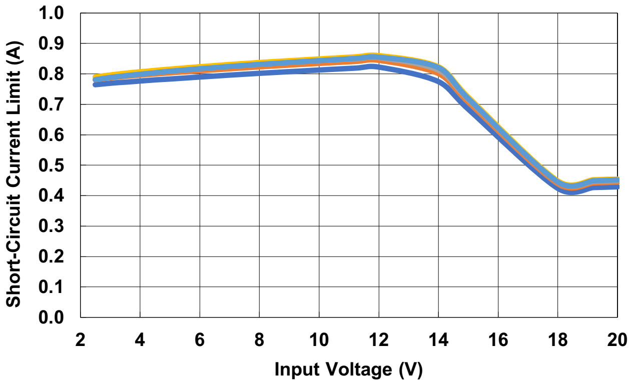


Figure 60. Short-Circuit Current Limit vs Input Voltage for Various Junction Temperatures (V_{OUT} = V_{ADJ})

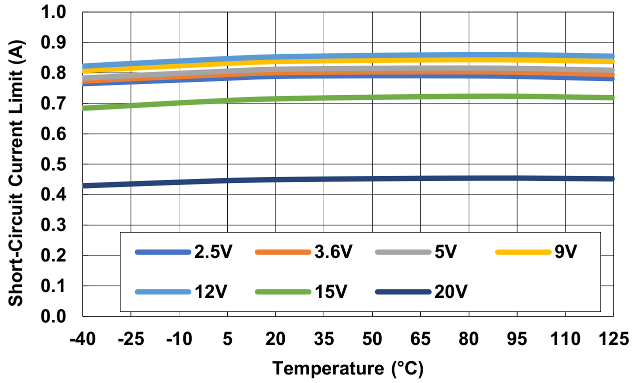


Figure 61. Short-Circuit Current Limit vs Junction Temperature for Various Input Voltages (V_{OUT} = V_{ADJ})

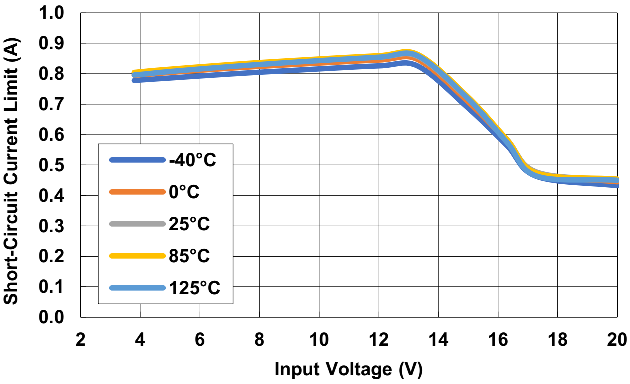


Figure 62. Short-Circuit Current Limit vs Input Voltage for Various Junction Temperatures (V_{OUT} = 3.3V)

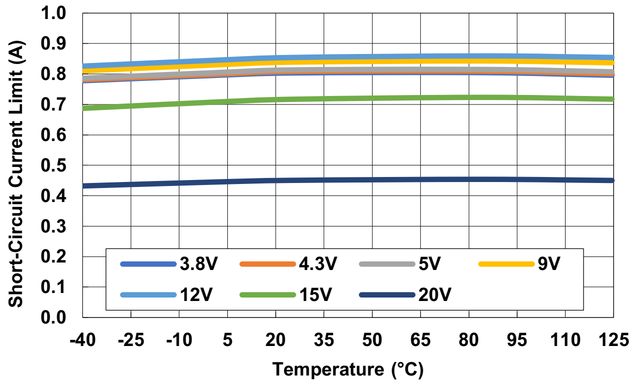


Figure 63. Short-Circuit Current Limit vs Junction Temperature for Various Input Voltages (V_{OUT} = 3.3V)

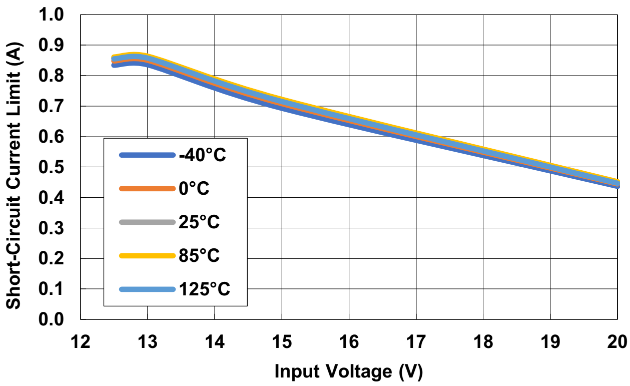


Figure 64. Short-Circuit Current Limit vs Input Voltage for Various Junction Temperatures (V_{OUT} = 12V)

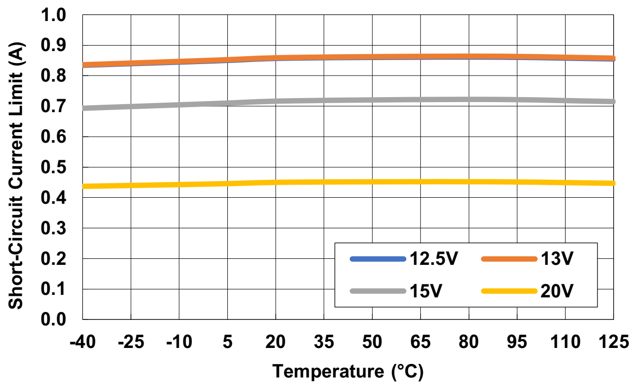


Figure 65. Short-Circuit Current Limit vs Junction Temperature for Various Input Voltages (V_{OUT} = 12V)

4.5 Output Noise and PSRR

C_{IN} = 10µF, unless otherwise stated.

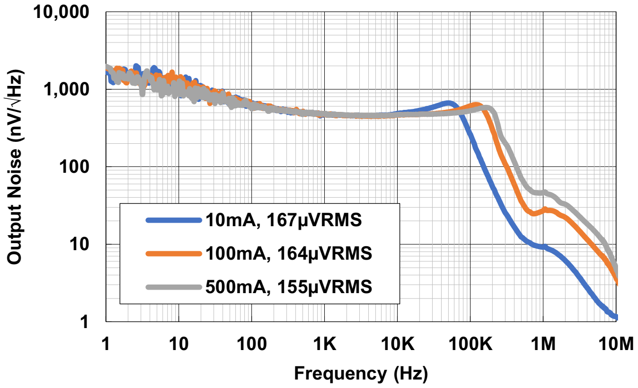


Figure 66. Output Noise vs Frequency for Various I_{OUT} (V_{IN} = 2.5V, V_{OUT} = V_{ADJ}, C_{OUT} = 10µF, C_{FF} = None)

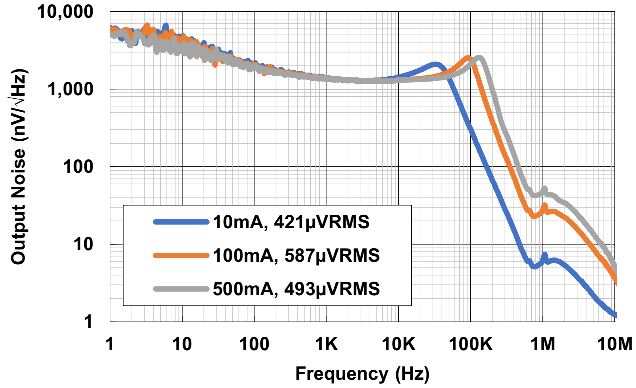


Figure 67. Output Noise vs Frequency for Various I_{OUT} (V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 10µF, C_{FF} = 0pF)

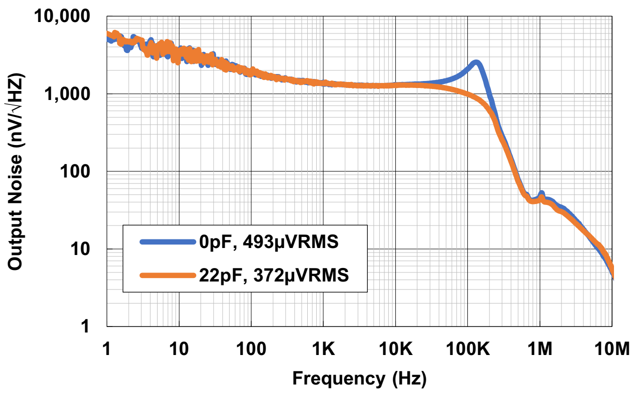


Figure 68. Output Noise vs Frequency for Various C_{FF} (V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 10µF, I_{OUT} = 500mA)

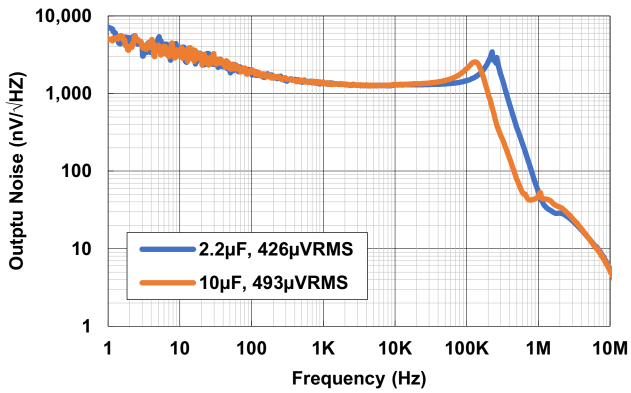


Figure 69. Output Noise vs Frequency for Various C_{OUT} (V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 500mA, C_{FF} = 0pF)

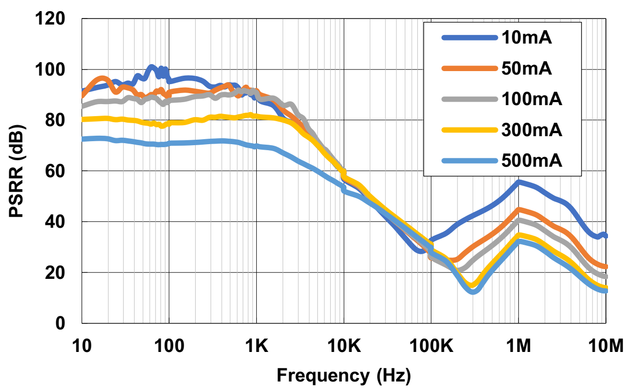


Figure 70. PSRR vs Frequency for Various Output Currents (V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{IN} = 0µF, C_{OUT} = 2.2µF, C_{FF} = 0pF)

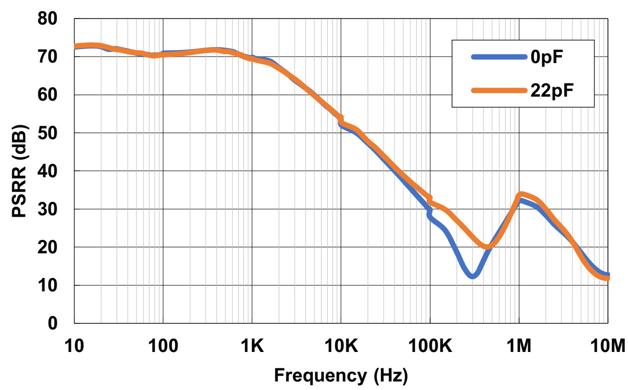


Figure 71. PSRR vs Frequency for Various C_{FF} (V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 500mA, C_{IN} = 0µF, C_{OUT} = 2.2µF)

C_{IN} = 10µF, unless otherwise stated. (Cont.)

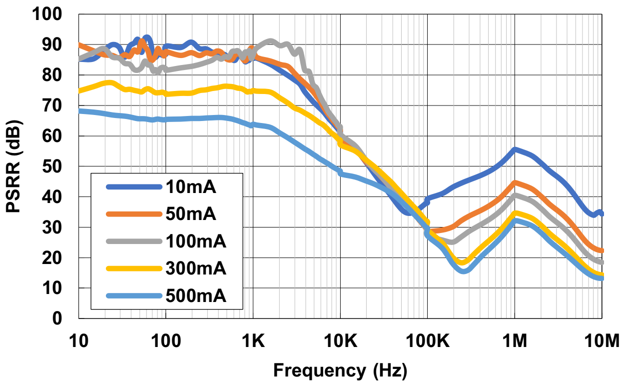


Figure 72. PSRR vs Frequency for Various Output Currents (V_{IN} = 6V, V_{OUT} = 5V, C_{IN} = 0µF, C_{OUT} = 2.2µF, C_{FF} = 0pF)

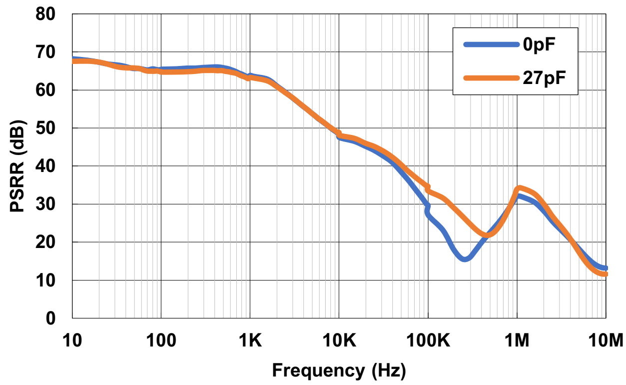


Figure 73. PSRR vs Frequency for Various C_{FF} (V_{IN} = 6V, V_{OUT} = 5V, I_{OUT} = 500mA, C_{IN} = 0µF, C_{OUT} = 2.2µF)

5. Application Information

5.1 Overview

The RAA214250 is a low-dropout (LDO) linear voltage regulator that operates from an input voltage of 2.5V to 20V while sourcing a maximum 500mA load. The output voltage is adjustable with external feedback resistors from 1.224V to 18V. It typically draws 68µA of ground current at no-load which drops to 2.4µA during shutdown.

The RAA214250 is designed and tested with a 2.2µF minimum output capacitor, and a 1µF input capacitor. The LDO is available in a 3×3mm 8 Ld DFN package or an 8 Ld EPSOIC.

The RAA214250 integrates the following additional features:

- Undervoltage Lockout (UVLO)
- Enable Control
- Short-Circuit Current Limit with Foldback
- Thermal Shutdown Protection

5.2 Theory of Operation of PMOS LDOs

Like the majority of LDOs with a PMOS pass transistor, the RAA214250 DC output voltage (V_{OUT}) regulation can be a modeled with a voltage reference (V_{REF}), PMOS pass-transistor, error amplifier and feedback (FB) resistors as shown in Figure 74.

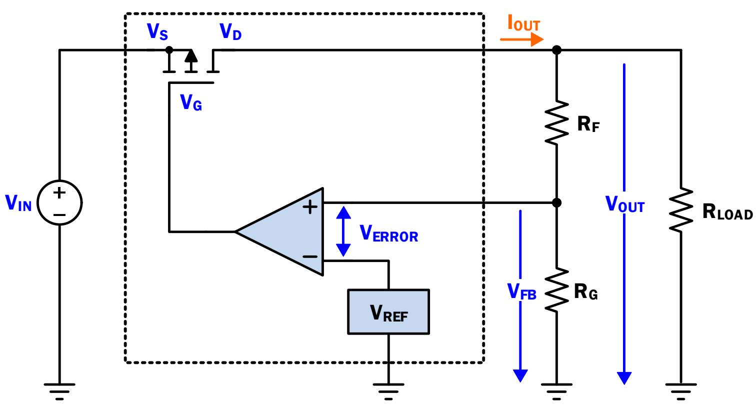


Figure 74. Simple PMOS LDO Regulator Block Diagram

The PMOS pass transistor can be modeled as a variable resistor ($r_{DS(ON)}$) that is controlled by the error amplifier to maintain a constant DC output voltage for changes in load current (I_{OUT}). Assuming the input voltage (V_{IN}) remains constant, the $r_{DS(ON)}$ is adjusted for a given I_{OUT} to set V_{OUT}. This relationship is summarized in Equation 1.

(EQ. 1) $$V_{OUT} = V_{IN} - I_{OUT} \times R_{DS(ON)}$$

V_{OUT} is set using the FB resistor divider, which sets V_{OUT} to a value that corresponds to Equation 2.

(EQ. 2) $$V_{OUT} = V_{FB} \times \left(\frac{R_F}{R_G} + 1\right)$$

The error amplifier compares V_{FB} with the fixed V_{REF} voltage and works to minimize the difference or error voltage between V_{FB} and V_{REF} by changing the gate voltage of the PMOS pass transistor and therefore the $r_{DS(ON)}$.

If the I_{OUT} suddenly increases because of decreased load resistance, V_{OUT} decreases because the regulator has not responded to the change and the $r_{DS(ON)}$ is set too high. V_{FB} correspondingly decreases and is below the V_{REF} voltage therefore, increasing the error voltage. The error amplifier senses and minimizes the error by driving the PMOS gate voltage more negative relative to the FET source to decrease the $r_{DS(ON)}$, which increases the output voltage bringing it back into regulation.

By similar logic, a sudden decrease in I_{OUT} because of increased load resistance causes V_{OUT} to increase because the $r_{DS(ON)}$ is set too low. V_{FB} is then higher than the fixed V_{REF} voltage increasing the error. The error amplifier senses and minimizes the error by driving the PMOS gate voltage more positive relative to the FET source to increase the $r_{DS(ON)}$, which decreases the output voltage bringing it back into regulation.

For a more detailed explanation of the DC regulation operation of a PMOS LDO regulator, see *R16AN0008: Fundamental Theory of PMOS Low-Dropout Voltage Regulators*.

6. Functional Description

6.1 UVLO

The RAA214250 integrates an internal UVLO circuit to keep the device safely disabled if the input voltage is below the UVLO threshold. This prevents the part from turning on in an unpredictable state.

When the input voltage is above the UVLO threshold, the part is enabled and the output voltage ramps up. The UVLO hysteresis prevents input voltage noise from causing the output to oscillate as well as prevents input voltage droops because of long input traces and wires from turning off the LDO when it turns on and draws current. Figure 75 illustrates the UVLO operation.

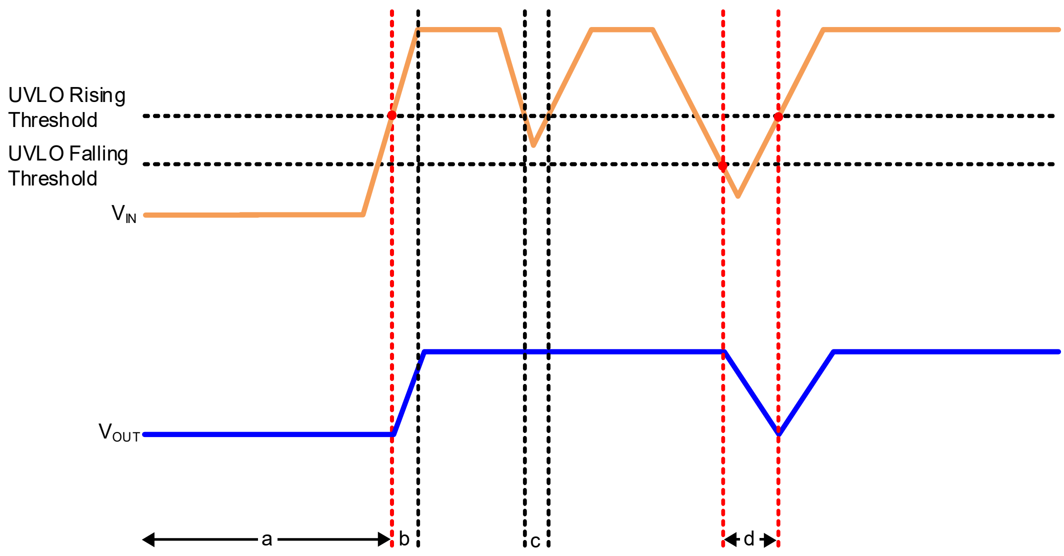


Figure 75. UVLO Operation

a, d The LDO is disabled.

b The LDO is enabled and the output starts to rise.

c The LDO remains enabled.

6.2 Enable Control

The RAA21450 uses the EN pin voltage (V_{EN}) to enable or disable the LDO. If V_{EN} is less than the V_{EN} threshold, the LDO is disabled. If V_{EN} is greater than the V_{EN} threshold, the LDO is enabled. The V_{EN} hysteresis prevents enable voltage noise from causing the output to oscillate. When the LDO is disabled, the shutdown current is typically 3µA.

The EN pin can be directly connected to the input voltage for automatic start-up or connected to a logic controller such as an MCU of FPGA. Some logic pins use an open-collector or open-drain transistor to pull LOW and float when HIGH. Make sure to connect a 1kΩ or 10kΩ pull-up resistor to ensure proper logic HIGH. To ensure proper Enable control operation, the V_{EN} signal source should be capable of swinging above and below the threshold values. The device also has a very accurate and stable Enable threshold, which allows the user to program the Enable voltage through a resistor divider.

6.3 Short-Circuit Current Limit Protection and Foldback

The Short-Circuit Protection circuitry (ILIM) limits the maximum output current the LDO can source during fault conditions such as short-circuits or start-up inrush current. During a short-circuit fault, the LDO becomes a constant current source and as a result any decrease in load resistance causes a decrease in the output voltage. This relationship is summarized in Equation 3.

(EQ. 3) $$V_{OUT} = ILIM \times R_{FAULT}$$

The RAA214250 also incorporates fold-back which reduces the constant current limit to reduce the amount of power dissipation caused during short-circuit events.

When the short or overcurrent condition is removed, the LDO returns to normal output voltage regulation. Because of the high power dissipation caused by overcurrent faults, the LDO may begin to cycle ON and OFF because the die junction temperature (T_J) is exceeding thermal fault conditions (+150°C) and subsequently cooling down to +130°C when the LDO is disabled.

6.4 Over-Temperature Shutdown (OTSD) Protection

The RAA214250 is protected against thermal overloads caused by current limit protection or high ambient temperature (T_A). When the die junction temperature (T_J) exceeds +150°C, the thermal shutdown circuit disables the LDO reducing the output current (I_{OUT}) to 0A and therefore reducing the output voltage (V_{OUT}) to 0V, allowing the LDO to cool. A 20°C hysteresis is included to prevent the LDO from uncontrollably heating and cooling.

Prolonged exposure to a T_J exceeding +125°C reduces the long-term stability and life of the LDO. Therefore, it is important that the design considers the T_A the LDO works in, the thermal resistance between T_J and T_A (θ_{JA}), and any fault conditions that can cause the T_J to exceed the recommended operating range. In some applications, a heat sink may need to be implemented. See Power Dissipation and Thermals to determine the maximum junction temperature for an application.

6.5 Voltage Requirements

6.5.1 Input Voltage

The RAA214250 operates with an input voltage of 2.7V to 20V on the VIN pin. The input supply must be able to supply enough current to keep the input voltage from drooping during load steps or high load currents.

For proper voltage regulation the input voltage must be chosen so that it is higher than the sum of the output voltage and the maximum dropout voltage expected for a given application as expressed in Equation 4.

(EQ. 4) $$V_{IN} > V_{OUT} + V_{DROPOUT(MAX)}$$

The difference between V_{IN} and V_{OUT} required for proper regulation is commonly called the headroom voltage ($V_{HEADROOM}$).

6.5.2 Programming the Output Voltage

The RAA214250 output voltage can be programmed down to 1.224V and up to 18V using external resistors, RF and RG shown in Figure 76.

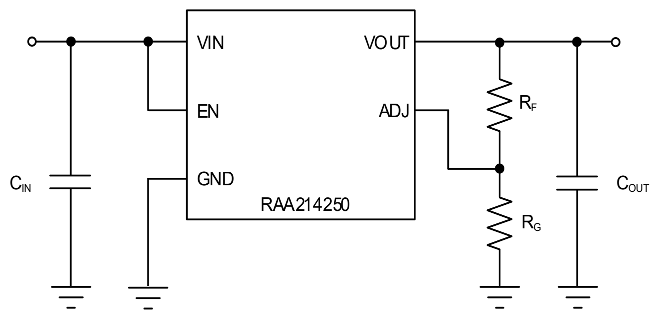


Figure 76. Setting the Output Voltage

V_{OUT} is calculated using Equation 5, where V_{REF} is the reference voltage.

(EQ. 5) $$V_{OUT} = 1.224V \times \left(1 + \frac{R_F}{R_G}\right)$$

Similarly, the R_F and R_G resistors are calculated for any target output voltage by rearranging Equation 5 to get Equation 6 and solving for R_F.

(EQ. 6) $$R_F = R_G \times \left(\frac{V_{OUT(TARGET)}}{1.224V} - 1\right)$$

Table 1 suggests the FB resistor values to get some common voltage rails with 0.1% error. These resistors are also commercially available in 0.1% tolerances. This table is not exhaustive and there may be other R_F and R_G resistor combinations that can provide better accuracy.

Table 1. Recommended R_F and R_G Feedback Resistor Values for Common Voltage Rails

$V_{OUT(TARGET)}$ (V)	R_F (kΩ)	R_G (kΩ)	Error (%)
1.224	0	None	0.0
1.5	100	442	-0.1
1.8	100	210	-0.4
1.9	100	180	-0.2
2.5	100	95.3	-0.3
3	100	68.1	-0.7
3.3	100	59	0.0
4.2	100	41.2	0.1
4.5	100	37.4	0.1
5	100	32.4	0.0
9	100	15.8	0.3
12	100	11.3	-0.5
18	100	7.32	0.3

6.6 External Capacitor Selection

The RAA214250 is stable with C_{IN} C_{OUT} and bypass capacitors. For improved load transient, line transient, PSRR and output noise performance a feed-forward capacitor (C_{FF}) is recommended though it is not required.

Multilayer ceramic capacitors (MLCC) are an excellent choice for bypass capacitors because of their small size, low ESR, low ESL, and wide operating temperature. They are not without their problems though. Ceramic capacitor values can vary with the DC bias voltage, temperature, and tolerance. Therefore, Renesas recommends using de-rated capacitors.

X5R, X7R, and C0G capacitors are recommended.To ensure the performance of the RAA214250. it is important that the effects of DC bias voltage, temperature, and tolerances for a chosen capacitor are evaluated. The X7R type is recommended because it has lower capacitance variation over temperature.

Place the bypass capacitors as close as is practical to their respective pins to minimize trace inductance.

6.6.1 Input Capacitor

The minimum input capacitor that is recommended is 1µF to reduce the negative effects of large input impedances because of long input traces of high source impedances. It is recommended that this capacitor be connected between VIN and GND. A larger bulk capacitor such as a 10µF may need to be added to minimize input voltage droops during large changes in load currents, such as during load transients or during start-up and do not affect stability. Larger input capacitors will also improve the line transient response.

6.6.2 Output Capacitor

The RAA214250 is designed to be stable with an output ceramic capacitor in the range of 2.2µF and 68µF.

A large value output capacitor can help minimize the overshoot and undershoot transient response due to large changes in load current. Larger output capacitors or multiple output capacitors can also be used to improve high-frequency PSRR.

6.6.3 Feed Forward Capacitor

A Feed-Forward Capacitor (C_{FF}) in parallel with the RF resistor as shown in Figure 77 can be used to improve the transient, noise, start-up and PSRR performance. However, it is not necessary to use one to achieve stability.

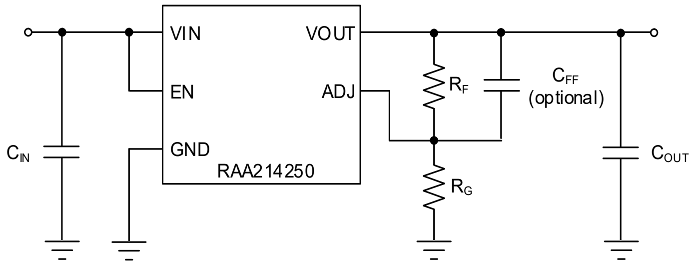


Figure 77. The Feed-Forward Capacitor

Table 2 lists some recommended R_F and R_G resistors and feed-forward capacitor combinations for typical voltage rails. Keep in mind that the R_F and R_G resistor values listed can be used without a feed-forward capacitor as well. When using the feed-forward capacitor, it is better to keep R_G constant, which is why Table 2 shows different R_F and R_G values than Table 1.

Table 2. Recommended R_F and R_G Feedback Resistors and CFF Feed-Forward Capacitors Values for Common Voltage Rails

$V_{OUT(TARGET)}$ (V)	R_F (kΩ)	R_G (kΩ)	C_{FF} (pF)	Error (%)
1.224	0	None	None	0.0
1.5	13	57.6	43	0.0
1.8	27	57.6	39	0.1
1.9	31.6	57.6	37	0.2
2.5	60.4	57.6	30	-0.3
3	84.5	57.6	25	-0.7
3.3	97.6	57.6	22	0.1
4.2	140	57.6	17	0.0
4.5	154	57.6	16	0.1
5	178	57.6	15	-0.1
9	365	57.6	DNP	0.2
12	511	57.6	DNP	-0.7
18	787	57.6	DNP	0.3

6.7 Power Dissipation and Thermals

To ensure reliable operation, the die junction temperature (T_J) of the RAA214250 must not exceed +125°C. In applications with high ambient temperature (T_A), large headroom voltages ($V_{HEADROOM}$), and large load currents (I_{OUT}), the heat dissipated in the package can become large enough to cause the T_J to exceed the maximum operating temperature of +125°C.

6.7.1 Power Dissipation

The Power Dissipation (PD) is calculated using Equation 7.

(EQ. 7) $$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times IQ(V_{IN})$$

Because the power dissipation contribution from the quiescent (or ground current) is typically small compared to the current the LDO needs to supply to a load, it can be ignored and Equation 7 simplifies to Equation 8.

(EQ. 8) $$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Therefore, to lower the power dissipated inside the die, the $V_{HEADROOM}$ and/or the I_{OUT} can be decreased.

6.7.2 The Junction Temperature and Thermal Resistance

The junction temperature (T_J) is the sum of the environmental ambient temperature (T_A) and the temperature rise in the T_J because of power dissipation, which is calculated using Equation 9 if the ambient temperature, Power Dissipation, and θ_{JA} are known.

(EQ. 9) $$T_J = T_A + \theta_{JA} \times PD$$

The θ_{JA} is the thermal resistance between the junction temperature and ambient temperature and is largely dependent on the device package and the PCB design. The θ_{JA} includes the thermal resistance of the junction to the bottom thermal pad ($\theta_{JC(BOTTOM)}$) and the resistance of the junction to the top of the package ($\theta_{JC(TOP)}$). These two thermal resistances are determined by the package features, dimensions, areas, thicknesses, and materials and therefore are fixed.

The remaining thermal resistance that makes up θ_{JA} largely depends on the total PCB copper area, copper weight, location of the thermal planes, and location of the IC on the PCB, amongst other things. Therefore, to compare the θ_{JA} of different products it is important to ensure the PCB layouts are similar, which is why the JEDEC standard exists.

6.7.2.1 Theta JA for Different Copper Area Sizes

Table 3 shows typical Theta J_A values of the 8 Ld 3×3mm DFN package for various copper areas and the JEDEC standard board to illustrate how the θJ_A can be improved with attention to board layout. **Note:** The thermal data on the Eval PCB is based on lab measurements.See Layout Guidelines for layout recommendations.

Table 3. Typical Theta JA Values for the 8-Ld 3x3mm DFN Package for Various PCB Copper Areas (4-layer)

PCB Type	FR-4 PCB Size		Top Copper Detail	Bottom Copper Detail	2 Buried CU Planes Thickness	Buried CU Planes Sizes		# PCB Thermal Vias Under Pkg	# PCB Thermal Vias Around Pkg	θ_{JA} of 8 Ld 3×3mm DFN (°C/W)
	mm	in				mm	in			
JEDEC std. PCB	76.2× 114.3	3×4.5	JEDEC std. 0.25mm wide (2oz thick) traces extend from the package	No meaningful CU on bottom	1-oz each	74.2×74.2	2.92×2.92	4 (touches 1 buried plane)	None	56 (JEDEC)
Eval PCB	101.6×101.6	4 ×4	2-oz, 101.6mm×101.6mm[1]	2-oz, 101.6mm×101.6mm	1-oz each	101.6×101.6	4×4	3[2]	~50 in a 1×1" area[2]	35
Eval PCB	76.2×76.2	3 x3	2-oz, 50.8mm×50.8mm[1]	2-oz, 50.8mm×50.8mm	1-oz each	76.2×76.2	3×3	3[2]	~50 in a 1×1" area[2]	38
Eval PCB	50.8×50.8	2×2	2-oz, 50.8mm×50.8mm[1]	2-oz, 50.8mm×50.8mm	1-oz each	50.8×50.8	2×2	3[2]	~50 in a 1×1" area[2]	43
Eval PCB	25.4×25.4	1×1	2-oz, 25.4mm×25.4mm[1]	2-oz, 25.4mm×25.4mm	1-oz each	25.4×25.4	1×1	3[2]	~50 in a 1×1" area[2]	47

1. Nearly complete Cu fill, with Cu directly connecting the package EPAD to large Cu areas.
2. The vias touch two buried planes and bottom plane.

The following figures provide information about the recommended maximum power dissipation for target junction temperatures for the same boards listed in Table 3 for the 3×3mm DFN package.

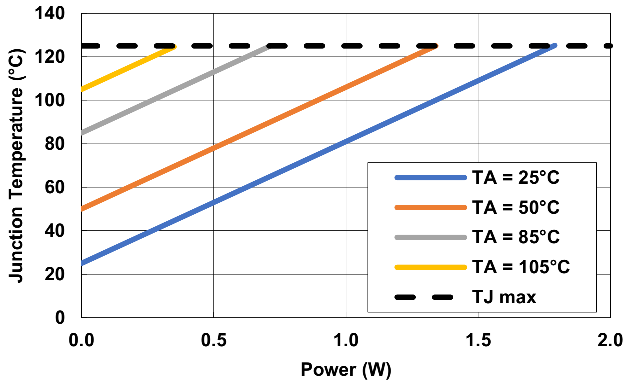


Figure 78. Power Dissipation vs Junction Temperature for Various T_A on the JEDEC Standard PCB (DFN)

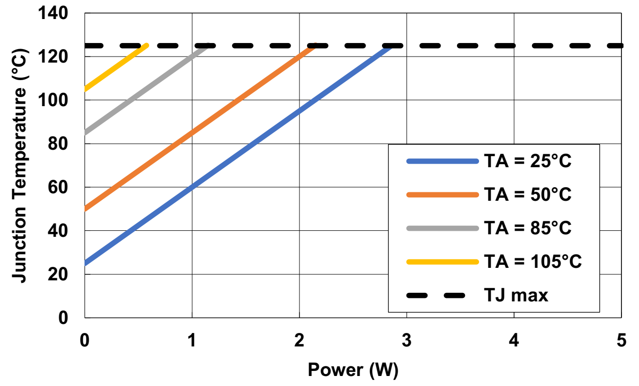


Figure 79. Power Dissipation vs Junction Temperature for Various T_A on a Thermally Optimized 4×4" PCB (DFN)

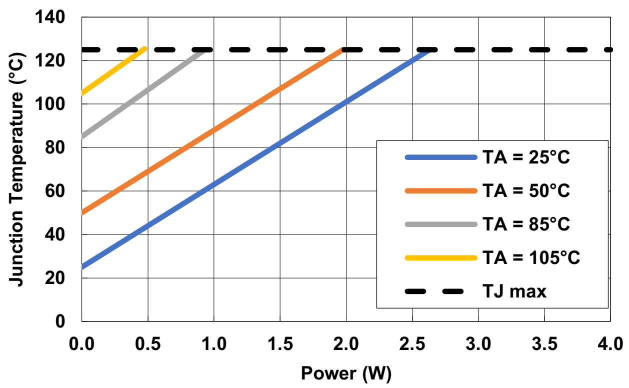


Figure 80. Power Dissipation vs Junction Temperature for Various T_A on a Thermally Optimized 3×3" PCB (DFN)

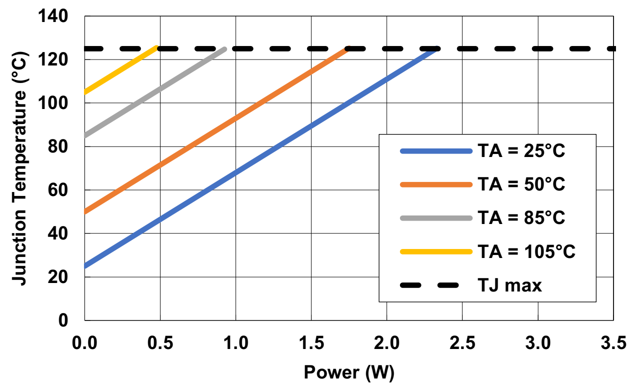


Figure 81. Power Dissipation vs Junction Temperature for Various T_A on a Thermally Optimized 2×2" PCB (DFN)

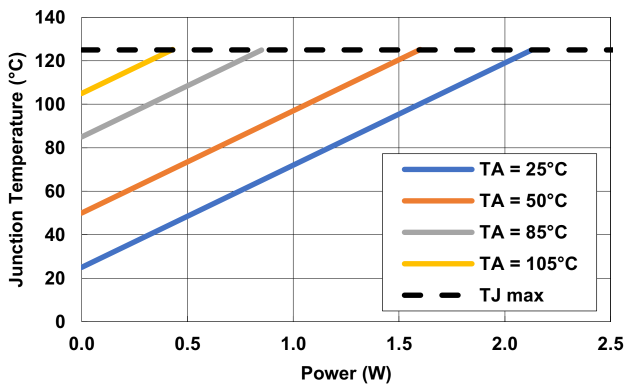


Figure 82. Power Dissipation vs Junction Temperature for Various T_A on a Thermally Optimized 1×1" PCB (DFN)

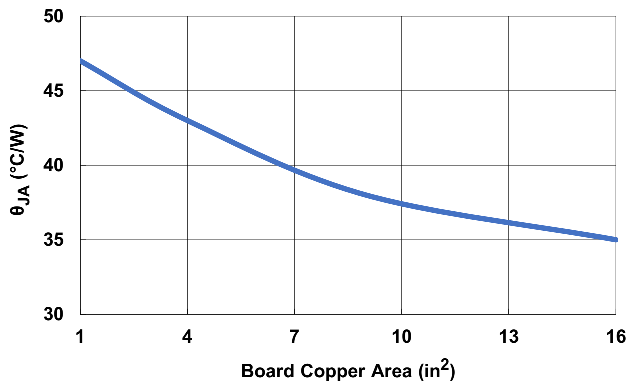


Figure 83. θ_{JA} vs Copper Area Sizes (DFN)

To maximize the θ_{JA} required for a design while keeping copper area size to a minimum, use Figure 83 to determine the heat sinking area required if using the 3x3mm DFN package.

Table 4 shows typical Theta J_A values of the 8-Ld SOIC package for various copper areas and the JEDEC standard board to illustrate how the θ_{JA} can be improved with attention to board layout. **Note:** The thermal data on the Eval PCB is based on lab measurements. See Layout Guidelines for layout recommendations. The SOIC package is better suited for higher power applications than the 3×3mm DFN.

Table 4. Typical Theta JA Values for the 8-Ld SOIC Package for Various PCB Copper Areas (4-layer)

PCB Type	FR-4 PCB Size		Top Copper Detail	Bottom Copper Detail	2 Buried CU Planes Thickness	Buried CU Planes Sizes		# PCB Thermal Vias Under Pkg	# PCB Thermal Vias Around Pkg	θ_{JA} of 8 Ld SOIC (°C/W)
	mm	in				mm	in			
JEDEC std. PCB	76.2×114.3	3× 4.5	JEDEC std. 0.25mm wide (2oz thick) traces extend from the package	No meaningful CU on bottom	1-oz each	74.2×74.2	2.92×2.92	4 (touches 1 buried plane)	None	58 (JEDEC)
Eval PCB	101.6×101.6	4×4	2-oz, 101.6mm×101.6mm[1]	2-oz, 101.6mm x 101.6mm	1-oz each	101.6×101.6	4×4	13[2]	~50 in a 1×1" area[2]	30
Eval PCB	76.2×76.2	3×3	2-oz, 50.8mm×50.8mm[1]	2-oz, 50.8mm x 50.8mm	1-oz each	76.2×76.2	3×3	13[2]	~50 in a 1×1" area[2]	38
Eval PCB	50.8×50.8	2×	2-oz, 50.8mm×50.8mm[1]	2-oz, 50.8mm x 50.8mm	1-oz each	50.8×50.8	2×2	13[2]	~50 in a 1×1" area[2]	43
Eval PCB	25.4×25.4	1×1	2-oz, 25.4mm×25.4mm[1]	2-oz, 25.4mm x 25.4mm	1-oz each	25.4×25.4	1×1	13[2]	~50 in a 1×1" area[2]	51

1. Nearly complete Cu fill, with Cu directly connecting the package EPAD to large Cu areas.
2. The vias touch two buried planes and bottom plane.

The following figures provide information about the recommended maximum power dissipation for target junction temperatures for the same boards listed in Table 4 for the SOIC package.

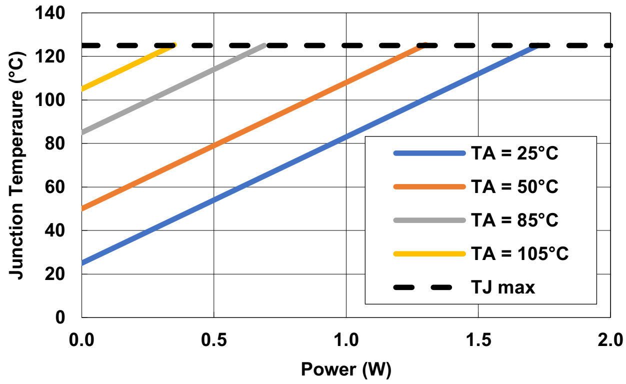


Figure 84. Power Dissipation vs Junction Temperature for Various T_A on the JEDEC Standard PCB (SOIC)

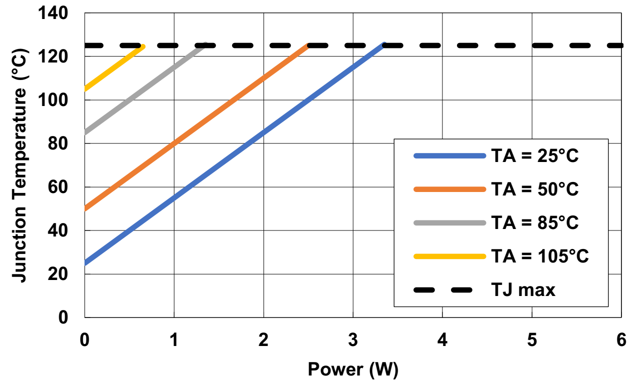


Figure 85. Power Dissipation vs Junction Temperature for Various T_A on a Thermally Optimized 4×4" PCB (SOIC)

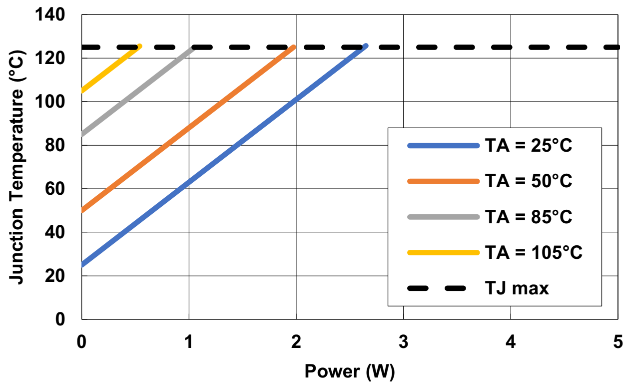


Figure 86. Power Dissipation vs Junction Temperature for Various T_A on a Thermally Optimized 3×3" PCB (SOIC)

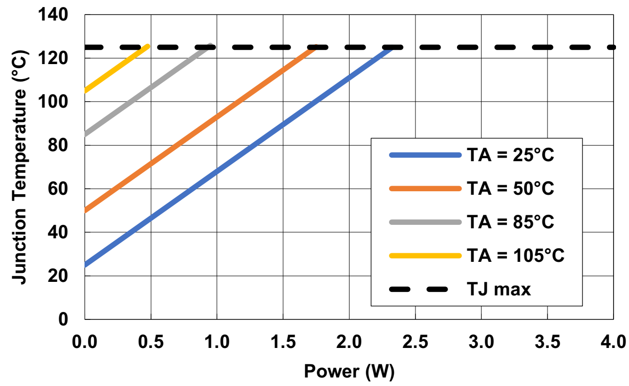


Figure 87. Power Dissipation vs Junction Temperature for Various T_A on a Thermally Optimized 2×2" PCB (SOIC)

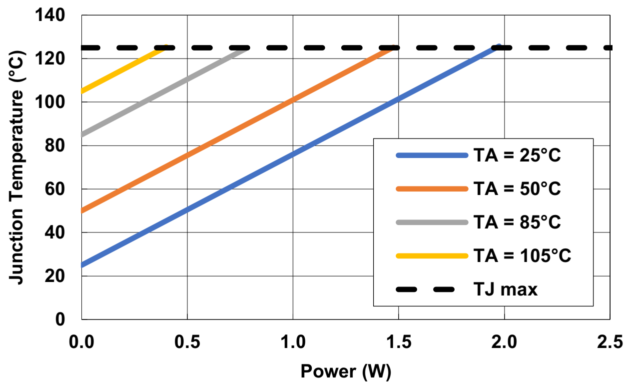


Figure 88. Power Dissipation vs Junction Temperature for Various T_A on a Thermally Optimized 1×1" PCB (SOIC)

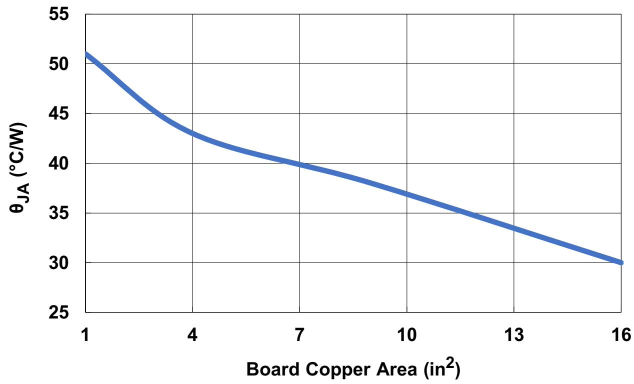


Figure 89. θ_{JA} vs Copper Area Sizes (SOIC)

To maximize the θ_{JA} required for a design while keeping copper area size to a minimum, use Figure 89 to determine the heat sinking area required if using the SOIC package.

7. Layout Guidelines

The following are recommendations for the RAA214250 to achieve optimal performance:

- Place all the required components for the RAA214250 on the same layer as the IC.
- Place a minimum capacitance of 1µF ceramic input capacitor to the VIN and GND pins of the LDO as close as practical.
- Place a minimum capacitance of 2.2µF ceramic output capacitor to the VOUT and GND pins of the LDO as close as practical.
- The feedback trace should be short, direct, and away from other noisy traces. Place the feedback resistors as close as possible to the IC.
- The package thermal EPAD is the largest heat conduction path for the package. It should be soldered to a copper pad on the PCB underneath the part. The PCB thermal pad should have as many plated vias to increase the heat flow from the package thermal EPAD to the inner PCB areas and/or the bottom PCB area. If possible, adding thermal vias around the PCB package helps improve heat spread from the package to other layers of the board.
- Keep the vias small but not so small that their inside diameter prevents solder from wicking through the holes during reflow. For efficient heat transfer, it is important that the vias have low thermal resistance. Do not use thermal relief patterns to connect the vias. It is important to have a complete connection of the plated through-hole to each plane. The top copper GND layer, that the EPAD is connected to is the least thermally resistant path for heat flow. To this end, minimize the components and traces that cut this layer.

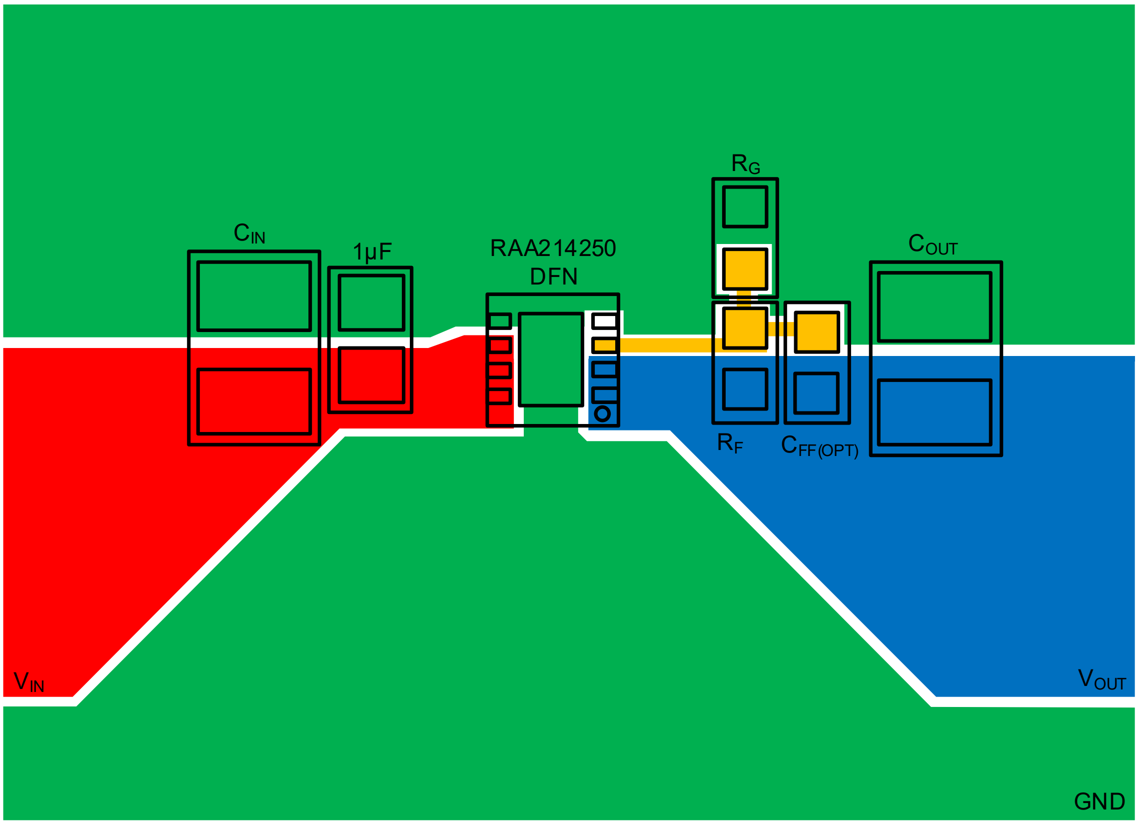


Figure 90. Layout Scheme - DFN

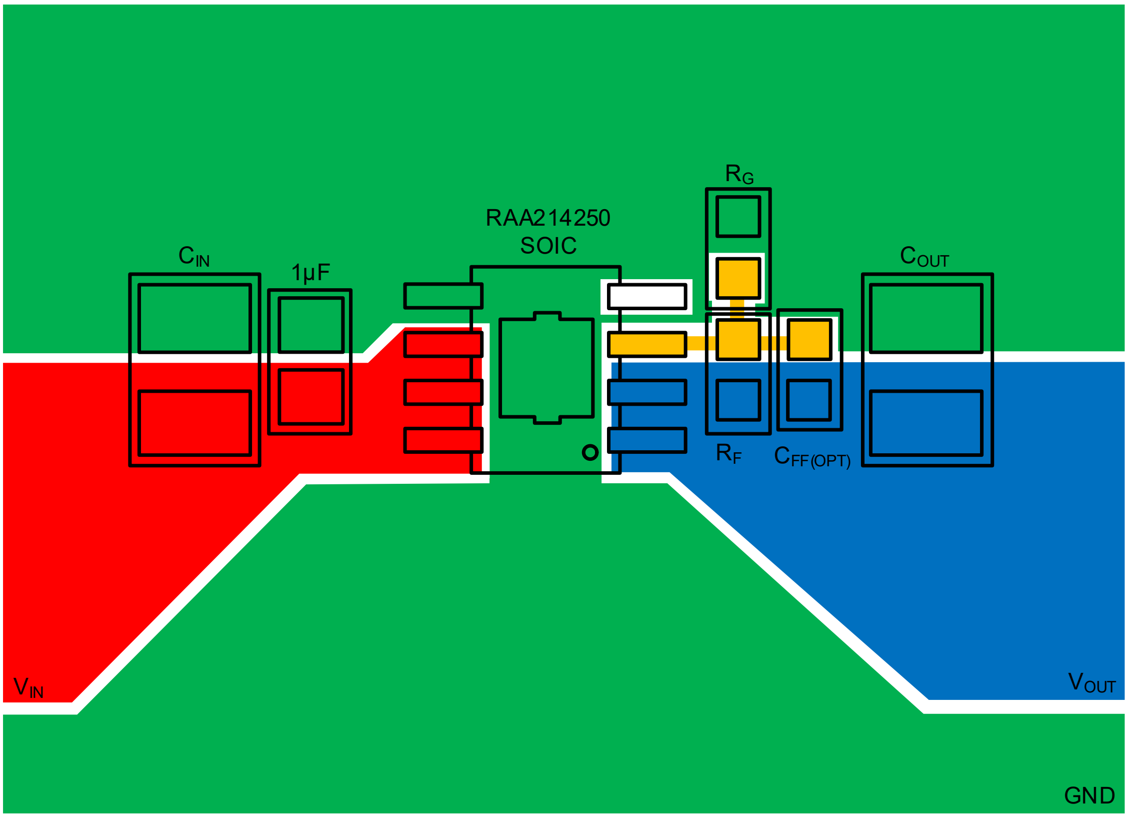
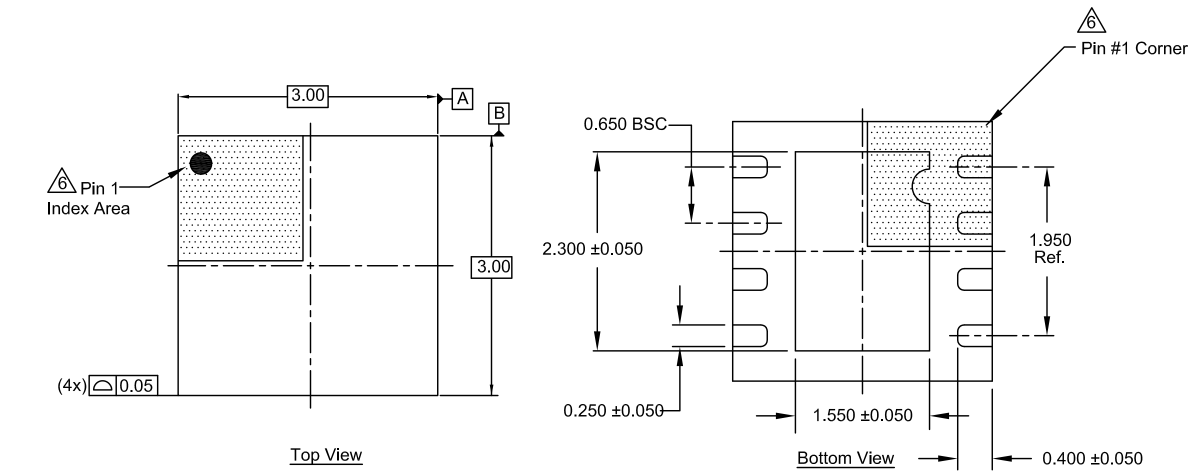


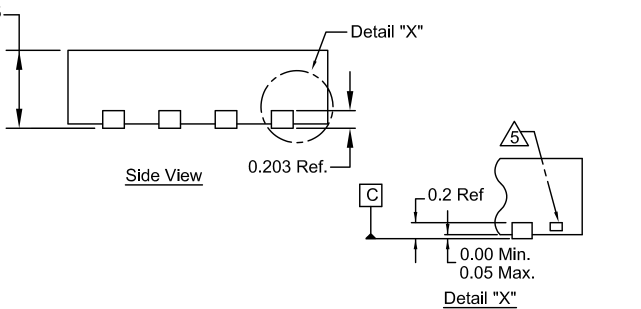
Figure 91. Layout Scheme - SOIC

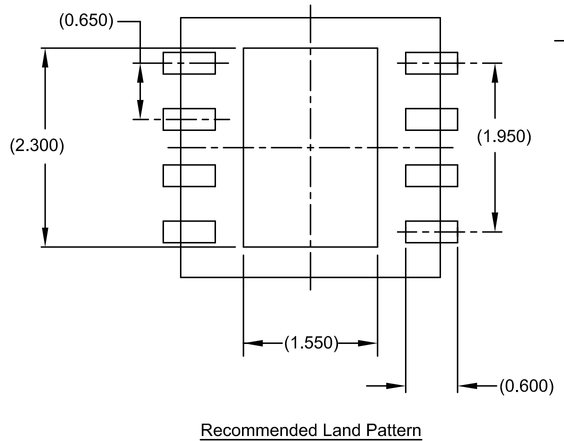
8. Package Outline Drawings

For the most recent package outline drawing, see L8.3x3L.

L8.3x3L
8 Lead Dual Flat No-Lead Plastic Package (DFN)
Rev 0, 3/20





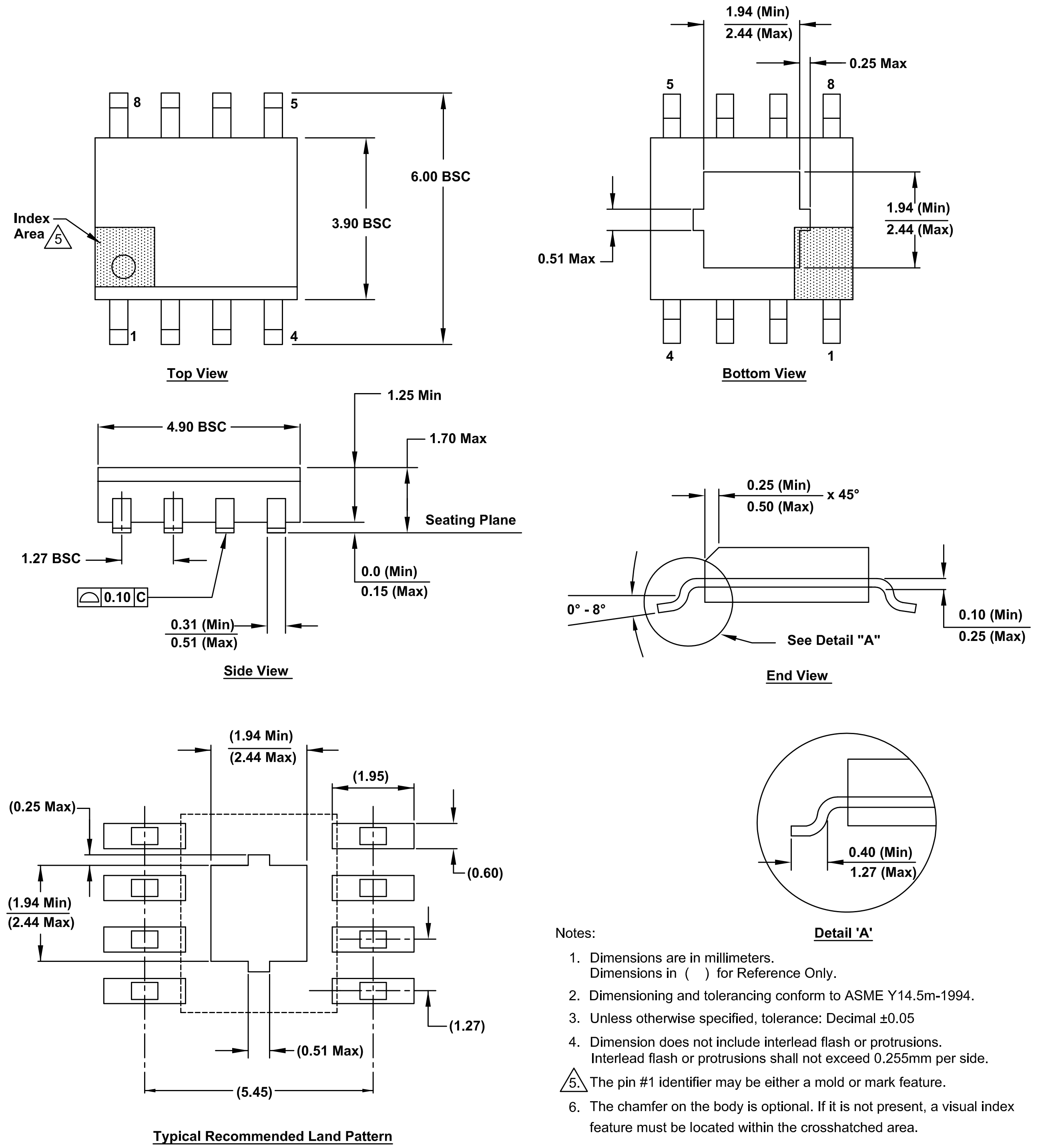


Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. (△4) This dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. (△5) Tiebar shown (if present) is a non-functional feature.
6. (△6) The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier can be either a mold or mark feature.

For the most recent package outline drawing, see M8.15H.

M8.15H
8 Lead Narrow Body Small Outline Exposed Pad Plastic Package (EPSOIC)
Rev 1, 1/20



Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.255mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

9. Ordering Information

Part Number[1][2]	Part Marking	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[4]	Temp. Range
RAA2142504GNP#HC0	214250	8Ld DFN3x3	L8.3x3L	Reel, 6k	-40°C to 125°C
RAA2142504GSP#HA0		8Ld SOIC	M8.15H	Reel, 2.5k	
RTKA214250DE0020BU	Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For the Moisture Sensitivity Level (MSL), see the Product Options on the RAA214250 product page (click the packaging icon). For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications

10. Revision History

Revision	Date	Description
1.03	Aug 17, 2023	Updated Input Voltage section. Moved Pb-Free Reflow note to Ordering Information table and max temp specs to abs max table.
1.02	Oct 14, 2021	Updated Figure 1.
1.01	Oct 11, 2021	Updated the ordering information table.
1.00	Oct 4, 2021	Initial release.

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