



## General Description

Renesas SLG7NT4317 is a low power and small form device. The SoC is housed in a 2mm x 3mm TQFN package which is optimal for using with small devices.

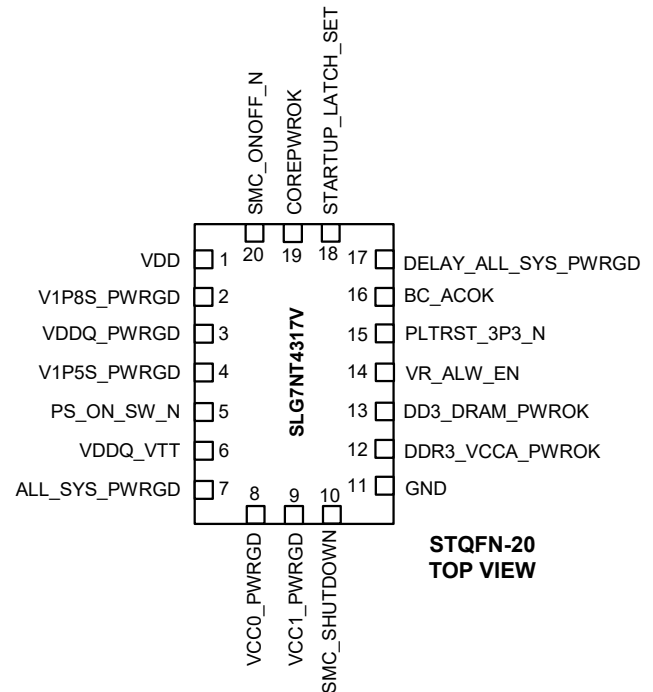
## Features

- Low Power Consumption
- 3.3V Supply
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-20 Package

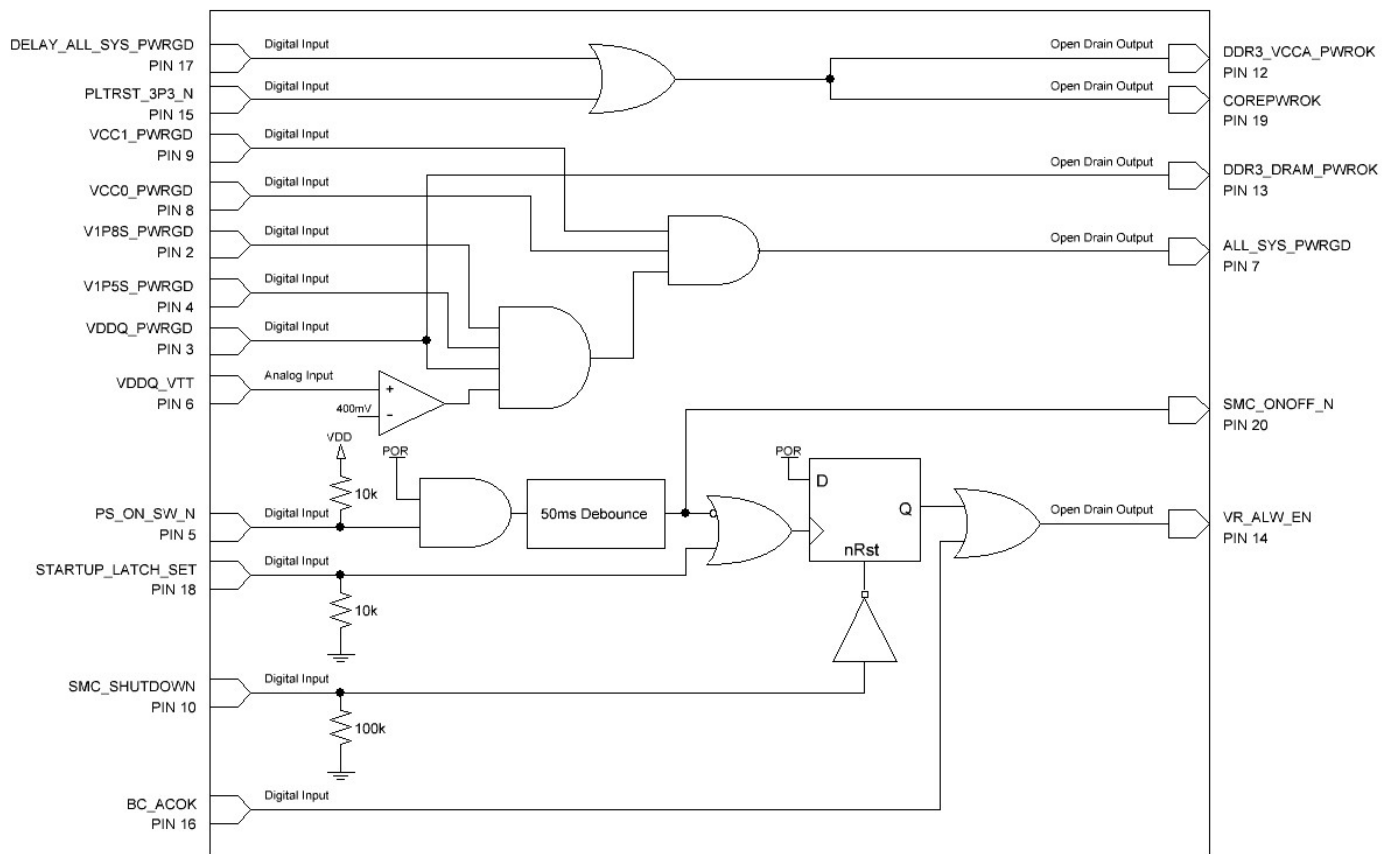
## Output Summary

- 6 Outputs – NMOS Open Drain 1X

## Pin Configuration



### Block Diagram



### Pin Configuration

| Pin # | Pin Name            | Type   | Pin Description                    |
|-------|---------------------|--------|------------------------------------|
| 1     | VDD                 | PWR    | Supply Voltage                     |
| 2     | V1P8S_PWRGD         | Input  | Digital Input                      |
| 3     | VDDQ_PWRGD          | Input  | Digital Input with Schmitt Trigger |
| 4     | V1P5S_PWRGD         | Input  | Digital Input                      |
| 5     | PS_ON_SW_N          | Input  | Digital Input with Schmitt Trigger |
| 6     | VDDQ_VTT            | Input  | Analog Input                       |
| 7     | ALL_SYS_PWRGD       | Output | NMOS Open Drain 1X                 |
| 8     | VCC0_PWRGD          | Input  | Digital Input                      |
| 9     | VCC1_PWRGD          | Input  | Digital Input                      |
| 10    | SMC_SHUTDOWN        | Input  | Digital Input                      |
| 11    | GND                 | --     | Ground                             |
| 12    | DDR3_VCCA_PWROK     | Output | NMOS Open Drain 1X                 |
| 13    | DDR3_DRAM_PWROK     | Output | NMOS Open Drain 1X                 |
| 14    | VR_ALW_EN           | Output | NMOS Open Drain 1X                 |
| 15    | PLTRST_3P3_N        | Input  | Digital Input                      |
| 16    | BC_ACOK             | Input  | Digital Input                      |
| 17    | DELAY_ALL_SYS_PWRGD | Input  | Digital Input                      |
| 18    | STARTUP_LATCH_SET   | Input  | Digital Input                      |
| 19    | COREPWROK           | Output | NMOS Open Drain 1X                 |
| 20    | SMC_ONOFF_N         | Output | NMOS Open Drain 1X                 |

### Ordering Information

| Part Number   | Package Type                        |
|---------------|-------------------------------------|
| SLG7NT4317V   | V=STQFN-20                          |
| SLG7NT4317VTR | STQFN-20 – Tape and Reel (3k units) |

### Absolute Maximum Conditions

| Parameter                 | Min. | Max. | Unit |
|---------------------------|------|------|------|
| V <sub>HIGH</sub> to GND  | -0.3 | 7    | V    |
| Voltage at input pins     | -0.3 | 7    | V    |
| Current at input pin      | -1.0 | 1.0  | mA   |
| Storage temperature range | -65  | 150  | °C   |
| Junction temperature      | --   | 150  | °C   |

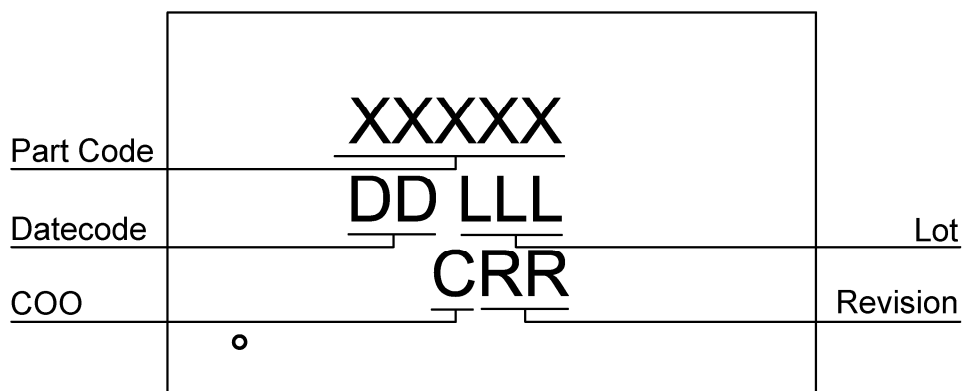
### Electrical Characteristics

(@ 25°C, unless otherwise stated)

| Symbol            | Parameter                           | Condition/Note                                                                                        | Min.  | Typ.  | Max.  | Unit |
|-------------------|-------------------------------------|-------------------------------------------------------------------------------------------------------|-------|-------|-------|------|
| V <sub>DD</sub>   | Supply Voltage                      |                                                                                                       | 3     | --    | 4.5   | V    |
| T <sub>A</sub>    | Operating Temperature               |                                                                                                       | -40   | 25    | 85    | °C   |
| I <sub>Q</sub>    | Quiescent Current                   | Static inputs and outputs at VDD=4.5V                                                                 | --    | 70    | --    | μA   |
| I <sub>L</sub>    | Input Leakage Current               | Leakage Current for Digital Inputs or outputs in High impedance state                                 | -1    | --    | 1     | μA   |
| V <sub>IH</sub>   | HIGH-Level Input Voltage            | Logic Input at VDD=3.3V                                                                               | 1.78  | --    | --    | V    |
|                   |                                     | Logic Input at VDD=5V                                                                                 | 2.64  | --    | --    |      |
|                   |                                     | Logic Input with Schmitt trigger at VDD=3.3V                                                          | 2.13  | --    | --    |      |
|                   |                                     | Logic Input with Schmitt trigger at VDD=5V                                                            | 3.16  | --    | --    |      |
| V <sub>IL</sub>   | LOW-Level Input Voltage             | Logic Input at VDD=3.3V                                                                               | --    | --    | 1.21  | V    |
|                   |                                     | Logic Input at VDD=5V                                                                                 | --    | --    | 1.84  |      |
|                   |                                     | Logic Input with Schmitt trigger at VDD=3.3V                                                          | --    | --    | 0.95  |      |
|                   |                                     | Logic Input with Schmitt trigger at VDD=5V                                                            | --    | --    | 0.78  |      |
| I <sub>IH</sub>   | HIGH-Level Input Current            | Logic Input Pins; V <sub>IN</sub> = 3.3 V                                                             | -1.0  | --    | 1.0   | μA   |
| I <sub>IL</sub>   | LOW-Level Input Current             | Logic Input Pins; V <sub>IN</sub> = 0 V                                                               | -1.0  | --    | 1.0   | μA   |
| V <sub>OL</sub>   | LOW-Level Output Voltage            | Open Drain, at VDD=3.3V, I <sub>OL</sub> = 3 mA, 1X Driver                                            | --    | 0.08  | 0.147 | V    |
|                   |                                     | Open Drain, at VDD=5V, I <sub>OL</sub> = 3 mA, 1X Driver                                              | --    | 0.102 | 0.180 |      |
| I <sub>OL</sub>   | LOW-Level Output Current            | Open Drain, at VDD=3.3V, V <sub>OL</sub> = 0.4 V 1X Driver                                            | 7.313 | 12.37 | --    | mA   |
|                   |                                     | Open Drain, at VDD=5V, V <sub>OL</sub> = 0.4 V, 1X Driver                                             | 10.82 | 17.38 | --    |      |
| V <sub>ACMP</sub> | Analog Comparator Threshold Voltage | ACMP0 threshold including input offset, V <sub>ref</sub> variation and hysteresis at 25°C temperature | 368   | --    | 432   | mV   |
| V <sub>HYST</sub> | Analog Comparator Hysteresis        | ACMP0, at 25°C                                                                                        | --    | 25    | --    | mV   |

|            |                                                            |                                         |    |     |     |    |
|------------|------------------------------------------------------------|-----------------------------------------|----|-----|-----|----|
| $V_O$      | Maximal Voltage Applied to any PIN in High-Impedance State |                                         | -- | --  | VDD | V  |
| $I_O$      | Maximal Average or DC Current                              | Per Each Side (PIN2-PIN10, PIN12-PIN20) | -- | --  | 80  | mA |
| $T_{DLY0}$ | Delay0 Time                                                | At 25°C temperature                     | 48 | --  | 52  | ms |
|            |                                                            | At 0-70°C temperature range             | 44 | --  | 56  |    |
| $R_{PU}$   | Internal Pull Up Resistance                                | On PIN5                                 | 7  | 10  | 13  | kΩ |
| $R_{PD}$   | Internal Pull Down Resistance                              | On PIN18                                | 7  | 10  | 13  | kΩ |
|            |                                                            | On PIN10                                | 70 | 100 | 130 |    |
| $T_{SU}$   | Start up Time                                              | After VDD reaches 1.6V level            | -- | 1   | --  | ms |

### Package Top Marking



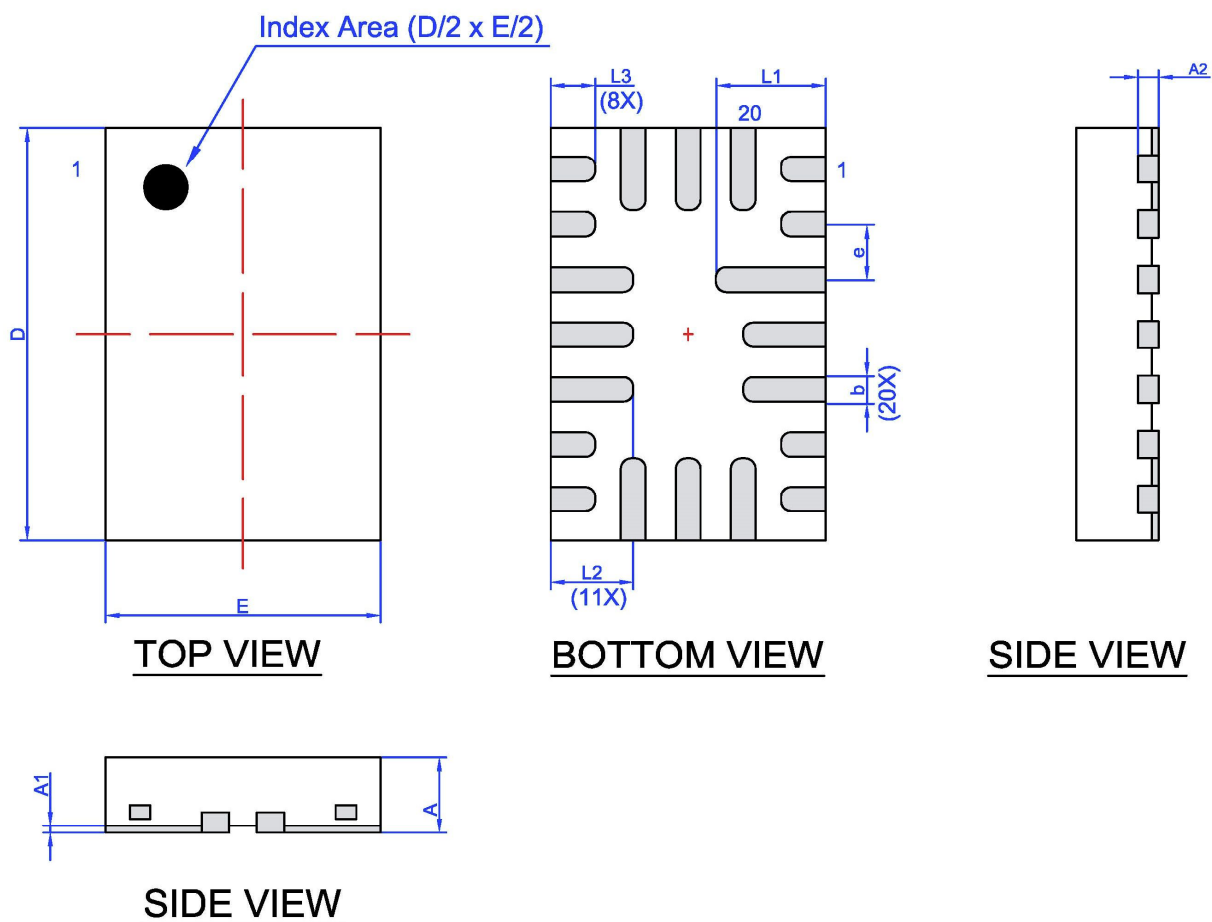
XXXXX – Part ID Field: identifies the specific device configuration  
 DD – Date Code Field: Coded date of manufacture  
 LLL – Lot Code: Designates Lot #  
 C – Assembly Site/COO: Specifies Assembly Site/Country of Origin  
 RR – Revision Code: Device Revision

| Datasheet Revision | Programming Code Number | Locked Status | Part Code | Revision | Date       |
|--------------------|-------------------------|---------------|-----------|----------|------------|
| 1.01               | 004                     | L             | 4317V     | AB       | 02/25/2022 |

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking

### Package Drawing and Dimensions

#### 20 Lead STQFN Package JEDEC MO-220, Variation WECE



Unit: mm

| Symbol | Min      | Nom. | Max   | Symbol | Min   | Nom.  | Max   |
|--------|----------|------|-------|--------|-------|-------|-------|
| A      | 0.50     | 0.55 | 0.60  | D      | 2.95  | 3.00  | 3.05  |
| A1     | 0.005    | -    | 0.050 | E      | 1.95  | 2.00  | 2.05  |
| A2     | 0.10     | 0.15 | 0.20  | L1     | 0.75  | 0.80  | 0.85  |
| b      | 0.13     | 0.18 | 0.23  | L2     | 0.55  | 0.60  | 0.65  |
| e      | 0.40 BSC |      |       | L3     | 0.275 | 0.325 | 0.375 |

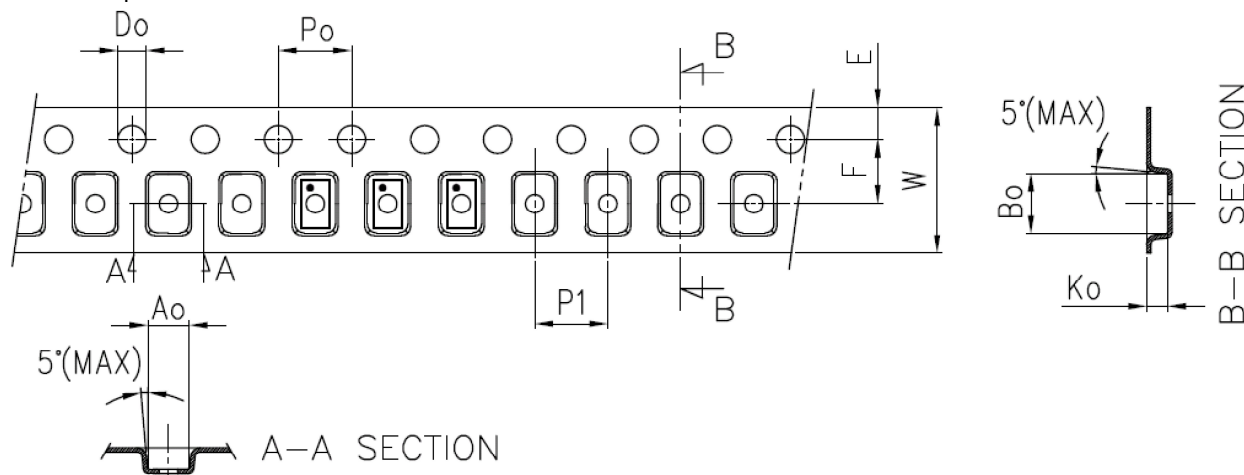
### Tape and Reel Specification

| Package Type                     | # of Pins | Nominal Package Size (mm) | Max Units |         | Reel & Hub Size (mm) | Trailer A |             | Leader B |             | Pocket (mm) |       |
|----------------------------------|-----------|---------------------------|-----------|---------|----------------------|-----------|-------------|----------|-------------|-------------|-------|
|                                  |           |                           | per reel  | per box |                      | Pockets   | Length (mm) | Pockets  | Length (mm) | Width       | Pitch |
| STQFN 20L<br>2x3mm 0.4P<br>Green | 20        | 2x3x0.55                  | 3000      | 3000    | 178/60               | 100       | 400         | 100      | 400         | 8           | 4     |

### Carrier Tape Drawing and Dimensions

| Package Type                     | Pocket BTM Length (mm) | Pocket BTM Width (mm) | Pocket Depth (mm) | Index Hole Pitch (mm) | Pocket Pitch (mm) | Index Hole Diameter (mm) | Index Hole to Tape Edge (mm) | Index Hole to Pocket Center (mm) | Tape Width (mm) |
|----------------------------------|------------------------|-----------------------|-------------------|-----------------------|-------------------|--------------------------|------------------------------|----------------------------------|-----------------|
|                                  | A0                     | B0                    | K0                | P0                    | P1                | D0                       | E                            | F                                | W               |
| STQFN 20L<br>2x3mm<br>0.4P Green | 2.2                    | 3.15                  | 0.76              | 4                     | 4                 | 1.5                      | 1.75                         | 3.5                              | 8               |

Refer to EIA-481 Specifications



### Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm<sup>3</sup> (nominal). More information can be found at [www.jedec.org](http://www.jedec.org).



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