

120-MHz 32-bit RX MCU, on-chip FPU, 240 DMIPS, up to 2-MB flash memory (supportive of the dual bank function), 640-KB SRAM, various communications interfaces including Ethernet MAC, SD host interface, SD slave interface, quad SPI, and CAN, 12-bit A/D converter, RTC, Encryption functions, CMOS camera interface, Graphic-LCD controller, 2D drawing engine

## Features

### ■ 32-bit RXv2 CPU core

- Max. operating frequency: 120 MHz  
Capable of 240 DMIPS in operation at 120 MHz
- Single precision 32-bit IEEE-754 floating point
- Two types of multiply-and-accumulation unit (between memories and between registers)
- 32-bit multiplier (fastest instruction execution takes one CPU clock cycle)
- Divider (fastest instruction execution takes two CPU clock cycles)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions: Ultra-compact code
- Supports the memory protection unit (MPU)
- JTAG and FINE (one-line) debugging interfaces

### ■ Low-power design and architecture

- Operation from a single 2.7- to 3.6-V supply
- Low power consumption: A product that supports all peripheral functions draws only 0.19 mA/MHz (Typ.).
- RTC is capable of operation from a dedicated power supply.
- Four low-power modes

### ■ On-chip code flash memory

- Supports versions with up to 2 Mbytes of ROM
- No wait cycles at up to 50 MHz or when the ROM cache is hit, one-wait state at up to 100 MHz, two-wait state at above 100 MHz
- User code is programmable by on-board or off-board programming.
- Programming/erasing as background operations (BGOs)
- A dual-bank structure allows exchanging the start-up bank.

### ■ On-chip data flash memory

- 32 Kbytes, reprogrammable up to 100,000 times
- Programming/erasing as background operations (BGOs)

### ■ On-chip SRAM, no wait states

- 256K/640 Kbytes of SRAM (no wait states)
- 8 Kbytes of standby RAM (backup on deep software standby)

### ■ Data transfer

- DMACa: 8 channels
- DTCb: 1 channel
- EXDMAC: 2 channels
- DMAC for the Ethernet controller: 1 channel

### ■ Reset and supply management

- Power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

### ■ Clock functions

- External crystal resonator or internal PLL for operation at 8 to 24 MHz
- Internal 240-kHz LOCO and HOCO selectable from 16, 18, and 20 MHz
- 120-kHz clock for the IWDtA

### ■ Real-time clock

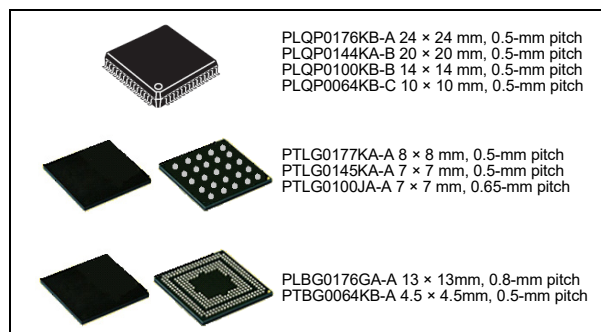
- Adjustment functions (30 seconds, leap year, and error)
- Real-time clock counting and binary counting modes are selectable
- Time capture function  
(for capturing times in response to event-signal input)

### ■ Independent watchdog timer

- 120-kHz (1/2 LOCO frequency) clock operation

### ■ Useful functions for IEC60730 compliance

- Oscillation-stoppage detection, frequency measurement, CRCA, IWDtA, self-diagnostic function for the A/D converter, etc.
- Register write protection function can protect values in important registers against overwriting.



### ■ Various communications interfaces

- Ethernet MAC (1 channel)
- PHY layer (1 channel) for host/function or OTG controller (1 channel) with full-speed USB 2.0 transfer
- CAN (compliant with ISO11898-1), incorporating 32 mailboxes (up to 2 channels)
- SCiG and SCiH with multiple functionalities (up to 11 channels)  
Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simplified SPI, simplified I<sup>2</sup>C, and extended serial mode.
- SCiI with 16-byte transmission and reception FIFOs (up to 2 channels)
- I<sup>2</sup>C bus interface for transfer at up to 1 Mbps (up to 3 channels)
- Four-wire QSPI (1 channel) in addition to RSPiC (3 channels)
- Parallel data capture unit (PDC) for the CMOS camera interface
- Graphic-LCD controller (GLCDC)
- 2D drawing engine (DRW2D)
- SD host interface (1 channel) with a 1- or 4-bit SD bus for use with SD memory or SDIO
- SD slave interface (1 channel) with a 1- or 4-bit SD bus for use with SD host interface
- MMCIF with 1-, 4-, or 8-bit transfer bus width

### ■ External address space

- Buses for full-speed data transfer (max. operating frequency of 60 MHz)
- 8 CS areas
- 8-, 16-, or 32-bit bus space is selectable per area
- Independent SDRAM area (128 Mbytes)

### ■ Up to 25 extended-function timers

- 16-bit TPUa, MTU3a
- 8-bit TMRa (4 channels), 16-bit CMT (4 channels), 32-bit CMTW (2 channels)

### ■ 12-bit A/D converter

- Two 12-bit units (8 channels for unit 0; 21 channels for unit 1)
- Self diagnosis, detection of analog input disconnection

### ■ 12-bit D/A converter: 2 channels

### ■ Temperature sensor for measuring temperature within the chip

### ■ Encryption functions

- AES (key lengths: 128, 192, and 256 bits)
- Trusted Secure IP (TSIP)

### ■ Up to 136 pins for general I/O ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability

### ■ Operating temp. range

- D-version: -40°C to +85°C
- G-version: -40°C to +105°C

# 1. Overview

## 1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 give a comparison of the functions of products in different packages.

Table 1.1 is an outline of maximum specifications, and the peripheral modules and the number of channels of the modules differ depending on the number of pins on the package and the capacity of the code flash memory. For details, see Table 1.2, Code Flash Memory Capacity and Comparison of Functions for Different Packages.

**Table 1.1 Outline of Specifications (1/10)**

| Classification | Module/Function   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CPU            | CPU               | <ul style="list-style-type: none"> <li>Maximum operating frequency: 120 MHz</li> <li>32-bit RX CPU (RXv2)</li> <li>Minimum instruction execution time: One instruction per state (cycle of the system clock)</li> <li>Address space: 4-Gbyte linear</li> <li>Register set of the CPU               <ul style="list-style-type: none"> <li>General purpose: Sixteen 32-bit registers</li> <li>Control: Ten 32-bit registers</li> <li>Accumulator: Two 72-bit registers</li> </ul> </li> <li>Basic instructions: 75</li> <li>Floating-point instructions: 11</li> <li>DSP instructions: 23</li> <li>Addressing modes: 11</li> <li>Data arrangement               <ul style="list-style-type: none"> <li>Instructions: Little endian</li> <li>Data: Selectable as little endian or big endian</li> </ul> </li> <li>On-chip 32-bit multiplier: <math>32 \times 32 \rightarrow 64</math> bits</li> <li>On-chip divider: <math>32 / 32 \rightarrow 32</math> bits</li> <li>Barrel shifter: 32 bits</li> </ul> |
|                | FPU               | <ul style="list-style-type: none"> <li>Single precision (32-bit) floating point</li> <li>Data types and floating-point exceptions in conformance with the IEEE754 standard</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Memory         | Code flash memory | <ul style="list-style-type: none"> <li>Capacity: 512 Kbytes/768 Kbytes/1 Mbyte/1.5 Mbytes/2 Mbytes</li> <li><math>50 \text{ MHz} \leq</math> No-wait cycle access</li> <li><math>100 \text{ MHz} \leq</math> 1-wait cycle access</li> <li><math>100 \text{ MHz} &gt;</math> 2-wait cycle access</li> <li>Instructions hitting the ROM cache or operand = 120 MHz: No-wait access</li> <li>On-board programming: Four types</li> <li>Off-board programming (parallel programmer mode)</li> <li>Instructions are executable only for the program stored in the TM target area by using the Trusted Memory (TM) function and protection against data reading is realized.</li> <li>A dual-bank structure allows programming during reading or exchanging the start-up areas</li> </ul>                                                                                                                                                                                                                     |
|                | Data flash memory | <ul style="list-style-type: none"> <li>Capacity: 32 Kbytes</li> <li>Programming/erasing: 100,000 times</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|                | Unique ID         | <ul style="list-style-type: none"> <li>16-byte unique ID for the device</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|                | RAM               | <ul style="list-style-type: none"> <li>Capacity: 256 Kbytes (Products with 1 Mbyte of code flash memory or less)</li> <li>RAM: 256 Kbytes</li> <li>Capacity: 640 Kbytes (Products with at least 1.5 Mbytes of code flash memory)</li> <li>RAM: 256 Kbytes</li> <li>Expansion RAM: 384 Kbytes</li> <li>120 MHz, no-wait access</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                | Standby RAM       | <ul style="list-style-type: none"> <li>Capacity: 8 Kbytes</li> <li>Operation synchronized with PCLKB: Up to 60 MHz, two-cycle access</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

**Table 1.1 Outline of Specifications (2/10)**

| Classification                   | Module/Function          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------------------------------|--------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Operating modes                  |                          | <ul style="list-style-type: none"> <li>Operating modes by the mode-setting pins at the time of release from the reset state               <ul style="list-style-type: none"> <li>Single-chip mode</li> <li>Boot mode (for the SCI interface)</li> <li>Boot mode (for the USB interface)</li> <li>Boot mode (for the FINE interface)</li> </ul> </li> <li>Selection of operating mode by register setting               <ul style="list-style-type: none"> <li>Single-chip mode</li> <li>On-chip ROM disabled extended mode</li> <li>On-chip ROM enabled extended mode</li> </ul> </li> <li>Endian selectable</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| Clock                            | Clock generation circuit | <ul style="list-style-type: none"> <li>Main clock oscillator, sub clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDG-dedicated on-chip oscillator</li> <li>The peripheral module clocks can be set to frequencies above that of the system clock.</li> <li>Main-clock oscillation stoppage detection</li> <li>Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), flash-IF clock (FCLK) and external bus clock (BCLK)</li> <li>The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 120 MHz</li> <li>Peripheral modules of MTU3, RSPI, SCli, ETHERC, EDMAC, AES, GLCDC, and DRW2D run in synchronization with PCLKA, which operates at up to 120 MHz.</li> <li>Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz</li> <li>ADCLK in the S12AD (unit 0) runs in synchronization with PCLKC: Up to 60 MHz</li> <li>ADCLK in the S12AD (unit 1) runs in synchronization with PCLKD: Up to 60 MHz</li> <li>Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz</li> <li>Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 60 MHz</li> <li>Multiplication is possible with using the high-speed on-chip oscillator (HOCO) as a reference clock of the PLL circuit</li> </ul> |
| Reset                            |                          | <p>Nine types of reset</p> <ul style="list-style-type: none"> <li>RES# pin reset: Generated when the RES# pin is driven low.</li> <li>Power-on reset: Generated when the RES# pin is driven high and VCC = AVCC0 = AVCC1 rises.</li> <li>Voltage-monitoring 0 reset: Generated when VCC = AVCC0 = AVCC1 falls.</li> <li>Voltage-monitoring 1 reset: Generated when VCC = AVCC0 = AVCC1 falls.</li> <li>Voltage-monitoring 2 reset: Generated when VCC = AVCC0 = AVCC1 falls.</li> <li>Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby.</li> <li>Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs.</li> <li>Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs.</li> <li>Software reset: Generated by register setting.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| Power-on reset                   |                          | <p>If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC = AVCC0 = AVCC1 has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Voltage detection circuit (LVDA) |                          | <p>Monitors the voltage being input to the VCC = AVCC0 = AVCC1 pins and generates an internal reset or interrupt.</p> <ul style="list-style-type: none"> <li>Voltage detection circuit 0           <ul style="list-style-type: none"> <li>Capable of generating an internal reset</li> <li>The option-setting memory can be used to select enabling or disabling of the reset.</li> <li>Voltage detection level: Selectable from three different levels (2.94 V, 2.87 V, 2.80 V)</li> </ul> </li> <li>Voltage detection circuits 1 and 2           <ul style="list-style-type: none"> <li>Voltage detection level: Selectable from three different levels (2.99 V, 2.92 V, 2.85 V)</li> <li>Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency)</li> <li>Capable of generating an internal reset</li> </ul> </li> <li>Two types of timing are selectable for release from reset           <ul style="list-style-type: none"> <li>An internal interrupt can be requested.</li> </ul> </li> <li>Detection of voltage rising above and falling below thresholds is selectable.</li> <li>Maskable or non-maskable interrupt is selectable</li> <li>Voltage detection monitoring</li> <li>Event linking</li> </ul>                                                                                                                                                                                                                                |

**Table 1.1 Outline of Specifications (3/10)**

| Classification         | Module/Function                 | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------------------------|---------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Low power consumption  | Low power consumption function  | <ul style="list-style-type: none"> <li>Module stop function</li> <li>Four low power consumption modes: Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                              |
|                        | Battery backup function         | <ul style="list-style-type: none"> <li>When the voltage on the VCC pin drops, battery power from the VBATT pin is supplied to keep the real-time clock (RTC) operating.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Interrupt              | Interrupt controller (ICUB)     | <ul style="list-style-type: none"> <li>Peripheral function interrupts: 262 sources</li> <li>External interrupts: 16 (pins IRQ0 to IRQ15)</li> <li>Software interrupts: 2 sources</li> <li>Non-maskable interrupts: 7 sources</li> <li>Sixteen levels specifiable for the order of priority</li> <li>Method of interrupt source selection:<br/>The interrupt vectors consist of 256 vectors (128 sources are fixed. The remaining 128 vectors are selected from among the other 123 sources.)</li> </ul>                                                                                                      |
| External bus extension |                                 | <ul style="list-style-type: none"> <li>The external address space can be divided into eight areas (CS0 to CS7), each with independent control of access settings.<br/>Capacity of each area: 16 Mbytes (CS0 to CS7)<br/>A chip-select signal (CS0# to CS7#) can be output for each area.<br/>Each area is specifiable as an 8-, 16-, or 32-bit bus space.<br/>The data arrangement in each area is selectable as little or big endian (only for data).</li> <li>SDRAM interface connectable</li> <li>Bus format: Separate bus, multiplex bus</li> <li>Wait control</li> <li>Write buffer facility</li> </ul> |
| DMA                    | DMA controller (DMACa)          | <ul style="list-style-type: none"> <li>8 channels</li> <li>Three transfer modes: Normal transfer, repeat transfer, and block transfer</li> <li>Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions</li> </ul>                                                                                                                                                                                                                                                                                                                                        |
|                        | EXDMA controller (EXDMACa)      | <ul style="list-style-type: none"> <li>2 channels</li> <li>Four transfer modes: Normal transfer, repeat transfer, block transfer, and cluster transfer</li> <li>Single-address transfer enabled with the EDACKn signal</li> <li>Request sources: Software trigger, external DMA requests (EDREQn), and interrupt requests from peripheral functions</li> </ul>                                                                                                                                                                                                                                               |
|                        | Data transfer controller (DTCb) | <ul style="list-style-type: none"> <li>Three transfer modes: Normal transfer, repeat transfer, and block transfer</li> <li>Request sources: External interrupts and interrupt requests from peripheral functions</li> <li>Sequence transfer</li> </ul>                                                                                                                                                                                                                                                                                                                                                       |

**Table 1.1 Outline of Specifications (4/10)**

| Classification              | Module/Function        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----------------------------|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I/O ports                   | Programmable I/O ports | <ul style="list-style-type: none"> <li>I/O ports for the 177-pin TFLGA, 176-pin LFBGA, and 176-pin LFQFP<br/>I/O pins: 136<br/>Input pin: 1<br/>Pull-up resistors: 136<br/>Open-drain outputs: 136<br/>5-V tolerance: 19</li> <li>I/O ports for the 145-pin TFLGA and 144-pin LFQFP<br/>I/O pins: 111<br/>Input pin: 1<br/>Pull-up resistors: 111<br/>Open-drain outputs: 111<br/>5-V tolerance: 18</li> <li>I/O ports for the 100-pin TFLGA and 100-pin LFQFP<br/>I/O pins: 78<br/>Input pin: 1<br/>Pull-up resistors: 78<br/>Open-drain outputs: 78<br/>5-V tolerance: 17</li> <li>I/O ports for the 64-pin TFBGA<br/>I/O pins: 41<br/>Input pin: 1<br/>Pull-up resistors: 41<br/>Open-drain outputs: 41<br/>5-V tolerance: 8</li> <li>I/O ports for the 64-pin LFQFP<br/>I/O pins: 42<br/>Input pin: 1<br/>Pull-up resistors: 42<br/>Open-drain outputs: 42<br/>5-V tolerance: 8</li> </ul> |
| Event link controller (ELC) |                        | <ul style="list-style-type: none"> <li>Event signals such as interrupt request signals can be interlinked with the operation of functions such as timer counting, eliminating the need for intervention by the CPU to control the functions.</li> <li>83 internal event signals can be freely combined for interlinked operation with connected functions.</li> <li>Event signals from peripheral modules can be used to change the states of output pins (of ports B and E).</li> <li>Changes in the states of pins (of ports B and E) being used as inputs can be interlinked with the operation of peripheral modules.</li> </ul>                                                                                                                                                                                                                                                           |

**Table 1.1 Outline of Specifications (5/10)**

| Classification | Module/Function                        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|----------------|----------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Timers         | 16-bit timer pulse unit (TPUa)         | <ul style="list-style-type: none"> <li>• (16 bits × 6 channels) × 1 unit</li> <li>• Maximum of 16 pulse-input/output possible</li> <li>• Select from among seven or eight counter-input clock signals for each channel</li> <li>• Input capture/output compare function</li> <li>• Output of PWM waveforms in up to 15 phases in PWM mode</li> <li>• Support for buffered operation, phase-counting mode (two phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel.</li> <li>• PPG output trigger can be generated</li> <li>• Capable of generating conversion start triggers for the A/D converters</li> <li>• Digital filtering of signals from the input capture pins</li> <li>• Event linking by the ELC</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|                | Multifunction timer pulse unit (MTU3a) | <ul style="list-style-type: none"> <li>• 9 channels (16 bits × 8 channels, 32 bits × 1 channel)</li> <li>• Maximum of 28 pulse-input/output and 3 pulse-input possible</li> <li>• Select from among 14 counter-input clock signals for each channel (PCLKA/1, PCLKA/2, PCLKA/4, PCLKA/8, PCLKA/16, PCLKA/32, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A)</li> <li>• 14 of the signals are available for channel 0, 11 are available for channels 1, 3, 4, 6 to 8, 12 are available for channel 2, and 10 are available for channel 5.</li> <li>• Input capture function</li> <li>• 39 output compare/input capture registers</li> <li>• Counter clear operation (synchronous clearing by compare match/input capture)</li> <li>• Simultaneous writing to multiple timer counters (TCNT)</li> <li>• Simultaneous register input/output by synchronous counter operation</li> <li>• Buffered operation</li> <li>• Support for cascade-connected operation</li> <li>• 43 interrupt sources</li> <li>• Automatic transfer of register data</li> <li>• Pulse output mode</li> <li>• Toggle/PWM/complementary PWM/reset-synchronized PWM</li> <li>• Complementary PWM output mode</li> <li>• Outputs non-overlapping waveforms for controlling 3-phase inverters</li> <li>• Automatic specification of dead times</li> <li>• PWM duty cycle: Selectable as any value from 0% to 100%</li> <li>• Delay can be applied to requests for A/D conversion.</li> <li>• Non-generation of interrupt requests at peak or trough values of counters can be selected.</li> <li>• Double buffer configuration</li> <li>• Reset synchronous PWM mode</li> <li>• Three phases of positive and negative PWM waveforms can be output with desired duty cycles.</li> <li>• Phase-counting mode: 16-bit mode (channels 1 and 2); 32-bit mode (channels 1 and 2)</li> <li>• Counter functionality for dead-time compensation</li> <li>• Generation of triggers for A/D converter conversion</li> <li>• A/D converter start triggers can be skipped</li> <li>• Digital filter function for signals on the input capture and external counter clock pins</li> <li>• PPG output trigger can be generated</li> <li>• Event linking by the ELC</li> </ul> |
|                | Port output enable 3 (POE3a)           | <ul style="list-style-type: none"> <li>• Control of the high-impedance state of the MTU3 waveform output pins</li> <li>• 5 pins for input from signal sources: POE0#, POE4#, POE8#, POE10#, POE11#</li> <li>• Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level)</li> <li>• Initiation by oscillation-stoppage detection or software</li> <li>• Additional programming of output control target pins is enabled</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|                | Programmable pulse generator (PPG)     | <ul style="list-style-type: none"> <li>• (4 bits × 4 groups) × 2 units</li> <li>• Pulse output with the MTU3 or TPU output as a trigger</li> <li>• Maximum of 32 pulse-output possible</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

**Table 1.1 Outline of Specifications (6/10)**

| Classification         | Module/Function                                 | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------------------------|-------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Timers                 | 8-bit timers (TMRb)                             | <ul style="list-style-type: none"> <li>• (8 bits × 2 channels) × 2 units</li> <li>• Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal</li> <li>• Capable of output of pulse trains with desired duty cycles or of PWM signals</li> <li>• The 2 channels of each unit can be cascaded to create a 16-bit timer</li> <li>• Generation of triggers for A/D converter conversion</li> <li>• Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12</li> <li>• Event linking by the ELC</li> </ul> |
|                        | Compare match timer (CMT)                       | <ul style="list-style-type: none"> <li>• (16 bits × 2 channels) × 2 units</li> <li>• Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512)</li> <li>• Event linking by the ELC</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                |
|                        | Compare match timer W (CMTW)                    | <ul style="list-style-type: none"> <li>• (32 bits × 1 channel) × 2 units</li> <li>• Compare-match, input-capture input, and output-comparison output are available.</li> <li>• Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512)</li> <li>• Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events.</li> <li>• Event linking by the ELC</li> </ul>                                                                                                                                                               |
|                        | Realtime clock (RTCd)*4                         | <ul style="list-style-type: none"> <li>• Clock sources: Main clock, sub clock</li> <li>• Selection of the 32-bit binary count in time count/second unit possible</li> <li>• Clock and calendar functions</li> <li>• Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt</li> <li>• Battery backup operation</li> <li>• Time-capture facility for three values</li> <li>• Event linking by the ELC</li> </ul>                                                                                                                                                                       |
|                        | Watchdog timer (WDTA)                           | <ul style="list-style-type: none"> <li>• 14 bits × 1 channel</li> <li>• Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192)</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                       |
|                        | Independent watchdog timer (IWDtA)              | <ul style="list-style-type: none"> <li>• 14 bits × 1 channel</li> <li>• Counter-input clock: IWDt-dedicated on-chip oscillator</li> <li>• Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256</li> <li>• Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled).</li> <li>• Event linking by the ELC</li> </ul>                                                                                                                 |
| Communication function | Ethernet controller (ETHERC)                    | <ul style="list-style-type: none"> <li>• Input and output of Ethernet/IEEE 802.3 frames</li> <li>• Transfer at 10 or 100 Mbps</li> <li>• Full- and half-duplex modes</li> <li>• MII (Media Independent Interface) or RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u</li> <li>• Detection of Magic Packets<sup>TM*1</sup> or output of a “wake-on-LAN” signal (WOL)</li> <li>• Compliance with flow control as defined in IEEE 802.3x standards</li> </ul>                                                                                                                            |
|                        | DMA controller for Ethernet controller (EDMACa) | <ul style="list-style-type: none"> <li>• Alleviation of CPU load by the descriptor control method</li> <li>• Transmission FIFO: 2 Kbytes; Reception FIFO: 2 Kbytes</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                              |
|                        | USB 2.0 FS host/function module (USBb)          | <ul style="list-style-type: none"> <li>• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 FS</li> <li>• One port</li> <li>• Compliance with the USB 2.0 specification</li> <li>• Transfer rate: Full speed (12 Mbps), low speed (1.5 Mbps) (host only)</li> <li>• Both self-powered mode and bus-powered mode are supported</li> <li>• OTG (On the Go) operation is possible (low-speed is not supported)</li> <li>• Incorporates 2 Kbytes of RAM as a transfer buffer</li> <li>• External pull-up and pull-down resistors are not required</li> </ul>                                   |

**Table 1.1 Outline of Specifications (7/10)**

| Classification         | Module/Function                                      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------------------------|------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Communication function | Serial communications interfaces (SCIg, SCIlh, SCli) | <ul style="list-style-type: none"> <li>13 channels (SCIg: 10 channels + SCIlh: 1 channel + SCli: 2 channels)</li> <li>SCIg, SCIlh, SCli</li> </ul> <p>Serial communications modes: Asynchronous, clock synchronous, and smart-card interface</p> <p>Multi-processor function</p> <p>On-chip baud rate generator allows selection of the desired bit rate</p> <p>Choice of LSB-first or MSB-first transfer</p> <p>Start-bit detection: Level or edge detection is selectable.</p> <p>Simple I<sup>2</sup>C</p> <p>Simple SPI</p> <p>9-bit transfer mode</p> <p>Bit rate modulation</p> <p>Double-speed mode</p> <ul style="list-style-type: none"> <li>SCIg, SCIlh</li> </ul> <p>Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12</p> <p>Event linking by the ELC (only on channel 5)</p> <ul style="list-style-type: none"> <li>SCIlh</li> </ul> <p>Supports the serial communications protocol, which contains the start frame and information frame</p> <p>Supports the LIN format</p> <ul style="list-style-type: none"> <li>SCli</li> </ul> <p>Data can be transmitted or received in sequence by the 16-byte FIFO buffers of the transmission and reception unit</p> |
|                        | I <sup>2</sup> C bus interface (RIICa)               | <ul style="list-style-type: none"> <li>3 channels (only channel 0 can be used in fast-mode plus)</li> </ul> <p>Communication formats</p> <p>I<sup>2</sup>C bus format/SMBus format</p> <p>Supports the multi-master</p> <p>Max. transfer rate: 1 Mbps (channel 0)</p> <ul style="list-style-type: none"> <li>Event linking by the ELC</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|                        | CAN module (CAN)                                     | <ul style="list-style-type: none"> <li>2 channels</li> <li>Compliance with the ISO11898-1 specification (standard frame and extended frame)</li> <li>32 mailboxes per channel</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                        | Serial peripheral interface (RSPIC)                  | <ul style="list-style-type: none"> <li>3 channels</li> </ul> <p>RSPI transfer facility</p> <p>Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines)</p> <p>Capable of handling serial transfer as a master or slave</p> <ul style="list-style-type: none"> <li>Data formats</li> </ul> <p>Switching between MSB first and LSB first</p> <p>The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits.</p> <p>128-bit buffers for transmission and reception</p> <p>Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits)</p> <p>Transit/receive data can be swapped in byte units</p> <ul style="list-style-type: none"> <li>Buffered structure</li> </ul> <p>Double buffers for both transmission and reception</p> <ul style="list-style-type: none"> <li>RSPCK can be stopped with the receive buffer full for master reception.</li> <li>Event linking by the ELC</li> </ul>                            |
|                        | Quad serial peripheral interface (QSPI)              | <ul style="list-style-type: none"> <li>1 channel</li> <li>Connectable with serial flash memory equipped with multiple input and output lines (i.e. for single, dual, or quad operation)</li> <li>Programmable bit length and selectable active sense and phase of the clock signal</li> <li>Sequential execution of transfer</li> <li>LSB or MSB first is selectable</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

**Table 1.1 Outline of Specifications (8/10)**

| Classification                   | Module/Function | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------------------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SD host interface (SDHI)*3       |                 | <ul style="list-style-type: none"> <li>• 1 channel</li> <li>• Transfer speed: Supports high-speed mode (25 MB/s) and default speed mode (12.5 MB/s)</li> <li>• One interface for SD memory and I/O cards (supporting 1- and 4-bit SD buses)</li> <li>• SD specifications               <ul style="list-style-type: none"> <li>Part 1: Physical Layer Specification Ver. 3.01 compliant (DDR not supported)</li> <li>Part E1: SDIO Specification Ver. 3.00</li> </ul> </li> <li>• Error checking: CRC7 for commands and CRC16 for data</li> <li>• Interrupt requests: Card access interrupt, SDIO access interrupt, card detection interrupt, SD buffer access interrupt</li> <li>• DMA transfer requests: SD_BUF write and SD_BUF read</li> <li>• Support for card detection and write protection</li> </ul>                                                                                                                                                    |
| SD slave interface (SDSI)*3      |                 | <ul style="list-style-type: none"> <li>• 1 channel</li> <li>• Compliant with the SDIO Card Specification Ver.2.00 (CSA is not supported)</li> <li>• 1-bit SD/4-bit SD/SPI mode</li> <li>• SDIO Proprietary command is supported</li> <li>• SD/SPI Mandatory command is supported</li> <li>• Interrupt requests: 6</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| MMC host interface (MMCIF)       |                 | <ul style="list-style-type: none"> <li>• 1 channel</li> <li>• Transfer speed: Data transfer mode (30 MB/s), backward compatible mode (25 MB/s)</li> <li>• Compliant with JEDEC STANDARD JESD84-A441 (DDR is not supported)</li> <li>• Interface for Multimedia Cards (MMCs)</li> <li>• Device buses: Support for 1-, 4-, and 8-bit MMC buses</li> <li>• Interrupt requests: Card detection interrupt, error/timeout interrupt, normal operation interrupt, MMCIF buffer access interrupt</li> <li>• DMA transfer requests: CE_DATA write and CE_DATA read</li> <li>• Support for card detection, boot operation, high priority interrupt (HPI)</li> </ul>                                                                                                                                                                                                                                                                                                       |
| Parallel data capture unit (PDC) |                 | <ul style="list-style-type: none"> <li>• 1 channel</li> <li>• Acquisition of synchronization through external 8-bit horizontal and vertical synchronization signals</li> <li>• Setting of the image size when clipping of the output for a one-frame image is required</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| Graphic-LCD controller (GLCDC)   |                 | <ul style="list-style-type: none"> <li>• 1 channel</li> <li>• Various data formats and LCD panels are supported</li> <li>• Superposition of 3 planes (single-color background, graphic 1, graphic 2)</li> <li>• 32- and 16-bpp graphics data and 8-, 4-, and 1-bit CLUT data formats are supported</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 2D drawing engine (DRW2D)        |                 | <ul style="list-style-type: none"> <li>• 1 channel</li> <li>• Vector drawing (straight lines, triangles, and circles)</li> <li>• Bit blitting (with support for filling, copying, stretching, and rotation)</li> <li>• Bus master function for input and output of frame buffer data               <ul style="list-style-type: none"> <li>32-, 16-, and 8-bit pixel graphics data are supported</li> </ul> </li> <li>• Bus master function for input of texture data               <ul style="list-style-type: none"> <li>Input of texture data (32, 24, 16, 8, 4, 2, or 1 bit) are supported.</li> <li>Run length encoding is supported</li> <li>A CLUT is installed and index data can be converted into color data</li> </ul> </li> <li>• Two rendering modes are supported (register mode and display list mode)</li> <li>• Performance counting</li> <li>• Interrupts in response to completion of rendering and processing of the display list</li> </ul> |

**Table 1.1 Outline of Specifications (9/10)**

| Classification                 | Module/Function                       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|--------------------------------|---------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12-bit A/D converter (S12ADFa) |                                       | <ul style="list-style-type: none"> <li>12 bits × 2 units (unit 0: 8 channels; unit 1: 21 channels)</li> <li>12-bit resolution (switchable between 8, 10, and 12 bits)</li> <li>Conversion time               <ul style="list-style-type: none"> <li>0.48 μs per channel (for 12-bit conversion)</li> <li>0.45 μs per channel (for 10-bit conversion)</li> <li>0.42 μs per channel (for 8-bit conversion)</li> </ul> </li> <li>Operating mode               <ul style="list-style-type: none"> <li>Scan mode (single scan mode, continuous scan mode, or 3 group scan mode)</li> <li>Group priority control (only for 3 group scan mode)</li> </ul> </li> <li>Sample-and-hold function               <ul style="list-style-type: none"> <li>Common sample-and-hold circuit included</li> <li>In addition, channel-dedicated sample-and-hold function (3 channels: in unit 0 only) included</li> </ul> </li> <li>Sampling variable               <ul style="list-style-type: none"> <li>Sampling time can be set up for each channel.</li> </ul> </li> <li>Digital comparison               <ul style="list-style-type: none"> <li>Method: Comparison to detect voltages above or below thresholds and window comparison</li> <li>Measurement: Comparison of two results of conversion or comparison of a value in the comparison register and a result of conversion</li> </ul> </li> <li>Self-diagnostic function               <ul style="list-style-type: none"> <li>The self-diagnostic function internally generates three analog input voltages (unit 0: VREFL0, VREFH0 × 1/2, VREFH0; unit 1: AVSS1, AVCC1 × 1/2, AVCC1)</li> </ul> </li> <li>Double trigger mode (A/D conversion data duplicated)</li> <li>Detection of analog input disconnection</li> <li>Three ways to start A/D conversion               <ul style="list-style-type: none"> <li>Software trigger, timer (MTU3, TMR, TPU) trigger, external trigger</li> </ul> </li> <li>Event linking by the ELC</li> </ul> |
|                                |                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|                                |                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|                                |                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 12-bit D/A converter (R12DA)   |                                       | <ul style="list-style-type: none"> <li>2 channels</li> <li>12-bit resolution</li> <li>Output voltage: 0.2 V to AVCC1 – 0.2 V (buffered output), 0 V to AVCC1 (unbuffered output)</li> <li>Buffered output or unbuffered output can be selected.</li> <li>Event linking by the ELC</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Temperature sensor             |                                       | <ul style="list-style-type: none"> <li>1 channel</li> <li>Relative precision: ± 1°C</li> <li>The voltage of the temperature is converted into a digital value by the 12-bit A/D converter (unit 1).</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Safety                         | Memory protection unit (MPU)          | <ul style="list-style-type: none"> <li>Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh.</li> <li>Minimum protection unit: 16 bytes</li> <li>Reading from, writing to, and enabling the execution access can be specified for each area.</li> <li>An access exception occurs when the detected access is not in the permitted area.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|                                | Trusted Memory (TM) Function          | <ul style="list-style-type: none"> <li>Programs in the TM target area in the code flash memory are protected against reading</li> <li>Instruction fetching by the CPU is the only form of access to these areas when the TM function is enabled.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|                                | Register write protection function    | <ul style="list-style-type: none"> <li>Protects important registers from being overwritten for in case a program runs out of control.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|                                | CRC calculator (CRCA)                 | <ul style="list-style-type: none"> <li>Generation of CRC codes for 8-/32-bit data</li> <li>8-bit data               <ul style="list-style-type: none"> <li>Selectable from the following three polynomials</li> <li><math>X^8 + X^2 + X + 1</math>, <math>X^{16} + X^{15} + X^2 + 1</math>, <math>X^{16} + X^{12} + X^5 + 1</math></li> </ul> </li> <li>32-bit data               <ul style="list-style-type: none"> <li>Selectable from the following two polynomials</li> <li><math>X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1</math>,</li> <li><math>X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1</math></li> </ul> </li> <li>Generation of CRC codes for use with LSB-first or MSB-first communications is selectable</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|                                | Main clock oscillation stop detection | <ul style="list-style-type: none"> <li>Main clock oscillation stop detection: Available</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

**Table 1.1 Outline of Specifications (10/10)**

| Classification        | Module/Function                                    | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-----------------------|----------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Safety                | Clock frequency accuracy measurement circuit (CAC) | <ul style="list-style-type: none"> <li>Monitors the clock output from the main clock oscillator, sub-clock oscillator, low- and high-speed on-chip oscillators, IWDT-dedicated on-chip oscillator, and PCLKB, and generates interrupts when the setting range is exceeded.</li> </ul>                                                                                                                                                                                                              |
|                       | Data operation circuit (DOC)                       | <ul style="list-style-type: none"> <li>The function to compare, add, or subtract 16-bit data</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                            |
| Encryption function   | AESa*2                                             | <ul style="list-style-type: none"> <li>Key lengths: 128, 192, and 256 bits</li> <li>Support for CFB, OFB, and CMAC operating modes</li> <li>Speed of calculations:               <ul style="list-style-type: none"> <li>128-bit key length in 22 cycles</li> <li>192-bit key length in 26 cycles</li> <li>256-bit key length in 30 cycles</li> </ul> </li> <li>Compliant with FIPS PUB 197</li> </ul>                                                                                              |
|                       | True random number generator (RNG)*2               | <ul style="list-style-type: none"> <li>Length of random numbers: 16 bits</li> <li>Generation of random-number-generated interrupts after a number is generated</li> <li>Random number generation time: 1.9 ms (typ)</li> </ul>                                                                                                                                                                                                                                                                     |
|                       | Trusted Secure IP (TSIP)*2                         | <ul style="list-style-type: none"> <li>Security algorithm               <ul style="list-style-type: none"> <li>Common key encryption: AES (compliant with NIST FIPS PUB 197), 3DES, ARC4</li> <li>Non-common key encryption: RSA</li> </ul> </li> <li>Other features               <ul style="list-style-type: none"> <li>TRNG (true-random number generator)</li> <li>Hash value generation: SHA1, SHA224, SHA256, GHASH</li> <li>Prevention from illicit copying of a key</li> </ul> </li> </ul> |
| Operating frequency   |                                                    | Up to 120 MHz                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| Power supply voltage  |                                                    | VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$ , $V_{BATT} = 1.62$ to $3.6$ V*6                                                                                                                                                                                                                                                                                                                                                                                        |
| Operating temperature |                                                    | D-version: -40 to +85°C<br>G-version: -40 to +105°C*5                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Package               |                                                    | 177-pin TFLGA (PTLG0177KA-A)<br>176-pin LFBGA (PLBG0176GA-A)<br>176-pin LFQFP (PLQP0176KB-A)<br>145-pin TFLGA (PTLG0145KA-A)<br>144-pin LFQFP (PLQP0144KA-B)<br>100-pin TFLGA (PTLG0100JA-A)<br>100-pin LFQFP (PLQP0100KB-B)<br>64-pin TFBGA (PTBG0064KB-A)<br>64-pin LFQFP (PLQP0064KB-C)                                                                                                                                                                                                         |
| Debugging interface   |                                                    | JTAG and FINE interfaces                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.

Note 2. The product part number differs according to whether or not the MCU includes the encryption function.

Note 3. The product part number differs according to whether or not the MCU includes an SDHI (SD host interface)/SDSI (SD slave interface) (products with 1 Mbyte of code flash memory or less).

Note 4. When the realtime clock is not used, initialize the registers in the time clock according to description in section 31.6.7, Initialization Procedure When the Realtime Clock is Not to be Used in the User's Manual: Hardware.

Note 5. Please contact us if you are using a G-version product.

Note 6. The low CL crystal unit cannot be used when the  $V_{BATT}$  voltage is less than 2.0 V.

**Table 1.2 Code Flash Memory Capacity and Comparison of Functions for Different Packages (1/2)**

| Functions              | Products                                   | Products with 1 Mbyte of code flash memory or less |                           |                        | Products with at least 1.5 Mbytes of code flash memory   |                    |                           |                        |
|------------------------|--------------------------------------------|----------------------------------------------------|---------------------------|------------------------|----------------------------------------------------------|--------------------|---------------------------|------------------------|
|                        | Package                                    | 145 Pins, 144 Pins                                 | 100 Pins                  | 64 Pins                | 177 Pins, 176 Pins                                       | 145 Pins, 144 Pins | 100 Pins                  | 64 Pins                |
| Code Flash Memory      | Code Flash Memory Capacity                 | 512 Kbytes/768 Kbytes /1 Mbyte                     |                           |                        | 1.5 Mbytes/2 Mbytes                                      |                    |                           |                        |
|                        | Dual bank function                         | Not available                                      |                           |                        | Available                                                |                    |                           |                        |
|                        | BGO function                               | Not available                                      |                           |                        | Available                                                |                    |                           |                        |
| Data Flash Memory      |                                            | Not available                                      |                           |                        | 32 Kbytes                                                |                    |                           |                        |
| RAM                    |                                            | 256 Kbytes                                         |                           |                        | 640 Kbytes<br>(256 Kbytes + 384 Kbytes of expansion RAM) |                    |                           |                        |
| External bus           | External bus width                         | 16/8 bits                                          |                           | Not available          | 32/16/8 bits                                             | 16/8 bits          |                           | Not available          |
|                        | SDRAM area controller                      | Available                                          | Not available             |                        | Available                                                |                    | Not available             |                        |
| DMA                    | DMA controller                             | Ch. 0 to 7                                         |                           |                        |                                                          |                    |                           |                        |
|                        | Data transfer controller                   | Available                                          |                           |                        |                                                          |                    |                           |                        |
|                        | EXDMA controller                           | Ch. 0 and 1                                        |                           | Not available          | Ch. 0 and 1                                              |                    | Not available             |                        |
| Timers                 | 16-bit timer pulse unit                    | Ch. 0 to 5                                         |                           |                        |                                                          |                    |                           |                        |
|                        | Multi-function timer pulse unit 3          | Ch. 0 to 8                                         |                           |                        |                                                          |                    |                           |                        |
|                        | Port output enable 3                       | Available                                          |                           |                        |                                                          |                    |                           |                        |
|                        | Programmable pulse generator               | Ch. 0 and 1                                        |                           | Not available          | Ch. 0 and 1                                              |                    | Not available             |                        |
|                        | 8-bit timers                               | Ch. 0 to 3                                         |                           |                        |                                                          |                    |                           |                        |
|                        | Compare match timer                        | Ch. 0 to 3                                         |                           |                        |                                                          |                    |                           |                        |
|                        | Compare match timer W                      | Ch. 0 and 1                                        |                           |                        |                                                          |                    |                           |                        |
|                        | Realtime clock                             | Available                                          |                           |                        |                                                          |                    |                           |                        |
|                        | Watchdog timer                             | Available                                          |                           |                        |                                                          |                    |                           |                        |
|                        | Independent watchdog timer                 | Available                                          |                           |                        |                                                          |                    |                           |                        |
| Communication function | Ethernet controller                        | Ch. 0 (only for RX65N group)                       |                           | Not available          | Ch. 0 (only for RX65N group)                             |                    | Not available             |                        |
|                        | DMA Controller for the Ethernet Controller | Ch. 0 (only for RX65N group)                       |                           | Not available          | Ch. 0 (only for RX65N group)                             |                    | Not available             |                        |
|                        | USB 2.0 FS host/function module            | Ch. 0                                              |                           | Ch. 0*1                | Ch. 0                                                    |                    | Ch. 0*1                   |                        |
|                        | Serial communications interfaces (SCIg)    | Ch. 0 to 9                                         | Ch. 0 to 3, 5, 6, 8 and 9 | Ch. 1 to 3, 5, 8 and 9 | Ch. 0 to 9                                               |                    | Ch. 0 to 3, 5, 6, 8 and 9 | Ch. 1 to 3, 5, 8 and 9 |
|                        | Serial communications interfaces (SCIh)    | Ch. 12                                             |                           |                        |                                                          |                    |                           |                        |
|                        | Serial communications interfaces (SCIl)    | Ch. 10 and 11                                      |                           |                        |                                                          |                    |                           |                        |
|                        | I <sup>2</sup> C bus interfaces            | Ch. 0 and 2                                        |                           |                        | Ch. 0 to 2                                               |                    | Ch. 0 and 2               |                        |
|                        | Serial peripheral interface                | Ch. 0 to 2                                         |                           | Ch. 0 and 1            | Ch. 0 to 2                                               |                    | Ch. 0 and 1               |                        |
|                        | CAN module                                 | Ch. 0 and 1                                        |                           | Not available          | Ch. 0 and 1                                              |                    | Not available             |                        |
|                        | Quad serial peripheral interface           | Ch. 0                                              |                           |                        |                                                          |                    |                           |                        |
|                        | SD host interface                          | Available                                          |                           |                        |                                                          |                    |                           |                        |
|                        | SD slave interface                         | Available                                          |                           | Not available          | Available                                                |                    | Not available             |                        |

**Table 1.2 Code Flash Memory Capacity and Comparison of Functions for Different Packages (2/2)**

| Functions                                        | Products                   | Products with 1 Mbyte of code flash memory or less                      |                                                                         |                                                                                  | Products with at least 1.5 Mbytes of code flash memory                  |                    |                                                                         |                                                                                  |
|--------------------------------------------------|----------------------------|-------------------------------------------------------------------------|-------------------------------------------------------------------------|----------------------------------------------------------------------------------|-------------------------------------------------------------------------|--------------------|-------------------------------------------------------------------------|----------------------------------------------------------------------------------|
|                                                  | Package                    | 145 Pins, 144 Pins                                                      | 100 Pins                                                                | 64 Pins                                                                          | 177 Pins, 176 Pins                                                      | 145 Pins, 144 Pins | 100 Pins                                                                | 64 Pins                                                                          |
| Communication function                           | MMC host interface         | Available                                                               |                                                                         | Not available                                                                    | Available                                                               |                    |                                                                         | Not available                                                                    |
|                                                  | Parallel data capture unit | Available                                                               | Not available                                                           |                                                                                  | Available                                                               |                    | Not available                                                           |                                                                                  |
| Graphics                                         | Graphic-LCD controller     | Not available                                                           |                                                                         |                                                                                  | Available                                                               |                    |                                                                         | Not available                                                                    |
|                                                  | 2D drawing engine          | Not available                                                           |                                                                         |                                                                                  | Available                                                               |                    |                                                                         | Not available                                                                    |
| 12-bit A/D converter                             |                            | AN000 to 007 (unit 0: 8 channels)<br>AN100 to 120 (unit 1: 21 channels) | AN000 to 007 (unit 0: 8 channels)<br>AN100 to 113 (unit 1: 14 channels) | AN000 to 003 (unit 0: 4 channels)<br>AN106, 107, 110 to 113 (unit 1: 6 channels) | AN000 to 007 (unit 0: 8 channels)<br>AN100 to 120 (unit 1: 21 channels) |                    | AN000 to 007 (unit 0: 8 channels)<br>AN100 to 113 (unit 1: 14 channels) | AN000 to 003 (unit 0: 4 channels)<br>AN106, 107, 110 to 113 (unit 1: 6 channels) |
| 12-bit D/A converter                             |                            | Ch. 0 and 1                                                             | Ch. 1*2                                                                 |                                                                                  | Ch. 0 and 1                                                             |                    | Ch. 1*2                                                                 |                                                                                  |
| Temperature sensor                               |                            | Available                                                               |                                                                         |                                                                                  |                                                                         |                    |                                                                         |                                                                                  |
| CRC calculator                                   |                            | Available                                                               |                                                                         |                                                                                  |                                                                         |                    |                                                                         |                                                                                  |
| Data operation circuit                           |                            | Available                                                               |                                                                         |                                                                                  |                                                                         |                    |                                                                         |                                                                                  |
| Clock frequency accuracy measurement circuit     |                            | Available                                                               |                                                                         |                                                                                  |                                                                         |                    |                                                                         |                                                                                  |
| Encryption                                       | AES                        | Available*3                                                             |                                                                         |                                                                                  | Incorporated in the Trusted Secure IP                                   |                    |                                                                         |                                                                                  |
|                                                  | RNG                        | Available*3                                                             |                                                                         |                                                                                  | Incorporated in the Trusted Secure IP                                   |                    |                                                                         |                                                                                  |
|                                                  | Trusted Secure IP          | Not available                                                           |                                                                         |                                                                                  | Available                                                               |                    |                                                                         |                                                                                  |
| Event link controller                            |                            | Available                                                               |                                                                         |                                                                                  |                                                                         |                    |                                                                         |                                                                                  |
| Off-board programming (parallel programmer mode) |                            | Available                                                               |                                                                         | Not available                                                                    | Available                                                               |                    |                                                                         | Not available                                                                    |

Note 1. Only supports the function controller.

Note 2. Not provided on the 64-pin TFBGA.

Note 3. Regarding the public release of this module, an exchange of non-disclosure agreement is necessary. For details, contact your Renesas sales agency.

## 1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

**Table 1.3 List of Products (1/12)**

| Group             | Part No.     | Package      | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI     | Dual bank     | Operating temperature (°C) |
|-------------------|--------------|--------------|--------------------------------------|------------------------|--------------------------------------|----------------------------|-------------------|---------------|---------------|----------------------------|
| RX65N (D version) | R5F565NEDDFC | PLQP0176KB-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                   | R5F565NEHDFC | PLQP0176KB-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                   | R5F565NCDDFC | PLQP0176KB-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                   | R5F565NCHDFC | PLQP0176KB-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                   | R5F565NEDDFB | PLQP0144KA-B | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                   | R5F565NEHDFB | PLQP0144KA-B | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                   | R5F565NCDDFB | PLQP0144KA-B | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                   | R5F565NCHDFB | PLQP0144KA-B | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                   | R5F565N9ADFB | PLQP0144KA-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                   | R5F565N9BDFB | PLQP0144KA-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                   | R5F565N9EDFB | PLQP0144KA-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                   | R5F565N9FDFB | PLQP0144KA-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                   | R5F565N7ADFB | PLQP0144KA-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                   | R5F565N7BDFB | PLQP0144KA-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                   | R5F565N7EDFB | PLQP0144KA-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                   | R5F565N7FDFB | PLQP0144KA-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                   | R5F565N4ADFB | PLQP0144KA-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                   | R5F565N4BDFB | PLQP0144KA-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                   | R5F565N4EDFB | PLQP0144KA-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                   | R5F565N4FDFB | PLQP0144KA-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                   | R5F565NEDDFP | PLQP0100KB-B | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                   | R5F565NEHDFP | PLQP0100KB-B | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                   | R5F565NCDDFP | PLQP0100KB-B | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                   | R5F565NCHDFP | PLQP0100KB-B | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                   | R5F565N9ADFP | PLQP0100KB-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                   | R5F565N9BDFP | PLQP0100KB-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                   | R5F565N9EDFP | PLQP0100KB-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                   | R5F565N9FDFP | PLQP0100KB-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |

Table 1.3 List of Products (2/12)

| Group                | Part No.     | Package      | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI     | Dual bank     | Operating temperature (°C) |
|----------------------|--------------|--------------|--------------------------------------|------------------------|--------------------------------------|----------------------------|-------------------|---------------|---------------|----------------------------|
| RX65N<br>(D version) | R5F565N7ADFP | PLQP0100KB-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                      | R5F565N7BDFP | PLQP0100KB-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                      | R5F565N7EDFP | PLQP0100KB-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                      | R5F565N7FDFP | PLQP0100KB-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                      | R5F565N4ADFP | PLQP0100KB-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                      | R5F565N4BDFP | PLQP0100KB-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                      | R5F565N4EDFP | PLQP0100KB-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                      | R5F565N4FDFP | PLQP0100KB-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                      | R5F565NEEDBG | PLBG0176GA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                      | R5F565NEHDBG | PLBG0176GA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                      | R5F565NCDDBG | PLBG0176GA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                      | R5F565NCHDBG | PLBG0176GA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                      | R5F565NEDDLK | PTLG0177KA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                      | R5F565NEHDLK | PTLG0177KA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                      | R5F565NCDDLK | PTLG0177KA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                      | R5F565NCHDLK | PTLG0177KA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                      | R5F565NEDDLK | PTLG0145KA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                      | R5F565NEHDLK | PTLG0145KA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                      | R5F565NCDDLK | PTLG0145KA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                      | R5F565NCHDLK | PTLG0145KA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                      | R5F565N9ADLK | PTLG0145KA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                      | R5F565N9BDLK | PTLG0145KA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                      | R5F565N9EDLK | PTLG0145KA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                      | R5F565N9FDLK | PTLG0145KA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                      | R5F565N7ADLK | PTLG0145KA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                      | R5F565N7BDLK | PTLG0145KA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                      | R5F565N7EDLK | PTLG0145KA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                      | R5F565N7FDLK | PTLG0145KA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                      | R5F565N4ADLK | PTLG0145KA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                      | R5F565N4BDLK | PTLG0145KA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |

Table 1.3 List of Products (3/12)

| Group                | Part No.     | Package      | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI     | Dual bank     | Operating temperature (°C) |
|----------------------|--------------|--------------|--------------------------------------|------------------------|--------------------------------------|----------------------------|-------------------|---------------|---------------|----------------------------|
| RX65N<br>(D version) | R5F565N4EDLK | PTLG0145KA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                      | R5F565N4FDLK | PTLG0145KA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                      | R5F565NEDDLJ | PTLG0100JA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                      | R5F565NEHDLJ | PTLG0100JA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                      | R5F565NCDDLJ | PTLG0100JA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                      | R5F565NCHDLJ | PTLG0100JA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                      | R5F565N9ADLJ | PTLG0100JA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                      | R5F565N9BDLJ | PTLG0100JA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                      | R5F565N9EDLJ | PTLG0100JA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                      | R5F565N9FDLJ | PTLG0100JA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                      | R5F565N7ADLJ | PTLG0100JA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                      | R5F565N7BDLJ | PTLG0100JA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                      | R5F565N7EDLJ | PTLG0100JA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                      | R5F565N7FDLJ | PTLG0100JA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                      | R5F565N4ADLJ | PTLG0100JA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                      | R5F565N4BDLJ | PTLG0100JA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                      | R5F565N4EDLJ | PTLG0100JA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                      | R5F565N4FDLJ | PTLG0100JA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
| RX65N<br>(G version) | R5F565NEDGFC | PLQP0176KB-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F565NEHGFC | PLQP0176KB-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                      | R5F565NCDGFC | PLQP0176KB-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F565NCHGFC | PLQP0176KB-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                      | R5F565NEDGFB | PLQP0144KA-B | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F565NEHGFB | PLQP0144KA-B | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                      | R5F565NCDGFB | PLQP0144KA-B | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F565NCHGFB | PLQP0144KA-B | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                      | R5F565N9AGFB | PLQP0144KA-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                      | R5F565N9BGFB | PLQP0144KA-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                      | R5F565N9EGFB | PLQP0144KA-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                      | R5F565N9FGFB | PLQP0144KA-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |

Table 1.3 List of Products (4/12)

| Group                | Part No.     | Package      | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI     | Dual bank     | Operating temperature (°C) |
|----------------------|--------------|--------------|--------------------------------------|------------------------|--------------------------------------|----------------------------|-------------------|---------------|---------------|----------------------------|
| RX65N<br>(G version) | R5F565N7AGFB | PLQP0144KA-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                      | R5F565N7BGFB | PLQP0144KA-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                      | R5F565N7EGFB | PLQP0144KA-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                      | R5F565N7FGFB | PLQP0144KA-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
|                      | R5F565N4AGFB | PLQP0144KA-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                      | R5F565N4BGFB | PLQP0144KA-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                      | R5F565N4EGFB | PLQP0144KA-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                      | R5F565N4FGFB | PLQP0144KA-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
|                      | R5F565NEDGFP | PLQP0100KB-B | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F565NEHGFP | PLQP0100KB-B | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                      | R5F565NCDGFP | PLQP0100KB-B | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F565NCHGFP | PLQP0100KB-B | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                      | R5F565N9AGFP | PLQP0100KB-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                      | R5F565N9BGFP | PLQP0100KB-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                      | R5F565N9EGFP | PLQP0100KB-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                      | R5F565N9FGFP | PLQP0100KB-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
|                      | R5F565N7AGFP | PLQP0100KB-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                      | R5F565N7BGFP | PLQP0100KB-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                      | R5F565N7EGFP | PLQP0100KB-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                      | R5F565N7FGFP | PLQP0100KB-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
|                      | R5F565N4AGFP | PLQP0100KB-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                      | R5F565N4BGFP | PLQP0100KB-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                      | R5F565N4EGFP | PLQP0100KB-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                      | R5F565N4FGFP | PLQP0100KB-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
|                      | R5F565NEDGBG | PLBG0176GA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F565NEHGBG | PLBG0176GA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                      | R5F565NCDGBG | PLBG0176GA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F565NCHGBG | PLBG0176GA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                      | R5F565NEDGLC | PTLG0177KA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F565NEHGLC | PTLG0177KA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |

Table 1.3 List of Products (5/12)

| Group                | Part No.     | Package      | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI     | Dual bank     | Operating temperature (°C) |
|----------------------|--------------|--------------|--------------------------------------|------------------------|--------------------------------------|----------------------------|-------------------|---------------|---------------|----------------------------|
| RX65N<br>(G version) | R5F565NCDGLC | PTLG0177KA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F565NCHGLC | PTLG0177KA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                      | R5F565NEDGLK | PTLG0145KA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F565NEHGLK | PTLG0145KA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                      | R5F565NCDGLK | PTLG0145KA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F565NCHGLK | PTLG0145KA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                      | R5F565N9AGLK | PTLG0145KA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                      | R5F565N9BGLK | PTLG0145KA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                      | R5F565N9EGLK | PTLG0145KA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                      | R5F565N9FGLK | PTLG0145KA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
|                      | R5F565N7AGLK | PTLG0145KA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                      | R5F565N7BGLK | PTLG0145KA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                      | R5F565N7EGLK | PTLG0145KA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                      | R5F565N7FGLK | PTLG0145KA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
|                      | R5F565N4AGLK | PTLG0145KA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                      | R5F565N4BGLK | PTLG0145KA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                      | R5F565N4EGLK | PTLG0145KA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                      | R5F565N4FGLK | PTLG0145KA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
|                      | R5F565NEDGLJ | PTLG0100JA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F565NEHGLJ | PTLG0100JA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                      | R5F565NCDGLJ | PTLG0100JA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F565NCHGLJ | PTLG0100JA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                      | R5F565N9AGLJ | PTLG0100JA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                      | R5F565N9BGLJ | PTLG0100JA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                      | R5F565N9EGLJ | PTLG0100JA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                      | R5F565N9FGLJ | PTLG0100JA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
|                      | R5F565N7AGLJ | PTLG0100JA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                      | R5F565N7BGLJ | PTLG0100JA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                      | R5F565N7EGLJ | PTLG0100JA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |

Table 1.3 List of Products (6/12)

| Group                | Part No.     | Package      | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI     | Dual bank     | Operating temperature (°C) |
|----------------------|--------------|--------------|--------------------------------------|------------------------|--------------------------------------|----------------------------|-------------------|---------------|---------------|----------------------------|
| RX65N<br>(G version) | R5F565N7FGLJ | PTLG0100JA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
|                      | R5F565N4AGLJ | PTLG0100JA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                      | R5F565N4BGLJ | PTLG0100JA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                      | R5F565N4EGLJ | PTLG0100JA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                      | R5F565N4FGLJ | PTLG0100JA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
| RX651<br>(D version) | R5F5651EDDFC | PLQP0176KB-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                      | R5F5651EHDFC | PLQP0176KB-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                      | R5F5651CDDFC | PLQP0176KB-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                      | R5F5651CHDFC | PLQP0176KB-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                      | R5F5651EDDFB | PLQP0144KA-B | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                      | R5F5651EHDFB | PLQP0144KA-B | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                      | R5F5651CDDFB | PLQP0144KA-B | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                      | R5F5651CHDFB | PLQP0144KA-B | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                      | R5F56519ADFB | PLQP0144KA-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                      | R5F56519BDFB | PLQP0144KA-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                      | R5F56519EDFB | PLQP0144KA-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                      | R5F56519FDFB | PLQP0144KA-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                      | R5F56517ADFB | PLQP0144KA-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                      | R5F56517BDFB | PLQP0144KA-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                      | R5F56517EDFB | PLQP0144KA-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                      | R5F56517FDFB | PLQP0144KA-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                      | R5F56514ADFB | PLQP0144KA-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                      | R5F56514BDFB | PLQP0144KA-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                      | R5F56514EDFB | PLQP0144KA-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                      | R5F56514FDFB | PLQP0144KA-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                      | R5F5651EDDFP | PLQP0100KB-B | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                      | R5F5651EHDFP | PLQP0100KB-B | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                      | R5F5651CDDFP | PLQP0100KB-B | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                      | R5F5651CHDFP | PLQP0100KB-B | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |

Table 1.3 List of Products (7/12)

| Group                | Part No.     | Package      | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI     | Dual bank     | Operating temperature (°C) |
|----------------------|--------------|--------------|--------------------------------------|------------------------|--------------------------------------|----------------------------|-------------------|---------------|---------------|----------------------------|
| RX651<br>(D version) | R5F56519ADFP | PLQP0100KB-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                      | R5F56519BDFP | PLQP0100KB-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                      | R5F56519EDFP | PLQP0100KB-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                      | R5F56519FDFP | PLQP0100KB-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                      | R5F56517ADFP | PLQP0100KB-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                      | R5F56517BDFP | PLQP0100KB-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                      | R5F56517EDFP | PLQP0100KB-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                      | R5F56517FDFP | PLQP0100KB-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                      | R5F56514ADFP | PLQP0100KB-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                      | R5F56514BDFP | PLQP0100KB-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                      | R5F56514EDFP | PLQP0100KB-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                      | R5F56514FDFP | PLQP0100KB-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                      | R5F5651EDDFM | PLQP0064KB-C | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available*1   | Available     | –40 to +85                 |
|                      | R5F5651EHDFM | PLQP0064KB-C | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available*1   | Available     | –40 to +85                 |
|                      | R5F5651CDDFM | PLQP0064KB-C | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available*1   | Available     | –40 to +85                 |
|                      | R5F5651CHDFM | PLQP0064KB-C | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available*1   | Available     | –40 to +85                 |
|                      | R5F56519BDFM | PLQP0064KB-C | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available*1   | Not available | –40 to +85                 |
|                      | R5F56519FDFM | PLQP0064KB-C | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available*1   | Not available | –40 to +85                 |
|                      | R5F56517BDFM | PLQP0064KB-C | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available*1   | Not available | –40 to +85                 |
|                      | R5F56517FDFM | PLQP0064KB-C | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available*1   | Not available | –40 to +85                 |
|                      | R5F56514BDFM | PLQP0064KB-C | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available*1   | Not available | –40 to +85                 |
|                      | R5F56514FDFM | PLQP0064KB-C | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available*1   | Not available | –40 to +85                 |
|                      | R5F5651EDDBG | PLBG0176GA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                      | R5F5651EHDBG | PLBG0176GA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                      | R5F5651CDDBG | PLBG0176GA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                      | R5F5651CHDBG | PLBG0176GA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                      | R5F5651EDDBP | PTBG0064KB-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available*1   | Available     | –40 to +85                 |
|                      | R5F5651EHDBP | PTBG0064KB-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available*1   | Available     | –40 to +85                 |
|                      | R5F5651CDDBP | PTBG0064KB-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available*1   | Available     | –40 to +85                 |
|                      | R5F5651CHDBP | PTBG0064KB-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available*1   | Available     | –40 to +85                 |

Table 1.3 List of Products (8/12)

| Group             | Part No.      | Package      | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI     | Dual bank     | Operating temperature (°C) |
|-------------------|---------------|--------------|--------------------------------------|------------------------|--------------------------------------|----------------------------|-------------------|---------------|---------------|----------------------------|
| RX651 (D version) | R5F56519BDBP  | PTBG0064KB-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available*1   | Not available | –40 to +85                 |
|                   | R5F56519FDBP  | PTBG0064KB-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available*1   | Not available | –40 to +85                 |
|                   | R5F56517BDBP  | PTBG0064KB-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available*1   | Not available | –40 to +85                 |
|                   | R5F56517FDBP  | PTBG0064KB-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available*1   | Not available | –40 to +85                 |
|                   | R5F56514BDBP  | PTBG0064KB-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available*1   | Not available | –40 to +85                 |
|                   | R5F56514FDBP  | PTBG0064KB-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available*1   | Not available | –40 to +85                 |
|                   | R5F5651EDDL   | PTLG0177KA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                   | R5F5651EHDLC  | PTLG0177KA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                   | R5F5651CDDL   | PTLG0177KA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                   | R5F5651CHDL   | PTLG0177KA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                   | R5F5651EDDLK  | PTLG0145KA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                   | R5F5651EHDLK  | PTLG0145KA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                   | R5F5651CDDLK  | PTLG0145KA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                   | R5F5651CHDLK  | PTLG0145KA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                   | R5F56519ADLK  | PTLG0145KA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                   | R5F56519BDLK  | PTLG0145KA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                   | R5F56519EDLK  | PTLG0145KA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                   | R5F56519FDLK  | PTLG0145KA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                   | R5F56517ADLK  | PTLG0145KA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                   | R5F56517BDLK  | PTLG0145KA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                   | R5F56517EDLK  | PTLG0145KA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                   | R5F56517FDLK  | PTLG0145KA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                   | R5F56514ADLK  | PTLG0145KA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                   | R5F56514BDLK  | PTLG0145KA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                   | R5F56514EDLK  | PTLG0145KA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                   | R5F56514FDLK  | PTLG0145KA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                   | R5F5651EDDLJ  | PTLG0100JA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                   | R5F5651EHD LJ | PTLG0100JA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |
|                   | R5F5651CDDLJ  | PTLG0100JA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +85                 |
|                   | R5F5651CHDLJ  | PTLG0100JA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +85                 |

Table 1.3 List of Products (9/12)

| Group             | Part No.     | Package      | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI     | Dual bank     | Operating temperature (°C) |
|-------------------|--------------|--------------|--------------------------------------|------------------------|--------------------------------------|----------------------------|-------------------|---------------|---------------|----------------------------|
| RX651 (D version) | R5F56519ADLJ | PTLG0100JA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                   | R5F56519BDLJ | PTLG0100JA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                   | R5F56519EDLJ | PTLG0100JA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                   | R5F56519FDLJ | PTLG0100JA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                   | R5F56517ADLJ | PTLG0100JA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                   | R5F56517BDLJ | PTLG0100JA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                   | R5F56517EDLJ | PTLG0100JA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                   | R5F56517FDLJ | PTLG0100JA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
|                   | R5F56514ADLJ | PTLG0100JA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +85                 |
|                   | R5F56514BDLJ | PTLG0100JA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +85                 |
|                   | R5F56514EDLJ | PTLG0100JA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +85                 |
|                   | R5F56514FDLJ | PTLG0100JA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +85                 |
| RX651 (G version) | R5F5651EDGFC | PLQP0176KB-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                   | R5F5651EHGFC | PLQP0176KB-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                   | R5F5651CDGFC | PLQP0176KB-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                   | R5F5651CHGFC | PLQP0176KB-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                   | R5F5651EDGFB | PLQP0144KA-B | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                   | R5F5651EHGFB | PLQP0144KA-B | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                   | R5F5651CDGFB | PLQP0144KA-B | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                   | R5F5651CHGFB | PLQP0144KA-B | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                   | R5F56519AGFB | PLQP0144KA-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                   | R5F56519BGFB | PLQP0144KA-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                   | R5F56519EGFB | PLQP0144KA-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                   | R5F56519FGFB | PLQP0144KA-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
|                   | R5F56517AGFB | PLQP0144KA-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                   | R5F56517BGFB | PLQP0144KA-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                   | R5F56517EGFB | PLQP0144KA-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                   | R5F56517FGFB | PLQP0144KA-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
|                   | R5F56514AGFB | PLQP0144KA-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                   | R5F56514BGFB | PLQP0144KA-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |

Table 1.3 List of Products (10/12)

| Group                | Part No.     | Package      | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI     | Dual bank     | Operating temperature (°C) |
|----------------------|--------------|--------------|--------------------------------------|------------------------|--------------------------------------|----------------------------|-------------------|---------------|---------------|----------------------------|
| RX651<br>(G version) | R5F56514EGFB | PLQP0144KA-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                      | R5F56514FGFB | PLQP0144KA-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
|                      | R5F5651EDGFP | PLQP0100KB-B | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F5651EHGFP | PLQP0100KB-B | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                      | R5F5651CDGFP | PLQP0100KB-B | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F5651CHGFP | PLQP0100KB-B | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                      | R5F56519AGFP | PLQP0100KB-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                      | R5F56519BGFP | PLQP0100KB-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                      | R5F56519EGFP | PLQP0100KB-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                      | R5F56519FGFP | PLQP0100KB-B | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
|                      | R5F56517AGFP | PLQP0100KB-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                      | R5F56517BGFP | PLQP0100KB-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                      | R5F56517EGFP | PLQP0100KB-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                      | R5F56517FGFP | PLQP0100KB-B | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
|                      | R5F56514AGFP | PLQP0100KB-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | –40 to +105                |
|                      | R5F56514BGFP | PLQP0100KB-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | –40 to +105                |
|                      | R5F56514EGFP | PLQP0100KB-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | –40 to +105                |
|                      | R5F56514FGFP | PLQP0100KB-B | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | –40 to +105                |
|                      | R5F5651EDGFM | PLQP0064KB-C | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available*1   | Available     | –40 to +105                |
|                      | R5F5651EHGFM | PLQP0064KB-C | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available*1   | Available     | –40 to +105                |
|                      | R5F5651CDGFM | PLQP0064KB-C | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available*1   | Available     | –40 to +105                |
|                      | R5F5651CHGFM | PLQP0064KB-C | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available*1   | Available     | –40 to +105                |
|                      | R5F56519BGFM | PLQP0064KB-C | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available*1   | Not available | –40 to +105                |
|                      | R5F56519FGFM | PLQP0064KB-C | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available*1   | Not available | –40 to +105                |
|                      | R5F56517BGFM | PLQP0064KB-C | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available*1   | Not available | –40 to +105                |
|                      | R5F56517FGFM | PLQP0064KB-C | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available*1   | Not available | –40 to +105                |
|                      | R5F56514BGFM | PLQP0064KB-C | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available*1   | Not available | –40 to +105                |
|                      | R5F56514FGFM | PLQP0064KB-C | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available*1   | Not available | –40 to +105                |
|                      | R5F5651EDGBG | PLBG0176GA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |
|                      | R5F5651EHGBG | PLBG0176GA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | –40 to +105                |
|                      | R5F5651CDGBG | PLBG0176GA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | –40 to +105                |

Table 1.3 List of Products (11/12)

| Group             | Part No.     | Package      | Code Flash Memory Capacity (byte(s)) | RAM Capacity (byte(s)) | Data Flash Memory Capacity (byte(s)) | Operating Frequency (Max.) | Encryption Module | SDHI/SDSI     | Dual bank     | Operating temperature (°C) |
|-------------------|--------------|--------------|--------------------------------------|------------------------|--------------------------------------|----------------------------|-------------------|---------------|---------------|----------------------------|
| RX651 (G version) | R5F5651CHGBG | PLBG0176GA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | -40 to +105                |
|                   | R5F5651EDGBP | PTBG0064KB-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available*1   | Available     | -40 to +105                |
|                   | R5F5651EHGBP | PTBG0064KB-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available*1   | Available     | -40 to +105                |
|                   | R5F5651CDGBP | PTBG0064KB-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available*1   | Available     | -40 to +105                |
|                   | R5F5651CHGBP | PTBG0064KB-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available*1   | Available     | -40 to +105                |
|                   | R5F56519BGBP | PTBG0064KB-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available*1   | Not available | -40 to +105                |
|                   | R5F56519FGBP | PTBG0064KB-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available*1   | Not available | -40 to +105                |
|                   | R5F56517BGBP | PTBG0064KB-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available*1   | Not available | -40 to +105                |
|                   | R5F56517FGBP | PTBG0064KB-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available*1   | Not available | -40 to +105                |
|                   | R5F56514BGBP | PTBG0064KB-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available*1   | Not available | -40 to +105                |
|                   | R5F56514FGBP | PTBG0064KB-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available*1   | Not available | -40 to +105                |
|                   | R5F5651EDGLC | PTLG0177KA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | -40 to +105                |
|                   | R5F5651EHGLC | PTLG0177KA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | -40 to +105                |
|                   | R5F5651CDGLC | PTLG0177KA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | -40 to +105                |
|                   | R5F5651CHGLC | PTLG0177KA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | -40 to +105                |
|                   | R5F5651EDGLK | PTLG0145KA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | -40 to +105                |
|                   | R5F5651EHGLK | PTLG0145KA-A | 2 M                                  | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | -40 to +105                |
|                   | R5F5651CDGLK | PTLG0145KA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Not available     | Available     | Available     | -40 to +105                |
|                   | R5F5651CHGLK | PTLG0145KA-A | 1.5 M                                | 640 K                  | 32 K                                 | 120 MHz                    | Available         | Available     | Available     | -40 to +105                |
|                   | R5F56519AGLK | PTLG0145KA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | -40 to +105                |
|                   | R5F56519BGLK | PTLG0145KA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | -40 to +105                |
|                   | R5F56519EGLK | PTLG0145KA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | -40 to +105                |
|                   | R5F56519FGLK | PTLG0145KA-A | 1 M                                  | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | -40 to +105                |
|                   | R5F56517AGLK | PTLG0145KA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | -40 to +105                |
|                   | R5F56517BGLK | PTLG0145KA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | -40 to +105                |
|                   | R5F56517EGLK | PTLG0145KA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | -40 to +105                |
|                   | R5F56517FGLK | PTLG0145KA-A | 768 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | -40 to +105                |
|                   | R5F56514AGLK | PTLG0145KA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Not available | Not available | -40 to +105                |
|                   | R5F56514BGLK | PTLG0145KA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Not available     | Available     | Not available | -40 to +105                |
|                   | R5F56514EGLK | PTLG0145KA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Not available | Not available | -40 to +105                |
|                   | R5F56514FGLK | PTLG0145KA-A | 512 K                                | 256 K                  | Not included                         | 120 MHz                    | Available         | Available     | Not available | -40 to +105                |

**Table 1.3 List of Products (12/12)**

| Group                     | Part No.     | Package      | Code Flash<br>Memory<br>Capacity<br>(byte(s)) | RAM<br>Capacity<br>(byte(s)) | Data Flash<br>Memory<br>Capacity<br>(byte(s)) | Operating<br>Frequency<br>(Max.) | Encryption<br>Module | SDHI/SDSI          | Dual bank        | Operating<br>tempera-<br>ture (°C) |
|---------------------------|--------------|--------------|-----------------------------------------------|------------------------------|-----------------------------------------------|----------------------------------|----------------------|--------------------|------------------|------------------------------------|
| RX651<br>(G ver-<br>sion) | R5F5651EDGLJ | PTLG0100JA-A | 2 M                                           | 640 K                        | 32 K                                          | 120 MHz                          | Not<br>available     | Available          | Available        | -40 to +105                        |
|                           | R5F5651EHGLJ | PTLG0100JA-A | 2 M                                           | 640 K                        | 32 K                                          | 120 MHz                          | Available            | Available          | Available        | -40 to +105                        |
|                           | R5F5651CDGLJ | PTLG0100JA-A | 1.5 M                                         | 640 K                        | 32 K                                          | 120 MHz                          | Not<br>available     | Available          | Available        | -40 to +105                        |
|                           | R5F5651CHGLJ | PTLG0100JA-A | 1.5 M                                         | 640 K                        | 32 K                                          | 120 MHz                          | Available            | Available          | Available        | -40 to +105                        |
|                           | R5F56519AGLJ | PTLG0100JA-A | 1 M                                           | 256 K                        | Not<br>included                               | 120 MHz                          | Not<br>available     | Not<br>available   | Not<br>available | -40 to +105                        |
|                           | R5F56519BGLJ | PTLG0100JA-A | 1 M                                           | 256 K                        | Not<br>included                               | 120 MHz                          | Not<br>available     | Available          | Not<br>available | -40 to +105                        |
|                           | R5F56519EGLJ | PTLG0100JA-A | 1 M                                           | 256 K                        | Not<br>included                               | 120 MHz                          | Available            | Not<br>available   | Not<br>available | -40 to +105                        |
|                           | R5F56519FGLJ | PTLG0100JA-A | 1 M                                           | 256 K                        | Not<br>included                               | 120 MHz                          | Available            | Available          | Not<br>available | -40 to +105                        |
|                           | R5F56517AGLJ | PTLG0100JA-A | 768 K                                         | 256 K                        | Not<br>included                               | 120 MHz                          | Not<br>available     | Not<br>available   | Not<br>available | -40 to +105                        |
|                           | R5F56517BGLJ | PTLG0100JA-A | 768 K                                         | 256 K                        | Not<br>included                               | 120 MHz                          | Not<br>available     | Available          | Not<br>available | -40 to +105                        |
|                           | R5F56517EGLJ | PTLG0100JA-A | 768 K                                         | 256 K                        | Not<br>included                               | 120 MHz                          | Available            | Not avail-<br>able | Not<br>available | -40 to +105                        |
|                           | R5F56517FGLJ | PTLG0100JA-A | 768 K                                         | 256 K                        | Not<br>included                               | 120 MHz                          | Available            | Available          | Not<br>available | -40 to +105                        |
|                           | R5F56514AGLJ | PTLG0100JA-A | 512 K                                         | 256 K                        | Not<br>included                               | 120 MHz                          | Not<br>available     | Not<br>available   | Not<br>available | -40 to +105                        |
|                           | R5F56514BGLJ | PTLG0100JA-A | 512 K                                         | 256 K                        | Not<br>included                               | 120 MHz                          | Not<br>available     | Available          | Not<br>available | -40 to +105                        |
|                           | R5F56514EGLJ | PTLG0100JA-A | 512 K                                         | 256 K                        | Not<br>included                               | 120 MHz                          | Available            | Not<br>available   | Not<br>available | -40 to +105                        |
|                           | R5F56514FGLJ | PTLG0100JA-A | 512 K                                         | 256 K                        | Not<br>included                               | 120 MHz                          | Available            | Available          | Not<br>available | -40 to +105                        |

Note 1. Only SDHI is available.

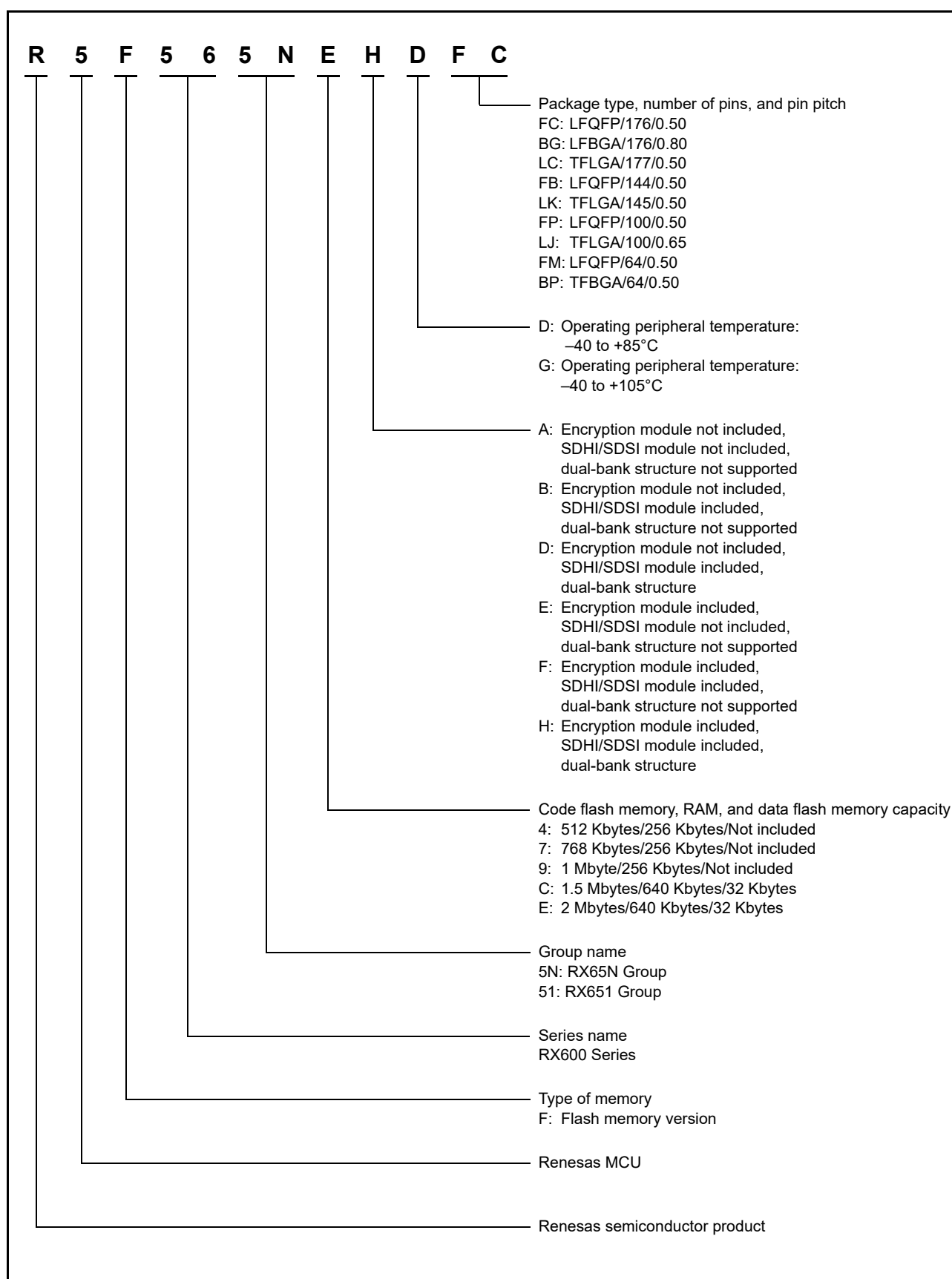
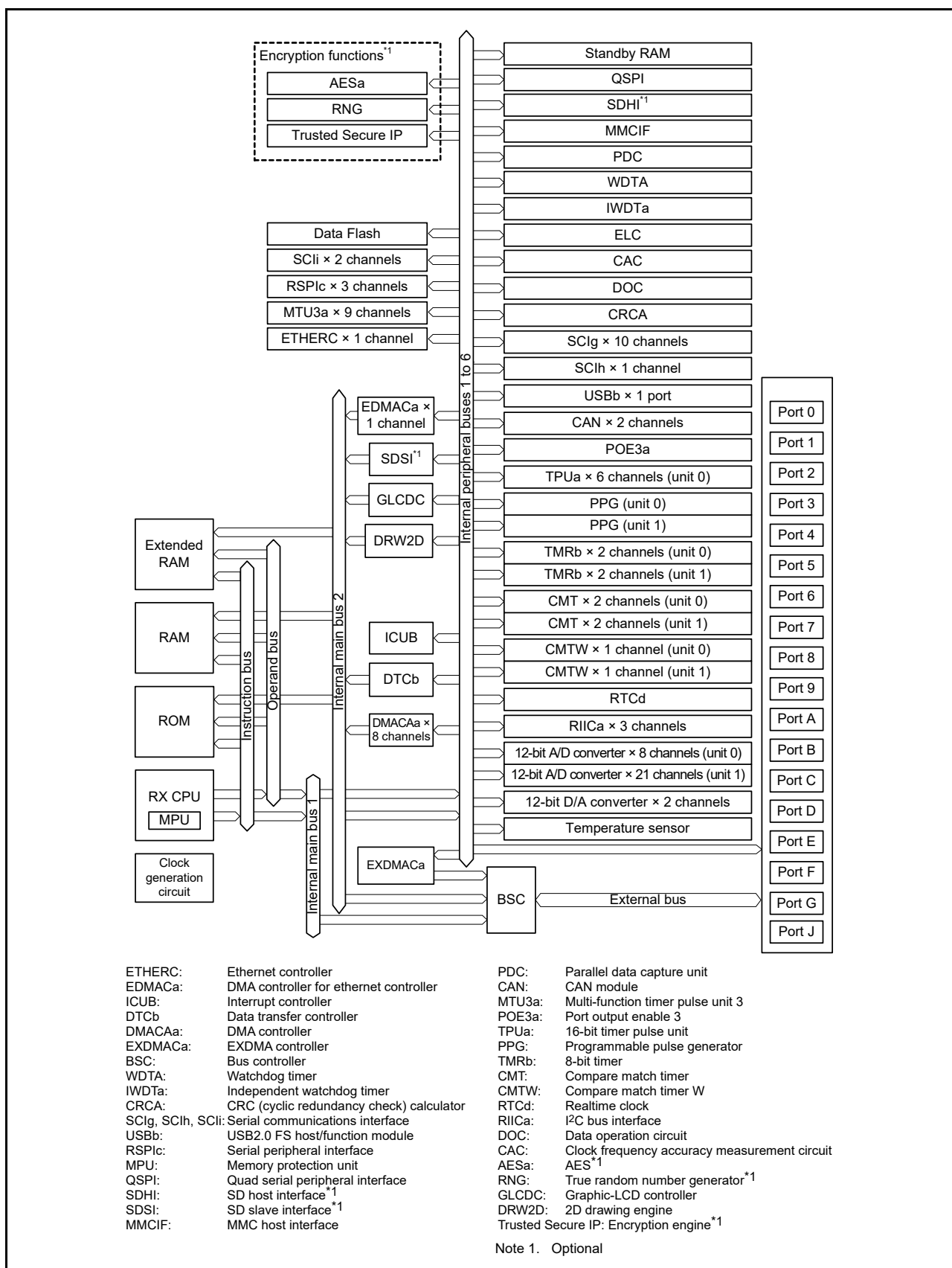


Figure 1.1 How to Read the Product Part Number

### 1.3 Block Diagram

Figure 1.2 shows a block diagram.



**Figure 1.2 Block Diagram**

## 1.4 Pin Functions

Table 1.4 lists the pin functions.

**Table 1.4 Pin Functions (1/8)**

| Classifications                      | Pin Name                                                                             | I/O    | Description                                                                                                                                                                       |
|--------------------------------------|--------------------------------------------------------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Digital power supply                 | VCC                                                                                  | Input  | Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
|                                      | VCL                                                                                  | Input  | Connect this pin to VSS via a 0.22-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.                                                              |
|                                      | VSS                                                                                  | Input  | Ground pin. Connect it to the system power supply (0 V).                                                                                                                          |
|                                      | VBATT                                                                                | Input  | Backup power pin                                                                                                                                                                  |
| Clock                                | XTAL                                                                                 | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.                                                                                        |
|                                      | EXTAL                                                                                | Input  |                                                                                                                                                                                   |
|                                      | BCLK                                                                                 | Output | Outputs the external bus clock for external devices.                                                                                                                              |
|                                      | SDCLK                                                                                | Output | Outputs the SDRAM-dedicated clock.                                                                                                                                                |
|                                      | XCOUT                                                                                | Output | Input/output pins for the sub clock oscillator. Connect a crystal resonator between XCOUT and XCIN.                                                                               |
|                                      | XCIN                                                                                 | Input  |                                                                                                                                                                                   |
| Clock frequency accuracy measurement | CACREF                                                                               | Input  | Reference clock input pin for the clock frequency accuracy measurement circuit                                                                                                    |
| Operating mode control               | MD                                                                                   | Input  | Pin for setting the operating mode. The signal level on this pin must not be changed during operation.                                                                            |
|                                      | UB                                                                                   | Input  | USB boot mode enable pin                                                                                                                                                          |
|                                      | UPSEL                                                                                | Input  | Selects the power supply method in USB boot mode. The low level selects self-powered mode and the high level selects bus-powered mode.                                            |
| System control                       | RES#                                                                                 | Input  | Reset signal input pin. This LSI enters the reset state when this signal goes low.                                                                                                |
|                                      | EMLE                                                                                 | Input  | Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.                      |
|                                      | BSCANP                                                                               | Input  | Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low.                                                               |
| On-chip emulator                     | FINED                                                                                | I/O    | Fine interface pin                                                                                                                                                                |
|                                      | TRST#                                                                                | Input  | On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.                                                      |
|                                      | TMS                                                                                  | Input  |                                                                                                                                                                                   |
|                                      | TDI                                                                                  | Input  |                                                                                                                                                                                   |
|                                      | TCK                                                                                  | Input  |                                                                                                                                                                                   |
|                                      | TDO                                                                                  | Output |                                                                                                                                                                                   |
|                                      | TRCLK                                                                                | Output | This pin outputs the clock for synchronization with the trace data.                                                                                                               |
|                                      | TRSYNC<br>TRSYNC1                                                                    | Output | These pins indicate that output from the TRDATA0 to TRDATA7 pins is valid.                                                                                                        |
|                                      | TRDATA0<br>TRDATA1<br>TRDATA2<br>TRDATA3<br>TRDATA4<br>TRDATA5<br>TRDATA6<br>TRDATA7 | Output | These pins output the trace information.                                                                                                                                          |
| Address bus                          | A0 to A23                                                                            | Output | Output pins for the address                                                                                                                                                       |
| Data bus                             | D0 to D31                                                                            | I/O    | Input and output pins for the bidirectional data bus                                                                                                                              |

**Table 1.4 Pin Functions (2/8)**

| Classifications                   | Pin Name                            | I/O    | Description                                                                                                                                                                                      |
|-----------------------------------|-------------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Multiplexed bus                   | A0/D0 to A15/D15                    | I/O    | Address/data multiplexed bus                                                                                                                                                                     |
| Bus control                       | RD#                                 | Output | Strobe signal which indicates that reading from the external bus interface space is in progress                                                                                                  |
|                                   | WR#                                 | Output | Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode                                                                            |
|                                   | WR0# to WR3#                        | Output | Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode   |
|                                   | BC0# to BC3#                        | Output | Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode |
|                                   | ALE                                 | Output | Address latch signal when address/data multiplexed bus is selected                                                                                                                               |
|                                   | WAIT#                               | Input  | Input pin for wait request signals in access to the external space                                                                                                                               |
|                                   | CS0# to CS7#                        | Output | Select signals for CS areas                                                                                                                                                                      |
|                                   | CKE                                 | Output | SDRAM clock enable signal                                                                                                                                                                        |
|                                   | SDCS#                               | Output | SDRAM chip select signal                                                                                                                                                                         |
|                                   | RAS#                                | Output | SDRAM row address strobe signal                                                                                                                                                                  |
|                                   | CAS#                                | Output | SDRAM column address strobe signal                                                                                                                                                               |
|                                   | WE#                                 | Output | SDRAM write enable pin                                                                                                                                                                           |
|                                   | DQM0 to DQM3                        | Output | SDRAM I/O data mask enable signals                                                                                                                                                               |
| EXDMA controller                  | EDREQ0, EDREQ1                      | Input  | External DMA transfer request pins                                                                                                                                                               |
|                                   | EDACK0, EDACK1                      | Output | Single address transfer acknowledge signals                                                                                                                                                      |
| Interrupt                         | NMI                                 | Input  | Non-maskable interrupt request pin                                                                                                                                                               |
|                                   | IRQ0 to IRQ15, IRQ0-DS to IRQ15-DS  | Input  | Maskable interrupt request pins                                                                                                                                                                  |
| Multi-function timer pulse unit 3 | MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D  | I/O    | The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins                                                                                                                     |
|                                   | MTIOC1A, MTIOC1B                    | I/O    | The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins                                                                                                                    |
|                                   | MTIOC2A, MTIOC2B                    | I/O    | The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins                                                                                                                    |
|                                   | MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D  | I/O    | The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins                                                                                                                     |
|                                   | MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D  | I/O    | The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins                                                                                                                     |
|                                   | MTIC5U, MTIC5V, MTIC5W              | Input  | The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins                                                                                                                |
|                                   | MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D  | I/O    | The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins                                                                                                                     |
|                                   | MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D  | I/O    | The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins                                                                                                                     |
|                                   | MTIOC8A, MTIOC8B, MTIOC8C, MTIOC8D  | I/O    | The TGRA8 to TGRD8 input capture input/output compare output/PWM output pins                                                                                                                     |
|                                   | MTCLKA, MTCLKB, MTCLKC, MTCLKD      | Input  | Input pins for external clock signals or for phase counting mode clock signals                                                                                                                   |
| Port output enable 3              | POE0#, POE4#, POE8#, POE10#, POE11# | Input  | Input pins for request signals to place the MTU in the high impedance state                                                                                                                      |

**Table 1.4 Pin Functions (3/8)**

| Classifications                        | Pin Name                                   | I/O    | Description                                                                    |
|----------------------------------------|--------------------------------------------|--------|--------------------------------------------------------------------------------|
| 16-bit timer pulse unit                | TIOCA0, TIOCB0, TIOCC0, TIOCD0             | I/O    | The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins   |
|                                        | TIOCA1, TIOCB1                             | I/O    | The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins  |
|                                        | TIOCA2, TIOCB2                             | I/O    | The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins  |
|                                        | TIOCA3, TIOCB3, TIOCC3, TIOCD3             | I/O    | The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins   |
|                                        | TIOCA4, TIOCB4                             | I/O    | The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins  |
|                                        | TIOCA5, TIOCB5                             | I/O    | The TGRA5 and TGRB5 input capture input/output compare output/PWM output pins  |
|                                        | TCLKA, TCLKB, TCLKC, TCLKD                 | Input  | Input pins for external clock signals or for phase counting mode clock signals |
| Programmable pulse generator           | PO0 to PO31                                | Output | Output pins for the pulse signals                                              |
| 8-bit timer                            | TMO0 to TMO3                               | Output | Compare match output pins                                                      |
|                                        | TMCI0 to TMCI3                             | Input  | Input pins for external clocks to be input to the counter                      |
|                                        | TMRI0 to TMRI3                             | Input  | Input pins for the counter reset                                               |
| Compare match timer W                  | TIC0 to TIC3                               | Input  | Input pins for CMTW                                                            |
|                                        | TOC0 to TOC3                               | Output | Output pins for CMTW                                                           |
| Serial communications interface (SCIg) | • Asynchronous mode/clock synchronous mode |        |                                                                                |
|                                        | SCK0 to SCK9                               | I/O    | Input/output pins for the clock                                                |
|                                        | RXD0 to RXD9                               | Input  | Input pins for received data                                                   |
|                                        | TXD0 to TXD9                               | Output | Output pins for transmitted data                                               |
|                                        | CTS0# to CTS9#                             | Input  | Input pins for controlling the start of transmission and reception             |
|                                        | RTS0# to RTS9#                             | Output | Output pins for controlling the start of transmission and reception            |
|                                        | • Simple I <sup>2</sup> C mode             |        |                                                                                |
|                                        | SSCL0 to SSCL9                             | I/O    | Input/output pins for the I <sup>2</sup> C clock                               |
|                                        | SSDA0 to SSDA9                             | I/O    | Input/output pins for the I <sup>2</sup> C data                                |
|                                        | • Simple SPI mode                          |        |                                                                                |
|                                        | SCK0 to SCK9                               | I/O    | Input/output pins for the clock                                                |
|                                        | SMISO0 to SMISO9                           | I/O    | Input/output pins for slave transmission of data                               |
|                                        | SMOSI0 to SMOSI9                           | I/O    | Input/output pins for master transmission of data                              |
|                                        | SS0# to SS9#                               | Input  | Chip-select input pins                                                         |

**Table 1.4 Pin Functions (4/8)**

| Classifications                        | Pin Name                                   | I/O    | Description                                                                          |
|----------------------------------------|--------------------------------------------|--------|--------------------------------------------------------------------------------------|
| Serial communications interface (SCIh) | • Asynchronous mode/clock synchronous mode |        |                                                                                      |
|                                        | SCK12                                      | I/O    | Input/output pin for the clock                                                       |
|                                        | RXD12                                      | Input  | Input pin for received data                                                          |
|                                        | TXD12                                      | Output | Output pin for transmitted data                                                      |
|                                        | CTS12#                                     | Input  | Input pin for controlling the start of transmission and reception                    |
|                                        | RTS12#                                     | Output | Output pin for controlling the start of transmission and reception                   |
|                                        | • Simple I <sup>2</sup> C mode             |        |                                                                                      |
|                                        | SSCL12                                     | I/O    | Input/output pin for the I <sup>2</sup> C clock                                      |
|                                        | SSDA12                                     | I/O    | Input/output pin for the I <sup>2</sup> C data                                       |
|                                        | • Simple SPI mode                          |        |                                                                                      |
|                                        | SCK12                                      | I/O    | Input/output pin for the clock                                                       |
|                                        | SMISO12                                    | I/O    | Input/output pin for slave transmission of data                                      |
|                                        | SMOSI12                                    | I/O    | Input/output pin for master transmission of data                                     |
|                                        | SS12#                                      | Input  | Chip-select input pin                                                                |
|                                        | • Extended serial mode                     |        |                                                                                      |
|                                        | RDX12                                      | Input  | Input pin for received data                                                          |
|                                        | TXDX12                                     | Output | Output pin for transmitted data                                                      |
|                                        | SIOX12                                     | I/O    | Input/output pin for received or transmitted data                                    |
| Serial communications interface (SCIi) | • Asynchronous mode/clock synchronous mode |        |                                                                                      |
|                                        | SCK10 and SCK11                            | I/O    | Input/output pin for the clock                                                       |
|                                        | RXD10 and RXD11                            | Input  | Input pin for received data                                                          |
|                                        | TXD10 and TXD11                            | Output | Output pin for transmitted data                                                      |
|                                        | CTS10# and CTS11#                          | Input  | Input pin for controlling the start of transmission and reception                    |
|                                        | RTS10# and RTS11#                          | Output | Output pin for controlling the start of transmission and reception                   |
|                                        | • Simple I <sup>2</sup> C mode             |        |                                                                                      |
|                                        | SSCL10 and SSCL11                          | I/O    | Input/output pin for the I <sup>2</sup> C clock                                      |
|                                        | SSDA10 and SSDA11                          | I/O    | Input/output pin for the I <sup>2</sup> C data                                       |
|                                        | • Simple SPI mode                          |        |                                                                                      |
|                                        | SCK10 and SCK11                            | I/O    | Input/output pin for the clock                                                       |
|                                        | SMISO10 and SMISO11                        | I/O    | Input/output pin for slave transmission of data                                      |
|                                        | SMOSI10 and SMOSI11                        | I/O    | Input/output pin for master transmission of data                                     |
|                                        | SS10# and SS11#                            | Input  | Chip-select input pin                                                                |
| I <sup>2</sup> C bus interface         | SCL0[FM+], SCL1, SCL2, SCL2-DS             | I/O    | Input/output pins for clocks. Bus can be directly driven by the N-channel open drain |
|                                        | SDA0[FM+], SDA1, SDA2, SDA2-DS             | I/O    | Input/output pins for data. Bus can be directly driven by the N-channel open drain   |

**Table 1.4 Pin Functions (5/8)**

| Classifications              | Pin Name                      | I/O    | Description                                                                                                                       |
|------------------------------|-------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------|
| Ethernet controller          | REF50CK0                      | Input  | 50-MHz reference clocks. These pins input reference signals for transmission/reception timings in RMII mode.                      |
|                              | RMII0_CRS_DV                  | Input  | Indicate that there are carrier detection signals and valid receive data on RMII0_RXD1 and RMII0_RXD0 in RMII mode.               |
|                              | RMII0_TXD0, RMII0_TXD1        | Output | 2-bit transmit data in RMII mode                                                                                                  |
|                              | RMII0_RXD0, RMII0_RXD1        | Input  | 2-bit receive data in RMII mode                                                                                                   |
|                              | RMII0_TXD_EN                  | Output | Output pins for data transmit enable signals in RMII mode                                                                         |
|                              | RMII0_RX_ER                   | Input  | Indicate an error has occurred during reception of data in RMII mode.                                                             |
|                              | ET0_CRS                       | Input  | Carrier detection/data reception enable pins                                                                                      |
|                              | ET0_RX_DV                     | Input  | Indicate that there are valid receive data on ET0_ERXD3 to ET0_ERXD0.                                                             |
|                              | ET0_EXOUT                     | Output | General-purpose external output pins                                                                                              |
|                              | ET0_LINKSTA                   | Input  | Input link status from the PHY-LSI.                                                                                               |
|                              | ET0_ETXD0 to ET0_ETXD3        | Output | 4 bits of MII transmit data                                                                                                       |
|                              | ET0_ERXD0 to ET0_ERXD3        | Input  | 4 bits of MII receive data                                                                                                        |
|                              | ET0_TX_EN                     | Output | Transmit enable pins. Function as signals indicating that transmit data is ready on ET0_ETXD3 to ET0_ETXD0.                       |
|                              | ET0_TX_ER                     | Output | Transmit error pins. Function as signals notifying the PHY-LSI of an error during transmission.                                   |
|                              | ET0_RX_ER                     | Input  | Receive error pins. Function as signals to recognize an error during reception.                                                   |
|                              | ET0_TX_CLK                    | Input  | Transmit clock pins. These pins input reference signals for output timings from ET0_TX_EN, ET0_ETXD3 to ET0_ETXD0, and ET0_TX_ER. |
|                              | ET0_RX_CLK                    | Input  | Receive clock pins. These pins input reference signals for input timings to ET0_RX_DV, ET0_ERXD3 to ET0_ERXD0, and ET0_RX_ER.     |
|                              | ET0_COL                       | Input  | Input collision detection signals.                                                                                                |
|                              | ET0_WOL                       | Output | Receive Magic packets.                                                                                                            |
|                              | ET0_MDC                       | Output | Output reference clock signals for information transfer via ET0_MDIO.                                                             |
|                              | ET0_MDIO                      | I/O    | Input or output bidirectional signals for exchange of management information between this MCU and the PHY-LSI.                    |
| USB 2.0 host/function module | VCC_USB                       | Input  | Power supply pin                                                                                                                  |
|                              | VSS_USB                       | Input  | Ground pin                                                                                                                        |
|                              | USB0_DP                       | I/O    | Input or output USB transceiver D+ data.                                                                                          |
|                              | USB0_DM                       | I/O    | Input or output USB transceiver D- data.                                                                                          |
|                              | USB0_EXICEN                   | Output | Connect to the OTG power IC.                                                                                                      |
|                              | USB0_ID                       | Input  | Connect to the OTG power IC.                                                                                                      |
|                              | USB0_VBUSEN                   | Output | USB VBUS power enable pins                                                                                                        |
|                              | USB0_OVRCURA/<br>USB0_OVRCURB | Input  | USB overcurrent pins                                                                                                              |
| CAN module                   | USB0_VBUS                     | Input  | USB cable connection/disconnection detection input pin                                                                            |
|                              | CRX0, CRX1, CRX1-DS           | Input  | Input pins                                                                                                                        |
|                              | CTX0, CTX1                    | Output | Output pins                                                                                                                       |

**Table 1.4 Pin Functions (6/8)**

| Classifications                  | Pin Name                                                                                                                                                                        | I/O    | Description                                   |
|----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------------------|
| Serial peripheral interface      | RSPCKA-A/RSPCKA-B/<br>RSPCKB-A/RSPCKB-B/<br>RSPCKC-A/RSPCKC-B                                                                                                                   | I/O    | Clock input/output pins                       |
|                                  | MOSIA-A/MOSIA-B/<br>MOSIB-A/MOSIB-B/<br>MOSIC-A/MOSIC-B                                                                                                                         | I/O    | Input or output data output from the master   |
|                                  | MISOA-A/MISOA-B/<br>MISOB-A/MISOB-B/<br>MISOC-A/MISOC-B                                                                                                                         | I/O    | Input or output data output from the slave    |
|                                  | SSLA0-A/SSLA0-B/<br>SSLB0-A/SSLB0-B/<br>SSLC0-A/SSLC0-B                                                                                                                         | I/O    | Input or output pins for slave selection      |
|                                  | SSLA1-A/SSLA1-B/<br>SSLB1-A/SSLB1-B/<br>SSLC1-A/SSLC1-B,<br>SSLA2-A/SSLA2-B/<br>SSLB2-A/SSLB2-B/<br>SSLC2-A/SSLC2-B,<br>SSLA3-A/SSLA3-B/<br>SSLB3-A/SSLB3-B/<br>SSLC3-A/SSLC3-B | Output | Output pins for slave selection               |
| Quad serial peripheral interface | QSPCLK-A/QSPCLK-B                                                                                                                                                               | Output | QSPI clock output pins                        |
|                                  | QSSL-A/QSSL-B                                                                                                                                                                   | Output | QSPI slave output pins                        |
|                                  | QMO-A/QMO-B,<br>QIO0-A/QIO0-B                                                                                                                                                   | I/O    | Master transmit data/data 0                   |
|                                  | QMI-A/QMI-B,<br>QIO1-A/QIO1-B                                                                                                                                                   | I/O    | Master input data/data 1                      |
|                                  | QIO2-A/QIO2-B,<br>QIO3-A/QIO3-B                                                                                                                                                 | I/O    | Data 2, data 3                                |
| MMC host interface               | MMC_CLK-A/<br>MMC_CLK-B                                                                                                                                                         | Output | MMC clock pins                                |
|                                  | MMC_CMD-A/<br>MMC_CMD-B                                                                                                                                                         | I/O    | Command/response pins                         |
|                                  | MMC_D7-A/MMC_D7-B to<br>MMC_D0-A/MMC_D0-B                                                                                                                                       | I/O    | Transmit data/receive data                    |
|                                  | MMC_CD-A/MMC_CD-B                                                                                                                                                               | Input  | Card detection pins                           |
|                                  | MMC_RES#-A/MMC_RES#-B                                                                                                                                                           | Output | MMC reset output pins                         |
| SD host interface                | SDHI_CLK-A/SDHI_CLK-B/<br>SDHI_CLK-C                                                                                                                                            | Output | SD clock output pins                          |
|                                  | SDHI_CMD-A/SDHI_CMD-B/<br>SDHI_CMD-C                                                                                                                                            | I/O    | SD command output, response input signal pins |
|                                  | SDHI_D3-A/SDHI_D3-B/<br>SDHI_D3-C to SDHI_D0-A/<br>SDHI_D0-B/SDHI_D0-C                                                                                                          | I/O    | SD data bus pins                              |
|                                  | SDHI_CD                                                                                                                                                                         | Input  | SD card detection pin                         |
|                                  | SDHI_WP                                                                                                                                                                         | Input  | SD write-protect signal                       |
| SD slave interface               | SDSI_CLK-A/SDSI_CLK-B                                                                                                                                                           | Input  | SD clock input pins                           |
|                                  | SDSI_CMD-A/SDSI_CMD-B                                                                                                                                                           | I/O    | SD command input, response output signal pins |
|                                  | SDSI_D3-A/SDSI_D3-B,<br>SDSI_D2-A/SDSI_D2-B,<br>SDSI_D1-A/SDSI_D1-B,<br>SDSI_D0-A/SDSI_D0-B                                                                                     | I/O    | SD data bus pins                              |

**Table 1.4 Pin Functions (7/8)**

| Classifications            | Pin Name                                                        | I/O    | Description                                                                                                                                                                                                                                                                                                                                                                     |
|----------------------------|-----------------------------------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Parallel data capture unit | PIXCLK                                                          | Input  | Image transfer clock pin                                                                                                                                                                                                                                                                                                                                                        |
|                            | VSYNC                                                           | Input  | Vertical synchronization signal pin                                                                                                                                                                                                                                                                                                                                             |
|                            | HSYNC                                                           | Input  | Horizontal synchronization signal pin                                                                                                                                                                                                                                                                                                                                           |
|                            | PIXD0 to PIXD7                                                  | Input  | 8-bit image data pins                                                                                                                                                                                                                                                                                                                                                           |
|                            | PCKO                                                            | Output | Output pin for dot clock                                                                                                                                                                                                                                                                                                                                                        |
| Graphic-LCD controller     | LCD_CLK-A, LCD_CLK-B                                            | Output | Panel clock output pins                                                                                                                                                                                                                                                                                                                                                         |
|                            | LCD_TCON3-A/<br>LCD_TCON3-B to<br>LCD_TCON0-A/<br>LCD_TCON0-B   | Output | Control signal output pins                                                                                                                                                                                                                                                                                                                                                      |
|                            | LCD_DATA23-A/<br>LCD_DATA23-B to<br>LCD_DATA0-A/<br>LCD_DATA0-B | Output | LCD signal output pins                                                                                                                                                                                                                                                                                                                                                          |
|                            | LCD_EXTCLK-A,<br>LCD_EXTCLK-B                                   | Input  | Panel clock source input pins                                                                                                                                                                                                                                                                                                                                                   |
| Realtime clock             | RTCOUT                                                          | Output | Output pin for 1-Hz/64-Hz clock                                                                                                                                                                                                                                                                                                                                                 |
|                            | RTCIC0 to RTCIC2                                                | Input  | Time capture event input pins                                                                                                                                                                                                                                                                                                                                                   |
| 12-bit A/D converter       | AN000 to AN007,<br>AN100 to AN120                               | Input  | Input pins for the analog signals to be processed by the A/D converter                                                                                                                                                                                                                                                                                                          |
|                            | ADTRG0#, ADTRG1#                                                | Input  | Input pins for the external trigger signals that start the A/D conversion                                                                                                                                                                                                                                                                                                       |
|                            | ANEX0                                                           | Output | Extended analog output pin                                                                                                                                                                                                                                                                                                                                                      |
|                            | ANEX1                                                           | Input  | Extended analog input pin                                                                                                                                                                                                                                                                                                                                                       |
| 12-bit D/A converter       | DA0, DA1                                                        | Output | Output pins for the analog signals to be processed by the D/A converter                                                                                                                                                                                                                                                                                                         |
| Analog power supply        | AVCC0                                                           | Input  | Analog voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VCC power supply. Connect the pin to AVSS0 via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.                                                                                                                                   |
|                            | AVSS0                                                           | Input  | Analog ground pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VSS ground power supply. Connect the pin to AVCC0 via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.                                                                                                                                    |
|                            | VREFH0                                                          | Input  | Analog reference voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to VCC if the 12-bit A/D converter is not to be used.                                                                                                                                                                                                                               |
|                            | VREFL0                                                          | Input  | Analog reference ground pin for the 12-bit A/D converter (unit 0). Connect this pin to VSS if the 12-bit A/D converter is not to be used.                                                                                                                                                                                                                                       |
|                            | AVCC1                                                           | Input  | Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog voltage to the temperature sensor. Connect this pin to a branch from the VCC power supply. Connect the pin to AVSS1 via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.               |
|                            | AVSS1                                                           | Input  | Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog ground voltage to the temperature sensor. Connect this pin to a branch from the VSS ground power supply. Connect the pin to AVCC1 via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |

**Table 1.4 Pin Functions (8/8)**

| Classifications | Pin Name             | I/O | Description                              |
|-----------------|----------------------|-----|------------------------------------------|
| I/O ports       | P00 to P03, P05, P07 | I/O | 6-bit input/output pins                  |
|                 | P10 to P17           | I/O | 8-bit input/output pins                  |
|                 | P20 to P27           | I/O | 8-bit input/output pins                  |
|                 | P30 to P37           | I/O | 8-bit input/output pins (P35: input pin) |
|                 | P40 to P47           | I/O | 8-bit input/output pins                  |
|                 | P50 to P57           | I/O | 8-bit input/output pins                  |
|                 | P60 to P67           | I/O | 8-bit input/output pins                  |
|                 | P70 to P77           | I/O | 8-bit input/output pins                  |
|                 | P80 to P87           | I/O | 8-bit input/output pins                  |
|                 | P90 to P97           | I/O | 8-bit input/output pins                  |
|                 | PA0 to PA7           | I/O | 8-bit input/output pins                  |
|                 | PB0 to PB7           | I/O | 8-bit input/output pins                  |
|                 | PC0 to PC7           | I/O | 8-bit input/output pins                  |
|                 | PD0 to PD7           | I/O | 8-bit input/output pins                  |
|                 | PE0 to PE7           | I/O | 8-bit input/output pins                  |
|                 | PF0 to PF5           | I/O | 6-bit input/output pins                  |
|                 | PG0 to PG7           | I/O | 8-bit input/output pins                  |
|                 | PJ0 to PJ3, PJ5      | I/O | 5-bit input/output pins                  |

Note: Note the following regarding pin names. For details, see section 1.5, Pin Assignments.

- When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group.  
All RSPI, QSPI, SDHI, MMC, GLCDC AC timings are measured in combination with the pins in the same group.
- When the pin functions have “-DS” appended to their names, they can also be used as triggers for release from deep software standby.
- IIC pin functions that have [FM+] appended to their names support fast-mode plus.

## 1.5 Pin Assignments

## 1.5.1 177-Pin TFLGA

|    | A      | B   | C      | D   | E                                                                                       | F      | G         | H    | J     | K   | L   | M   | N   | P        | R        |          |   |
|----|--------|-----|--------|-----|-----------------------------------------------------------------------------------------|--------|-----------|------|-------|-----|-----|-----|-----|----------|----------|----------|---|
| 15 | PE2    | PE3 | P70    | P65 | P67                                                                                     | VSS    | VCC       | PG7  | PA6   | PB0 | P72 | PB4 | VSS | VCC      | PC1      | 15       |   |
| 14 | PE1    | PE0 | VSS    | PE7 | PG3                                                                                     | PA0    | PA1       | PA2  | PA7   | VCC | PB1 | PB5 | P73 | P75      | P74      | 14       |   |
| 13 | P63    | P64 | PE4    | VCC | PG2                                                                                     | PG4    | PG6       | PA3  | VSS   | P71 | PB3 | PB7 | PC0 | PC2      | P76      | 13       |   |
| 12 | P60    | VSS | P62    | PE5 | PE6                                                                                     | P66    | PG5       | PA4  | PA5   | PB2 | PB6 | P77 | PC3 | PC4      | P80      | 12       |   |
| 11 | PD6    | PG1 | VCC    | P61 | RX65N Group, RX651 Group<br>PTLG0177KA-A<br>(177-Pin TFLGA)<br>(Upper Perspective View) |        |           |      |       |     |     | P81 | P82 | PC6      | VCC      | 11       |   |
| 10 | P97    | PD4 | PG0    | PD7 |                                                                                         |        |           |      |       |     |     | PC5 | PC7 | P83      | VSS      | 10       |   |
| 9  | VCC    | P96 | PD3    | PD5 |                                                                                         |        |           |      |       |     |     | P50 | P51 | P52      | P53      | 9        |   |
| 8  | P94    | PD1 | PD2    | VSS |                                                                                         |        |           |      |       |     |     | P55 | P54 | P10      | P11      | 8        |   |
| 7  | VSS    | P92 | PD0    | P95 |                                                                                         |        |           |      |       |     |     | P85 | P84 | P57      | P56      | 7        |   |
| 6  | VCC    | P91 | P90    | P93 |                                                                                         |        |           |      |       |     |     | PJ1 | PJ0 | VSS_ USB | USB0_ DP | 6        |   |
| 5  | P46    | P47 | P45    | P44 | NC                                                                                      |        |           |      |       |     |     |     | PJ2 | P12      | VCC_ USB | USB0_ DM | 5 |
| 4  | P42    | P41 | P43    | P00 | VSS                                                                                     | BSCANP | PF4       | P35  | PF3   | PF1 | P25 | P86 | P15 | P14      | P13      | 4        |   |
| 3  | VREFL0 | P40 | VREFH0 | P03 | PF5                                                                                     | PJ3    | MD/ FINED | RES# | P34   | PF2 | PF0 | P24 | P22 | P87      | P16      | 3        |   |
| 2  | AVCC0  | P07 | AVCC1  | P02 | EMLE                                                                                    | VCL    | XCOUT     | VSS  | VCC   | P32 | P30 | P26 | P23 | P17      | P20      | 2        |   |
| 1  | AVSS0  | P05 | AVSS1  | P01 | PJ5                                                                                     | VBATT  | XCIN      | XTAL | EXTAL | P33 | P31 | P27 | VCC | VSS      | P21      | 1        |   |
|    | A      | B   | C      | D   | E                                                                                       | F      | G         | H    | J     | K   | L   | M   | N   | P        | R        |          |   |

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.3 Pin Assignment (177-Pin TFLGA)

## 1.5.2 176-Pin LFBGA

|    | A      | B   | C      | D   | E                                                                                                                   | F      | G            | H    | J     | K   | L   | M   | N   | P       | R       |    |
|----|--------|-----|--------|-----|---------------------------------------------------------------------------------------------------------------------|--------|--------------|------|-------|-----|-----|-----|-----|---------|---------|----|
| 15 | PE2    | PE3 | P70    | P65 | P67                                                                                                                 | VSS    | VCC          | PG7  | PA6   | PB0 | P72 | PB4 | VSS | VCC     | PC1     | 15 |
| 14 | PE1    | PE0 | VSS    | PE7 | PG3                                                                                                                 | PA0    | PA1          | PA2  | PA7   | VCC | PB1 | PB5 | P73 | P75     | P74     | 14 |
| 13 | P63    | P64 | PE4    | VCC | PG2                                                                                                                 | PG4    | PG6          | PA3  | VSS   | P71 | PB3 | PB7 | PC0 | PC2     | P76     | 13 |
| 12 | P60    | VSS | P62    | PE5 | PE6                                                                                                                 | P66    | PG5          | PA4  | PA5   | PB2 | PB6 | P77 | PC3 | PC4     | P80     | 12 |
| 11 | PD6    | PG1 | VCC    | P61 | <b>RX65N Group, RX651 Group</b><br><b>PLBG0176GA-A</b><br><b>(176-Pin LFBGA)</b><br><b>(Upper Perspective View)</b> |        |              |      |       |     |     | P81 | P82 | PC6     | VCC     | 11 |
| 10 | P97    | PD4 | PG0    | PD7 |                                                                                                                     |        |              |      |       |     |     | PC5 | PC7 | P83     | VSS     | 10 |
| 9  | VCC    | P96 | PD3    | PD5 |                                                                                                                     |        |              |      |       |     |     | P50 | P51 | P52     | P53     | 9  |
| 8  | P94    | PD1 | PD2    | VSS |                                                                                                                     |        |              |      |       |     |     | P55 | P54 | P10     | P11     | 8  |
| 7  | VSS    | P92 | PD0    | P95 |                                                                                                                     |        |              |      |       |     |     | P85 | P84 | P57     | P56     | 7  |
| 6  | VCC    | P91 | P90    | P93 |                                                                                                                     |        |              |      |       |     |     | PJ1 | PJ0 | VSS_USB | USB0_DP | 6  |
| 5  | P46    | P47 | P45    | P44 |                                                                                                                     |        |              |      |       |     |     | PJ2 | P12 | VCC_USB | USB0_DM | 5  |
| 4  | P42    | P41 | P43    | P00 | VSS                                                                                                                 | BSCANP | PF4          | P35  | PF3   | PF1 | P25 | P86 | P15 | P14     | P13     | 4  |
| 3  | VREFL0 | P40 | VREFH0 | P03 | PF5                                                                                                                 | PJ3    | MD/<br>FINED | RES# | P34   | PF2 | PF0 | P24 | P22 | P87     | P16     | 3  |
| 2  | AVCC0  | P07 | AVCC1  | P02 | EMLE                                                                                                                | VCL    | XCOUT        | VSS  | VCC   | P32 | P30 | P26 | P23 | P17     | P20     | 2  |
| 1  | AVSS0  | P05 | AVSS1  | P01 | PJ5                                                                                                                 | VBATT  | XCIN         | XTAL | EXTAL | P33 | P31 | P27 | VCC | VSS     | P21     | 1  |
|    | A      | B   | C      | D   | E                                                                                                                   | F      | G            | H    | J     | K   | L   | M   | N   | P       | R       |    |

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.4 Pin Assignment (176-Pin LFBGA)

## 1.5.3 176-Pin LFQFP

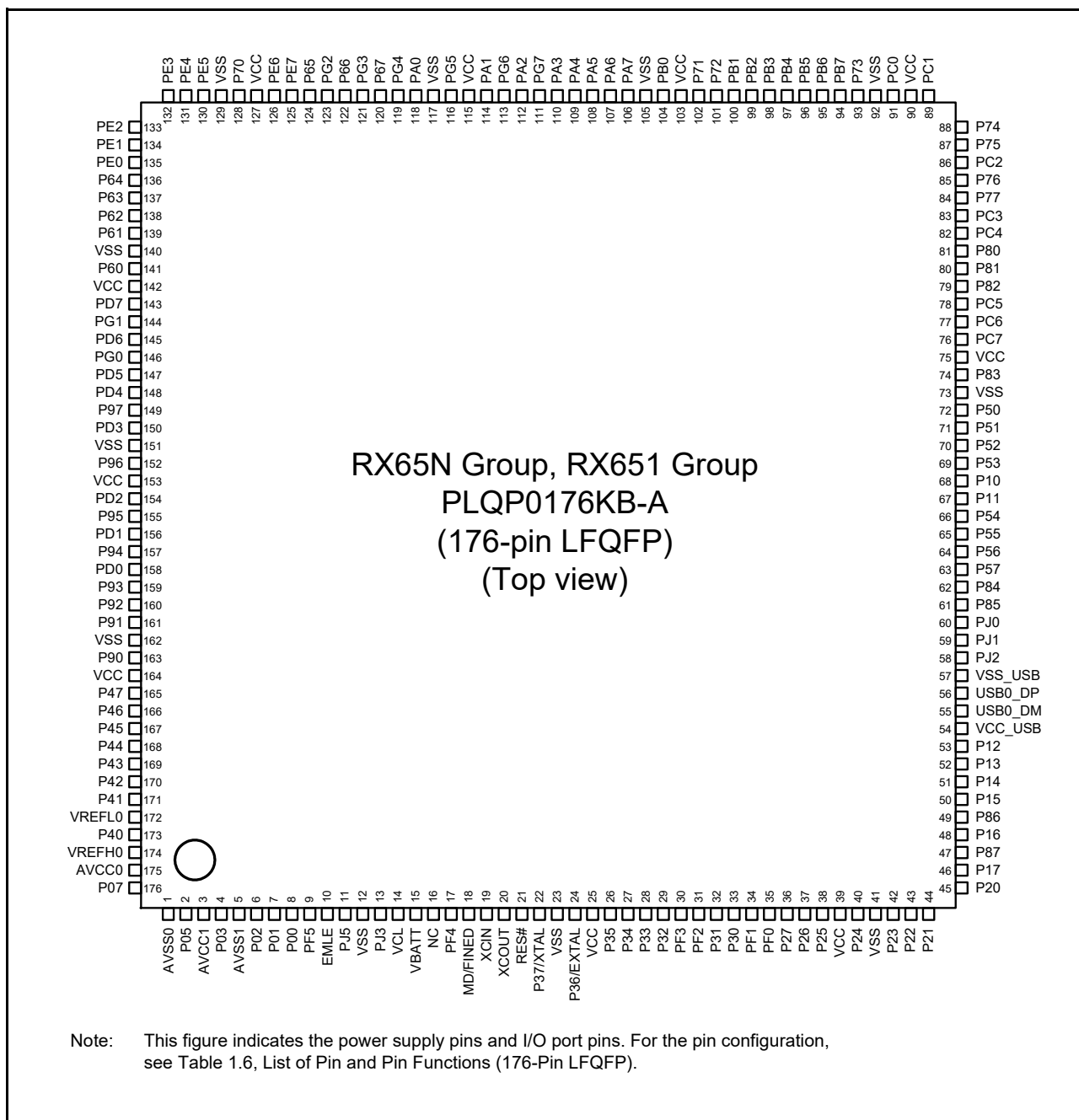


Figure 1.5 Pin Assignment (176-Pin LFQFP)

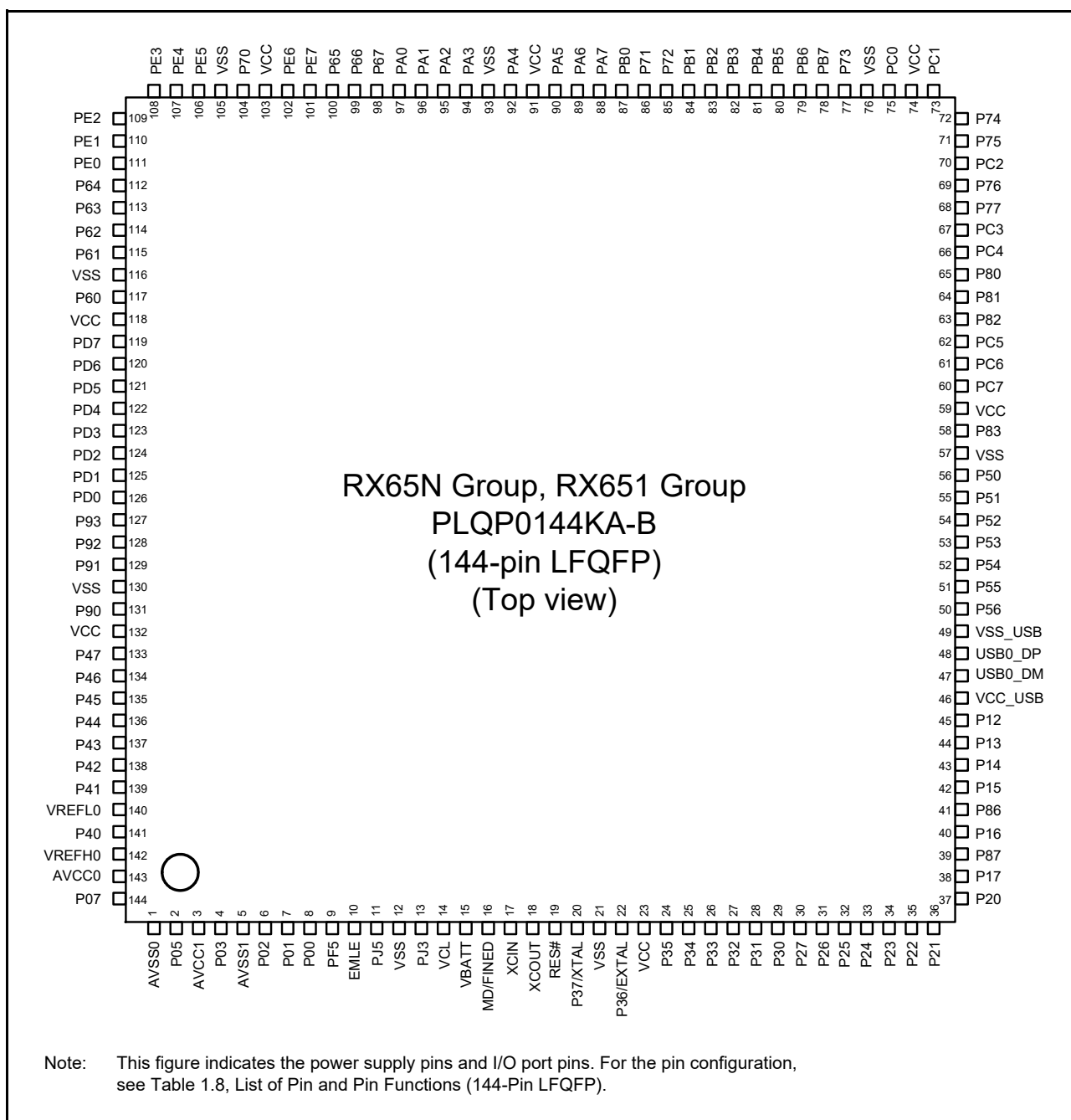
## 1.5.4 145-Pin TFLGA

|    | A     | B      | C      | D   | E                                                                                                     | F     | G            | H     | J   | K   | L   | M           | N           |    |
|----|-------|--------|--------|-----|-------------------------------------------------------------------------------------------------------|-------|--------------|-------|-----|-----|-----|-------------|-------------|----|
| 13 | PE3   | PE4    | VSS    | PE6 | P67                                                                                                   | PA2   | PA4          | PA7   | PB1 | PB5 | VSS | VCC         | P74         | 13 |
| 12 | PE1   | PE2    | P70    | PE5 | P65                                                                                                   | PA1   | VCC          | PB0   | PB2 | PB6 | P73 | PC1         | P75         | 12 |
| 11 | P62   | P61    | PE0    | VCC | P66                                                                                                   | VSS   | PA6          | P71   | PB4 | PB7 | PC2 | PC0         | PC3         | 11 |
| 10 | VSS   | VCC    | P63    | PE7 | PA0                                                                                                   | PA3   | PA5          | P72   | PB3 | P76 | PC4 | P77         | P82         | 10 |
| 9  | PD6   | PD4    | PD7    | P64 | <b>RX65N Group, RX651<br/>Group<br/>PTLG0145KA-A<br/>(145-Pin TFLGA)<br/>(Upper Perspective View)</b> |       |              |       |     | P80 | PC5 | P81         | PC7         | 9  |
| 8  | PD2   | PD0    | PD3    | P60 |                                                                                                       |       |              |       |     | VCC | P83 | PC6         | VSS         | 8  |
| 7  | P92   | P91    | PD1    | PD5 |                                                                                                       |       |              |       |     | P51 | P52 | P50         | P55         | 7  |
| 6  | P90   | P47    | VSS    | P93 |                                                                                                       |       |              |       |     | P53 | P56 | VSS_<br>USB | USB0_<br>DP | 6  |
| 5  | P45   | P43    | P46    | VCC | P44                                                                                                   |       |              |       |     | P54 | P13 | VCC_<br>USB | USB0_<br>DM | 5  |
| 4  | P42   | VREFL0 | P41    | P01 | EMLE                                                                                                  | VBATT | BSCANP       | P35   | P30 | P15 | P24 | P12         | P14         | 4  |
| 3  | P40   | P05    | VREFH0 | P03 | PJ5                                                                                                   | PJ3   | MD/<br>FINED | VSS   | P32 | P31 | P16 | P86         | P87         | 3  |
| 2  | P07   | AVCC0  | P02    | PF5 | VCL                                                                                                   | XCOUT | RES#         | VCC   | P33 | P26 | P23 | P17         | P20         | 2  |
| 1  | AVSS0 | AVCC1  | AVSS1  | P00 | VSS                                                                                                   | XCIN  | XTAL         | EXTAL | P34 | P27 | P25 | P22         | P21         | 1  |
|    | A     | B      | C      | D   | E                                                                                                     | F     | G            | H     | J   | K   | L   | M           | N           |    |

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pin and Pin Functions (145-Pin TFLGA).

Figure 1.6 Pin Assignment (145-Pin TFLGA)

## 1.5.5 144-Pin LFQFP

**Figure 1.7 Pin Assignment (144-Pin LFQFP)**

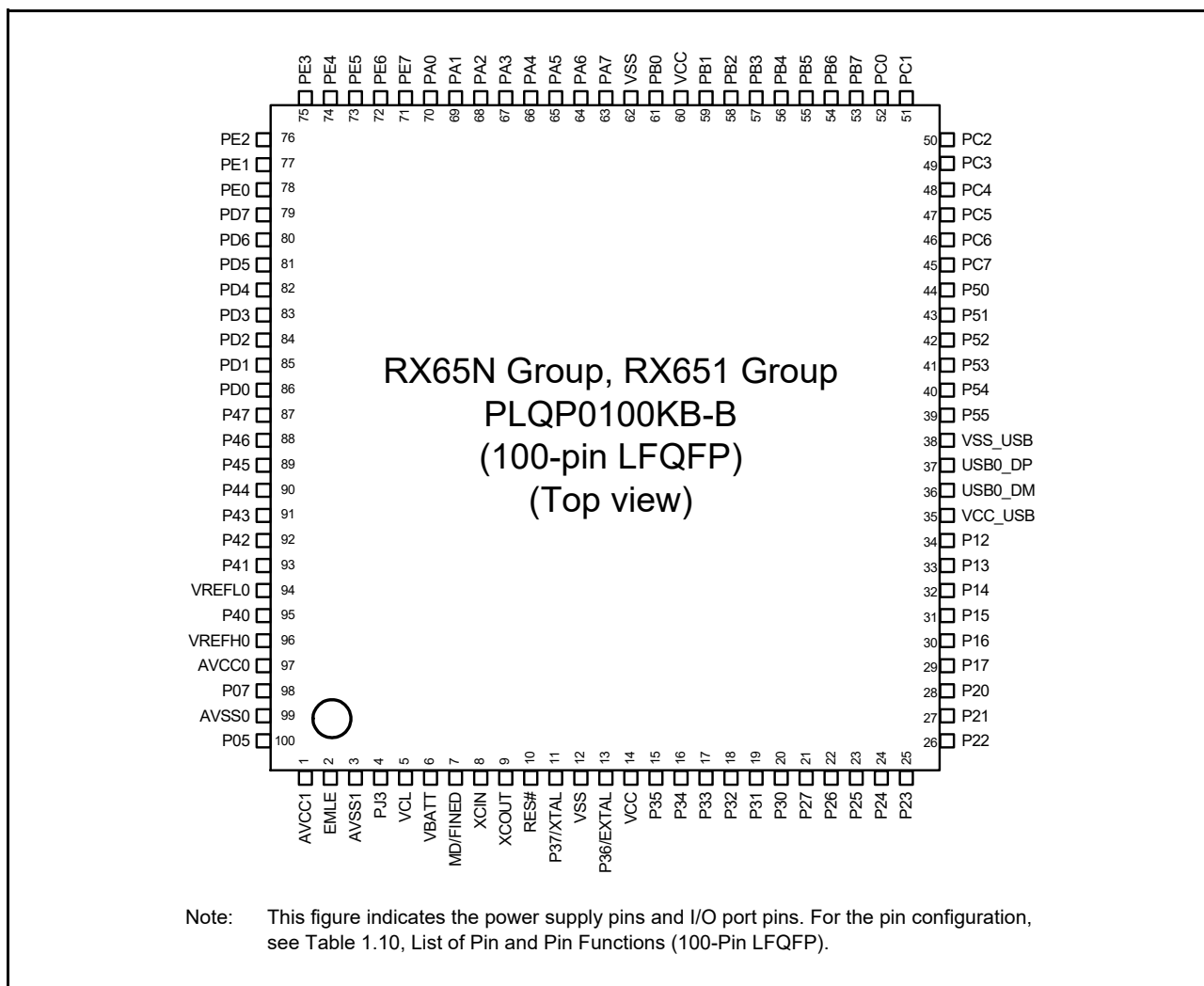
## 1.5.6 100-Pin TFLGA

|    |        |       |        |           |      |       |     |     |          |          |    |
|----|--------|-------|--------|-----------|------|-------|-----|-----|----------|----------|----|
|    | A      | B     | C      | D         | E    | F     | G   | H   | J        | K        |    |
| 10 | PE2    | PE3   | PE4    | PA0       | PA3  | VSS   | VCC | PB7 | PC1      | PC2      | 10 |
| 9  | PE1    | PD7   | PE5    | PA1       | PA5  | PA7   | PB1 | PB6 | PC0      | PC3      | 9  |
| 8  | PE0    | PD6   | PD5    | PE7       | PA4  | PB0   | PB4 | PC6 | PC4      | PC5      | 8  |
| 7  | PD4    | PD3   | PD2    | PE6       | PA6  | PB2   | PB5 | PC7 | P50      | P51      | 7  |
| 6  | PD0    | PD1   | P47    | P46       | PA2  | PB3   | P52 | P54 | VCC_ USB | USB0_ DP | 6  |
| 5  | P43    | P44   | P42    | P45       | P41  | P12   | P53 | P55 | VSS_ USB | USB0_ DM | 5  |
| 4  | VREFL0 | P40   | VREFH0 | VBATT     | P34  | P32   | P27 | P15 | P13      | P14      | 4  |
| 3  | P07    | AVCC0 | PJ3    | MD/ FINED | RES# | P35   | P30 | P16 | P17      | P20      | 3  |
| 2  | AVCC1  | AVSS0 | AVSS1  | XCOUT     | VSS  | VCC   | P31 | P25 | P21      | P22      | 2  |
| 1  | P05    | EMLE  | VCL    | XCIN      | XTAL | EXTAL | P33 | P26 | P24      | P23      | 1  |
|    | A      | B     | C      | D         | E    | F     | G   | H   | J        | K        |    |

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pin and Pin Functions (100-Pin TFLGA).

Figure 1.8 Pin Assignment (100-Pin TFLGA)

## 1.5.7 100-Pin LFQFP

**Figure 1.9 Pin Assignment (100-Pin LFQFP)**

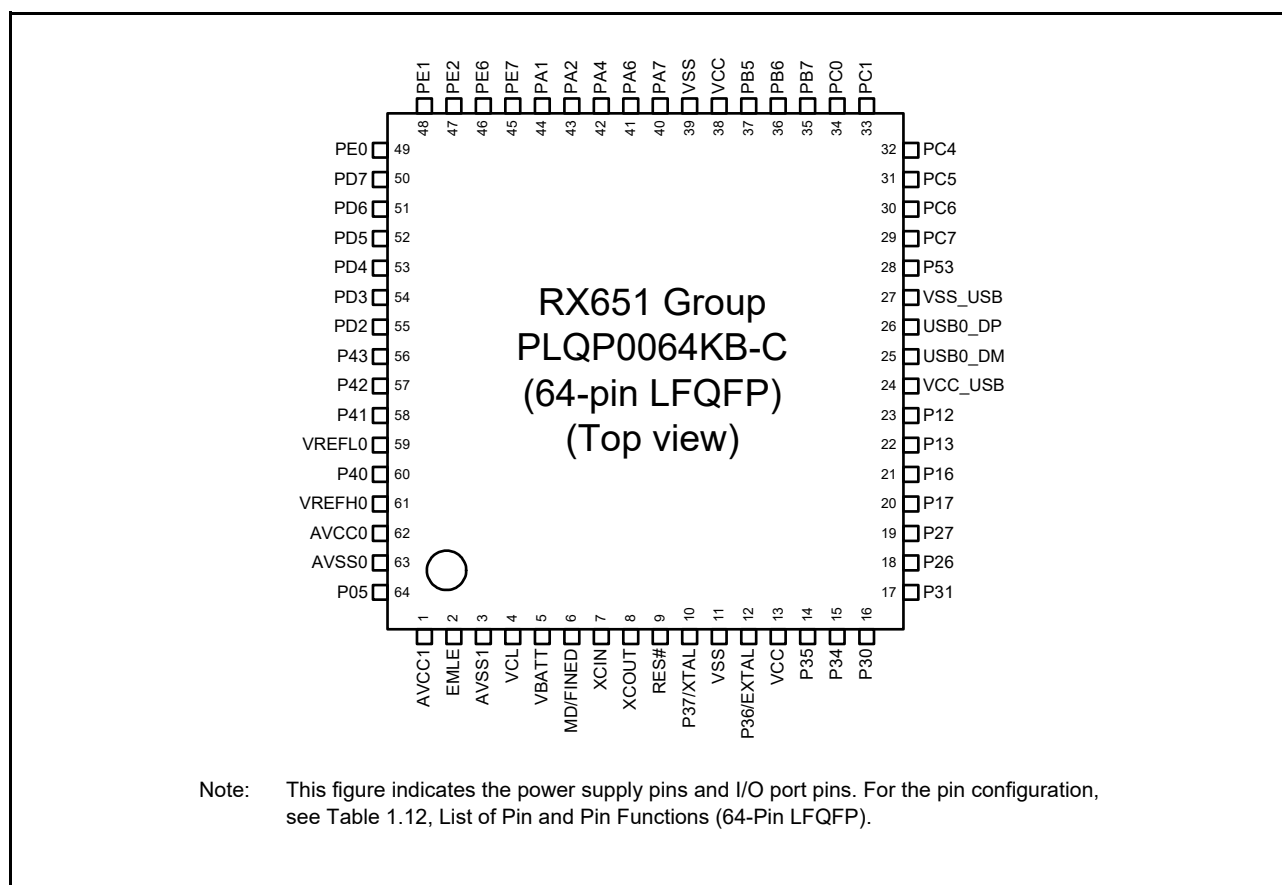
## 1.5.8 64-Pin TFBGA

| RX651 Group                 |  |        |       |          |       |        |       |         |         |  |   |
|-----------------------------|--|--------|-------|----------|-------|--------|-------|---------|---------|--|---|
| PTBG0064KB-A (64-Pin TFBGA) |  |        |       |          |       |        |       |         |         |  |   |
| (Upper Perspective View)    |  |        |       |          |       |        |       |         |         |  |   |
|                             |  | A      | B     | C        | D     | E      | F     | G       | H       |  |   |
| 8                           |  | PE2    | PE6   | PE7      | PA4   | VSS    | PB5   | PC0     | PC1     |  | 8 |
| 7                           |  | PE0    | PE1   | PA1      | PA2   | VCC    | PB6   | PC5     | PC4     |  | 7 |
| 6                           |  | PD7    | PD6   | PD5      | PA6   | PA7    | PB7   | PC7     | PC6     |  | 6 |
| 5                           |  | PD2    | PD3   | PD4      | P43   | BSCANP | P53   | VSS_USB | USB0_DP |  | 5 |
| 4                           |  | VREFL0 | P42   | P41      | P40   | P13    | P12   | VCC_USB | USB0_DM |  | 4 |
| 3                           |  | VREFH0 | AVCC0 | MD/FINED | RES#  | P34    | P35   | P30     | P16     |  | 3 |
| 2                           |  | AVSS0  | AVSS1 | VBATT    | XCOUT | VSS    | VCC   | P31     | P17     |  | 2 |
| 1                           |  | AVCC1  | EMLE  | VCL      | XCIN  | XTAL   | EXTAL | P27     | P26     |  | 1 |
|                             |  | A      | B     | C        | D     | E      | F     | G       | H       |  |   |

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.11, List of Pin and Pin Functions (64-Pin TFBGA).

Figure 1.10 Pin Assignment (64-Pin TFBGA)

## 1.5.9 64-Pin LFQFP

**Figure 1.11 Pin Assignment (64-Pin LFQFP)**

## 1.6 List of Pin and Pin Functions

## 1.6.1 177-Pin TFLGA, 176-Pin LFBGA

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/8)

| Pin Number<br>177-Pin<br>TFLGA<br>176-Pin<br>LFBGA | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC        | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB) | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC            | Interrupt | A/D<br>D/A |
|----------------------------------------------------|-----------------------------------------|----------|--------------------------------|-------------------------------------------------------------|------------------------------------------------------------|----------------------------------------------------------------------------|------------------|-----------|------------|
| A1                                                 | AVSS0                                   |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| A2                                                 | AVCC0                                   |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| A3                                                 | VREFL0                                  |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| A4                                                 |                                         | P42      |                                |                                                             |                                                            |                                                                            |                  | IRQ10-DS  | AN002      |
| A5                                                 |                                         | P46      |                                |                                                             |                                                            |                                                                            |                  | IRQ14-DS  | AN006      |
| A6                                                 | VCC                                     |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| A7                                                 | VSS                                     |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| A8                                                 |                                         | P94      | D20/A20                        |                                                             |                                                            |                                                                            |                  |           |            |
| A9                                                 | VCC                                     |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| A10                                                | TRSYNC1                                 | P97      | D23/A23                        |                                                             |                                                            |                                                                            |                  |           |            |
| A11                                                |                                         | PD6      | D6[A6/D6]                      | MTIC5V/<br>MTIOC8A/<br>POE4#                                | SSLC2-A                                                    | QMO-B/QIO0-B/<br>SDHI_D0-B/<br>MMC_D0-B                                    | LCD_DA<br>TA18-B | IRQ6      | AN106      |
| A12                                                |                                         | P60      | CS0#                           |                                                             |                                                            |                                                                            |                  |           |            |
| A13                                                |                                         | P63      | CAS#/<br>D2[A2/D2]/<br>CS3#    |                                                             |                                                            |                                                                            |                  |           |            |
| A14                                                |                                         | PE1      | D9[A9/D9]/<br>D1[A1/D1]        | MTIOC4C/<br>MTIOC3B/<br>PO18                                | TXD12/<br>SMOS12/<br>SSDA12/<br>TXDX12/<br>SIOX12/SSLB2-B  | MMC_D5-B                                                                   | LCD_DA<br>TA15-B |           | ANEX1      |
| A15                                                |                                         | PE2      | D10[A10/<br>D10]/D2[A2/<br>D2] | MTIOC4A/<br>PO23/TIC3                                       | RXD12/<br>SMISO12/<br>SSCL12/<br>RXDX12/SSLB3-B            | MMC_D6-B                                                                   | LCD_DA<br>TA14-B | IRQ7-DS   | AN100      |
| B1                                                 |                                         | P05      |                                |                                                             |                                                            |                                                                            |                  | IRQ13     | DA1        |
| B2                                                 |                                         | P07      |                                |                                                             |                                                            |                                                                            |                  | IRQ15     | ADTRG0#    |
| B3                                                 |                                         | P40      |                                |                                                             |                                                            |                                                                            |                  | IRQ8-DS   | AN000      |
| B4                                                 |                                         | P41      |                                |                                                             |                                                            |                                                                            |                  | IRQ9-DS   | AN001      |
| B5                                                 |                                         | P47      |                                |                                                             |                                                            |                                                                            |                  | IRQ15-DS  | AN007      |
| B6                                                 |                                         | P91      | D17/A17                        |                                                             | SCK7                                                       |                                                                            |                  |           | AN115      |
| B7                                                 |                                         | P92      | D18/A18                        | POE4#                                                       | RXD7/SMISO7/<br>SSCL7                                      |                                                                            |                  |           | AN116      |
| B8                                                 |                                         | PD1      | D1[A1/D1]                      | MTIOC4B/<br>POE0#                                           | MOSIC-A/CTX0                                               |                                                                            | LCD_DA<br>TA23-B | IRQ1      | AN109      |
| B9                                                 | TRDATA5                                 | P96      | D22/A22                        |                                                             |                                                            |                                                                            |                  |           |            |
| B10                                                |                                         | PD4      | D4[A4/D4]                      | MTIOC8B/<br>POE11#                                          | SSLC0-A                                                    | QSSL-B/<br>SDHI_CMD-B/<br>MMC_CMD-B                                        | LCD_DA<br>TA20-B | IRQ4      | AN112      |
| B11                                                | TRDATA7                                 | PG1      | D25                            |                                                             |                                                            |                                                                            |                  |           |            |
| B12                                                | VSS                                     |          |                                |                                                             |                                                            |                                                                            |                  |           |            |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/8)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC        | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB) | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC            | Interrupt    | A/D<br>D/A |
|------------|-----------------------------------------|----------|--------------------------------|-------------------------------------------------------------|------------------------------------------------------------|----------------------------------------------------------------------------|------------------|--------------|------------|
| B13        |                                         | P64      | WE#/D3[A3/<br>D3]/CS4#         |                                                             |                                                            |                                                                            |                  |              |            |
| B14        |                                         | PE0      | D8[A8/D8]/<br>D0[A0/D0]        | MTIOC3D                                                     | SCK12/SSLB1-B                                              | MMC_D4-B                                                                   | LCD_DA<br>TA16-B |              | ANEX0      |
| B15        |                                         | PE3      | D11[A11/<br>D11]/D3[A3/<br>D3] | MTIOC4B/<br>PO26/TOC3/<br>POE8#                             | ET0_ERXD3/<br>CTS12#/<br>RTS12#/SS12#                      | MMC_D7-B                                                                   | LCD_DA<br>TA13-B |              | AN101      |
| C1         | AVSS1                                   |          |                                |                                                             |                                                            |                                                                            |                  |              |            |
| C2         | AVCC1                                   |          |                                |                                                             |                                                            |                                                                            |                  |              |            |
| C3         | VREFH0                                  |          |                                |                                                             |                                                            |                                                                            |                  |              |            |
| C4         |                                         | P43      |                                |                                                             |                                                            |                                                                            |                  | IRQ11-<br>DS | AN003      |
| C5         |                                         | P45      |                                |                                                             |                                                            |                                                                            |                  | IRQ13-<br>DS | AN005      |
| C6         |                                         | P90      | D16/A16                        |                                                             | TXD7/SMOSI7/<br>SSDA7                                      |                                                                            |                  |              | AN114      |
| C7         |                                         | PD0      | D0[A0/D0]                      | POE4#                                                       |                                                            |                                                                            | LCD_EX<br>TCLK-B | IRQ0         | AN108      |
| C8         |                                         | PD2      | D2[A2/D2]                      | MTIOC4D/TIC2                                                | MISOC-A/CRX0                                               | QIO2-B/SDHI_D2-<br>B/MMC_D2-B                                              | LCD_DA<br>TA22-B | IRQ2         | AN110      |
| C9         |                                         | PD3      | D3[A3/D3]                      | MTIOC8D/<br>TOC2/POE8#                                      | RSPCKC-A                                                   | QIO3-B/SDHI_D3-<br>B/MMC_D3-B                                              | LCD_DA<br>TA21-B | IRQ3         | AN111      |
| C10        | TRDATA6                                 | PG0      | D24                            |                                                             |                                                            |                                                                            |                  |              |            |
| C11        | VCC                                     |          |                                |                                                             |                                                            |                                                                            |                  |              |            |
| C12        |                                         | P62      | RAS#/<br>D1[A1/D1]/<br>CS2#    |                                                             |                                                            |                                                                            |                  |              |            |
| C13        |                                         | PE4      | D12[A12/<br>D12]/D4[A4/<br>D4] | MTIOC4D/<br>MTIOC1A/<br>PO28                                | ET0_ERXD2/<br>SSLB0-B                                      |                                                                            | LCD_DA<br>TA12-B |              | AN102      |
| C14        | VSS                                     |          |                                |                                                             |                                                            |                                                                            |                  |              |            |
| C15        |                                         | P70      | SDCLK                          |                                                             |                                                            |                                                                            |                  |              |            |
| D1         |                                         | P01      |                                | TMC10                                                       | RXD6/SMISO6/<br>SSCL6                                      |                                                                            |                  | IRQ9         | AN119      |
| D2         |                                         | P02      |                                | TMC11                                                       | SCK6                                                       |                                                                            |                  | IRQ10        | AN120      |
| D3         |                                         | P03      |                                |                                                             |                                                            |                                                                            |                  | IRQ11        | DA0        |
| D4         |                                         | P00      |                                | TMRI0                                                       | TXD6/SMOSI6/<br>SSDA6                                      |                                                                            |                  | IRQ8         | AN118      |
| D5         |                                         | P44      |                                |                                                             |                                                            |                                                                            |                  | IRQ12-<br>DS | AN004      |
| D6         |                                         | P93      | D19/A19                        | POE0#                                                       | CTS7#/RTS7#/<br>SS7#                                       |                                                                            |                  |              | AN117      |
| D7         | TRDATA4                                 | P95      | D21/A21                        |                                                             |                                                            |                                                                            |                  |              |            |
| D8         | VSS                                     |          |                                |                                                             |                                                            |                                                                            |                  |              |            |
| D9         |                                         | PD5      | D5[A5/D5]                      | MTIC5W/<br>MTIOC8C/<br>POE10#                               | SSLC1-A                                                    | QSPCLK-B/<br>SDHI_CLK-B/<br>MMC_CLK-B                                      | LCD_DA<br>TA19-B | IRQ5         | AN113      |
| D10        |                                         | PD7      | D7[A7/D7]                      | MTIC5U/<br>POE0#                                            | SSLC3-A                                                    | QMI-B/QIO1-B/<br>SDHI_D1-B/<br>MMC_D1-B                                    | LCD_DA<br>TA17-B | IRQ7         | AN107      |
| D11        |                                         | P61      | SDCS#/<br>D0[A0/D0]/<br>CS1#   |                                                             |                                                            |                                                                            |                  |              |            |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/8)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC        | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB) | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC            | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|--------------------------------|-------------------------------------------------------------|------------------------------------------------------------|----------------------------------------------------------------------------|------------------|-----------|------------|
| D12        |                                         | PE5      | D13[A13/<br>D13]/D5[A5/<br>D5] | MTIOC4C/<br>MTIOC2B                                         | ET0_RX_CLK/<br>REF50CK0/<br>RSPCKB-B                       |                                                                            | LCD_DA<br>TA11-B | IRQ5      | AN103      |
| D13        | VCC                                     |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| D14        |                                         | PE7      | D15[A15/<br>D15]/D7[A7/<br>D7] | MTIOC6A/<br>TOC1                                            | MISOB-B                                                    | SDHI_WP/<br>MMC_RES#-B                                                     | LCD_DA<br>TA9-B  | IRQ7      | AN105      |
| D15        |                                         | P65      | CKE/CS5#                       |                                                             |                                                            |                                                                            |                  |           |            |
| E1         |                                         | PJ5      |                                | POE8#                                                       | CTS2#/RTS2#/<br>SS2#                                       |                                                                            |                  |           |            |
| E2         | EMLE                                    |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| E3         |                                         | PF5      |                                |                                                             |                                                            |                                                                            |                  | IRQ4      |            |
| E4         | VSS                                     |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| E5 *1      | NC                                      |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| E12        |                                         | PE6      | D14[A14/<br>D14]/D6[A6/<br>D6] | MTIOC6C/TIC1                                                | MOSIB-B                                                    | SDHI_CD/<br>MMC_CD-B                                                       | LCD_DA<br>TA10-B | IRQ6      | AN104      |
| E13        | TRDATA0                                 | PG2      | D26                            |                                                             |                                                            |                                                                            |                  |           |            |
| E14        | TRDATA1                                 | PG3      | D27                            |                                                             |                                                            |                                                                            |                  |           |            |
| E15        |                                         | P67      | DQM1/CS7#                      | MTIOC7C                                                     |                                                            |                                                                            |                  | IRQ15     |            |
| F1         | VBATT                                   |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| F2         | VCL                                     |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| F3         |                                         | PJ3      | EDACK1                         | MTIOC3C                                                     | ET0_EXOUT/<br>CTS6#/RTS6#/<br>SS6#/CTS0#/<br>RTS0#/SS0#    |                                                                            |                  |           |            |
| F4         | BSCANP                                  |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| F12        |                                         | P66      | DQM0/CS6#                      | MTIOC7D                                                     |                                                            |                                                                            |                  |           |            |
| F13        | TRSYNC                                  | PG4      | D28                            |                                                             |                                                            |                                                                            |                  |           |            |
| F14        |                                         | PA0      | DQM2/<br>BC0#/A0               | MTIOC4A/<br>MTIOC6D/<br>TIOCA0/PO16/<br>CACREF              | ET0_TX_EN/<br>RMII0_TXD_EN/<br>SSLA1-B                     |                                                                            | LCD_DA<br>TA8-B  |           |            |
| F15        | VSS                                     |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| G1         | XCIN                                    |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| G2         | XCOUT                                   |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| G3         | MD/FINED                                |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| G4         | TRST#                                   | PF4      |                                |                                                             |                                                            |                                                                            |                  |           |            |
| G12        | TRCLK                                   | PG5      | D29                            |                                                             |                                                            |                                                                            |                  |           |            |
| G13        | TRDATA2                                 | PG6      | D30                            |                                                             |                                                            |                                                                            |                  |           |            |
| G14        |                                         | PA1      | DQM3/A1                        | MTIOC0B/<br>MTCLKC/<br>MTIOC7B/<br>TIOCB0/PO17              | ET0_WOL/<br>SCK5/SSLA2-B                                   |                                                                            | LCD_DA<br>TA7-B  | IRQ11     |            |
| G15        | VCC                                     |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| H1         | XTAL                                    | P37      |                                |                                                             |                                                            |                                                                            |                  |           |            |
| H2         | VSS                                     |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| H3         | RES#                                    |          |                                |                                                             |                                                            |                                                                            |                  |           |            |
| H4         | UPSEL                                   | P35      |                                |                                                             |                                                            |                                                                            |                  | NMI       |            |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/8)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC)                 | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)               | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSI,<br>MMCIF, PDC) | GLCDC           | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|-------------------------|-----------------------------------------------------------------------------|--------------------------------------------------------------------------|---------------------------------------------------------------------------|-----------------|-----------|------------|
| H12        |                                         | PA4      | A4                      | MTIC5U/<br>MTCLKA/<br>TIOCA1/<br>TMRI0/PO20                                 | ET0_MDC/TXD5/<br>SMOSI5/SSDA5/<br>SSLA0-B                                |                                                                           | LCD_DA<br>TA4-B | IRQ5-DS   |            |
| H13        |                                         | PA3      | A3                      | MTIOC0D/<br>MTCLKD/<br>TIOC0D/<br>TCLKB/PO19                                | ET0_MDIO/<br>RXD5/SMISO5/<br>SSCL5                                       |                                                                           | LCD_DA<br>TA5-B | IRQ6-DS   |            |
| H14        |                                         | PA2      | A2                      | MTIOC7A/<br>PO18                                                            | RXD5/SMISO5/<br>SSCL5/SSLA3-B                                            |                                                                           | LCD_DA<br>TA6-B |           |            |
| H15        | TRDATA3                                 | PG7      | D31                     |                                                                             |                                                                          |                                                                           |                 |           |            |
| J1         | EXTAL                                   | P36      |                         |                                                                             |                                                                          |                                                                           |                 |           |            |
| J2         | VCC                                     |          |                         |                                                                             |                                                                          |                                                                           |                 |           |            |
| J3         |                                         | P34      |                         | MTIOC0A/<br>TMCI3/PO12/<br>POE10#                                           | ET0_LINKSTA/<br>SCK6/SCK0                                                |                                                                           |                 | IRQ4      |            |
| J4         | TMS                                     | PF3      |                         |                                                                             |                                                                          |                                                                           |                 |           |            |
| J12        |                                         | PA5      | A5                      | MTIOC6B/<br>TIOCB1/PO21                                                     | ET0_LINKSTA/<br>RSPCKA-B                                                 |                                                                           | LCD_DA<br>TA3-B |           |            |
| J13        | VSS                                     |          |                         |                                                                             |                                                                          |                                                                           |                 |           |            |
| J14        |                                         | PA7      | A7                      | TIOCB2/PO23                                                                 | ET0_WOL/<br>MISOA-B                                                      |                                                                           | LCD_DA<br>TA1-B |           |            |
| J15        |                                         | PA6      | A6                      | MTIC5V/<br>MTCLKB/<br>TIOCA2/<br>TMCI3/PO22/<br>POE10#                      | ET0_EXOUT/<br>CTS5#/RTS5#/<br>SS5#/MOSIA-B                               |                                                                           | LCD_DA<br>TA2-B |           |            |
| K1         |                                         | P33      | EDREQ1                  | MTIOC0D/<br>TIOC0D/<br>TMRI3/PO11/<br>POE4#/<br>POE11#                      | RXD6/SMISO6/<br>SSCL6/RXD0/<br>SMISO0/SSCL0/<br>CRX0                     | PCKO                                                                      |                 | IRQ3-DS   |            |
| K2         |                                         | P32      |                         | MTIOC0C/<br>TIOCC0/<br>TMO3/PO10/<br>RTCIC2/<br>RTCOUT/<br>POE0#/<br>POE10# | TXD6/SMOSI6/<br>SSDA6/TXD0/<br>SMOSI0/SSDA0/<br>CTX0/<br>USB0_VBUSEN     | VSYNC                                                                     |                 | IRQ2-DS   |            |
| K3         | TDI                                     | PF2      |                         |                                                                             | RXD1/SMISO1/<br>SSCL1                                                    |                                                                           |                 |           |            |
| K4         | TCK                                     | PF1      |                         |                                                                             | SCK1                                                                     |                                                                           |                 |           |            |
| K12        |                                         | PB2      | A10                     | TIOCC3/<br>TCLKC/PO26                                                       | ET0_RX_CLK/<br>REF50CK0/<br>CTS4#/RTS4#/<br>SS4#/CTS6#/<br>RTS6#/SS6#    | SDSI_D2-B                                                                 | LCD_TC<br>ON2-B |           |            |
| K13        |                                         | P71      | A18/CS1#                |                                                                             | ET0_MDIO                                                                 |                                                                           |                 |           |            |
| K14        | VCC                                     |          |                         |                                                                             |                                                                          |                                                                           |                 |           |            |
| K15        |                                         | PB0      | A8                      | MTIC5W/<br>TIOCA3/PO24                                                      | ET0_ERXD1/<br>RMII0_RXD1/<br>RXD4/SMISO4/<br>SSCL4/RXD6/<br>SMISO6/SSCL6 |                                                                           | LCD_DA<br>TA0-B | IRQ12     |            |
| L1         |                                         | P31      |                         | MTIOC4D/<br>TMCI2/PO9/<br>RTCIC1                                            | CTS1#/RTS1#/<br>SS1#/SSLB0-A                                             |                                                                           |                 | IRQ1-DS   |            |
| L2         |                                         | P30      |                         | MTIOC4B/<br>TMRI3/PO8/<br>RTCIC0/<br>POE8#                                  | RXD1/SMISO1/<br>SSCL1/MISOB-A                                            |                                                                           |                 | IRQ0-DS   |            |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (5/8)**

| Pin Number<br>177-Pin TFLGA<br>176-Pin LFBGA | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC          | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC)   | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)                      | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC            | Interrupt | A/D<br>D/A  |
|----------------------------------------------|-----------------------------------------|----------|----------------------------------|---------------------------------------------------------------|---------------------------------------------------------------------------------|----------------------------------------------------------------------------|------------------|-----------|-------------|
| L3                                           | TDO                                     | PF0      |                                  |                                                               | TXD1/SMOSI1/<br>SSDA1                                                           |                                                                            |                  |           |             |
| L4                                           |                                         | P25      | CS5#/<br>EDACK1                  | MTIOC4C/<br>MTCLKB/<br>TIOCA4/PO5                             | RXD3/SMISO3/<br>SSCL3                                                           | SDHI_CD/HSYNC                                                              |                  |           | ADTRG0<br># |
| L12                                          |                                         | PB6      | A14                              | MTIOC3D/<br>TIOCA5/PO30                                       | ET0_ETXD1/<br>RMII0_TXD1/<br>RXD9/SMISO9/<br>SSCL9/<br>SMISO11/<br>SSCL11/RXD11 | SDSI_D0-B                                                                  |                  |           |             |
| L13                                          |                                         | PB3      | A11                              | MTIOC0A/<br>MTIOC4A/<br>TIOCD3/<br>TCLKD/TMO0/<br>PO27/POE11# | ET0_RX_ER/<br>RMII0_RX_ER/<br>SCK4/SCK6                                         | SDSI_D3-B                                                                  | LCD_TC<br>ON1-B  |           |             |
| L14                                          |                                         | PB1      | A9                               | MTIOC0C/<br>MTIOC4C/<br>TIOCB3/<br>TMCI0/PO25                 | ET0_ERXD0/<br>RMII0_RXD0/<br>TXD4/SMOSI4/<br>SSDA4/TXD6/<br>SMOSI6/SSDA6        |                                                                            | LCD_TC<br>ON3-B  | IRQ4-DS   |             |
| L15                                          |                                         | P72      | A19/CS2#                         |                                                               | ET0_MDC                                                                         |                                                                            | LCD_DA<br>TA23-A |           |             |
| M1                                           |                                         | P27      | CS7#                             | MTIOC2B/<br>TMCI3/PO7                                         | SCK1/RSPCKB-<br>A                                                               |                                                                            |                  |           |             |
| M2                                           |                                         | P26      | CS6#                             | MTIOC2A/<br>TMO1/PO6                                          | TXD1/SMOSI1/<br>SSDA1/CTS3#/<br>RTS3#/SS3#/<br>MOSIB-A                          |                                                                            |                  |           |             |
| M3                                           |                                         | P24      | CS4#/<br>EDREQ1                  | MTIOC4A/<br>MTCLKA/<br>TIOCB4/<br>TMRI1/PO4                   | SCK3/<br>USB0_VBUSEN                                                            | SDHI_WP/PIXCLK                                                             |                  |           |             |
| M4                                           |                                         | P86      |                                  | MTIOC4D/<br>TIOCA0                                            | SMISO10/<br>SSCL10/RXD10                                                        | PIXD1                                                                      |                  |           |             |
| M5                                           |                                         | PJ2      |                                  |                                                               | TXD8/SMOSI8/<br>SSDA8/SSLC3-B                                                   |                                                                            | LCD_TC<br>ON2-A  |           |             |
| M6                                           |                                         | PJ1      |                                  | MTIOC6A                                                       | RXD8/SMISO8/<br>SSCL8/SSLC2-B                                                   |                                                                            | LCD_TC<br>ON3-A  |           |             |
| M7                                           |                                         | P85      |                                  | MTIOC6C/<br>TIOCC0                                            |                                                                                 |                                                                            | LCD_DA<br>TA1-A  |           |             |
| M8                                           |                                         | P55      | D0[A0/D0]/<br>EDREQ0/<br>WAIT#   | MTIOC4D/<br>TMO3                                              | ET0_EXOUT/<br>TXD7/SMOSI7/<br>SSDA7/MISOC-<br>B/CRX1                            |                                                                            | LCD_DA<br>TA5-A  | IRQ10     |             |
| M9                                           |                                         | P50      | WR0#/WR#                         |                                                               | TXD2/SMOSI2/<br>SSDA2/SSLB1-A                                                   |                                                                            |                  |           |             |
| M10                                          |                                         | PC5      | D3[A3/D3]/<br>A21/CS2#/<br>WAIT# | MTIOC3B/<br>MTCLKD/<br>TMRI2/PO29                             | ET0_ETXD2/<br>SCK8/SCK10/<br>RSPCKA-A                                           | MMC_D5-A                                                                   | LCD_DA<br>TA11-A |           |             |
| M11                                          |                                         | P81      | EDACK0                           | MTIOC3D/<br>PO27                                              | ET0_ETXD0/<br>RMII0_TXD0/<br>SMISO10/<br>SSCL10/RXD10                           | QIO3-A/SDHI_CD/<br>MMC_D3-A                                                | LCD_DA<br>TA13-A |           |             |
| M12                                          |                                         | P77      | CS7#                             | PO23                                                          | ET0_RX_ER/<br>RMII0_RX_ER/<br>SMOSI11/<br>SSDA11/TXD11                          | QSPCLK-A/<br>SDHI_CLK-A/<br>SDSI_CLK-A/<br>MMC_CLK-A                       | LCD_DA<br>TA17-A |           |             |
| M13                                          |                                         | PB7      | A15                              | MTIOC3B/<br>TIOCB5/PO31                                       | ET0_CRS/<br>RMII0_CRS_DV/<br>TXD9/SMOSI9/<br>SSDA9/<br>SMOSI11/<br>SSDA11/TXD11 | SDSI_D1-B                                                                  |                  |           |             |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (6/8)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC      | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC)              | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)                  | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSI,<br>MMCIF, PDC) | GLCDC            | Interrupt | A/D<br>D/A  |
|------------|-----------------------------------------|----------|------------------------------|--------------------------------------------------------------------------|-----------------------------------------------------------------------------|---------------------------------------------------------------------------|------------------|-----------|-------------|
| M14        |                                         | PB5      | A13                          | MTIOC2A/<br>MTIOC1B/<br>TIOCB4/<br>TMRI1/PO29/<br>POE4#                  | ET0_ETXD0/<br>RMII0_TXD0/<br>SCK9/SCK11                                     | SDSI_CLK-B                                                                | LCD_CLK-B        |           |             |
| M15        |                                         | PB4      | A12                          | TIOCA4/PO28                                                              | ET0_TX_EN/<br>RMII0_TXD_EN/<br>CTS9#/RTS9#/<br>SS9#/SS11#/<br>CTS11#/RTS11# | SDSI_CMD-B                                                                | LCD_TC<br>ON0-B  |           |             |
| N1         | VCC                                     |          |                              |                                                                          |                                                                             |                                                                           |                  |           |             |
| N2         |                                         | P23      | EDACK0                       | MTIOC3D/<br>MTCLKD/<br>TIOCD3/PO3                                        | TXD3/SMOSI3/<br>SSDA3/CTS0#/<br>RTS0#/SS0#                                  | SDHI_D1-C/PIXD7                                                           |                  |           |             |
| N3         |                                         | P22      | EDREQ0                       | MTIOC3B/<br>MTCLKC/<br>TIOCC3/<br>TMO0/PO2                               | SCK0/<br>USB0_OVRCUR<br>B                                                   | SDHI_D0-C/PIXD6                                                           |                  |           |             |
| N4         |                                         | P15      |                              | MTIOC0B/<br>MTCLKB/<br>TIOCB2/<br>TCLKB/TMC12/<br>PO13                   | RXD1/SMISO1/<br>SSCL1/SCK3/<br>CRX1-DS                                      | PIXD0                                                                     |                  | IRQ5      |             |
| N5         |                                         | P12      | WR3#/BC3#                    | MTIC5U/<br>TMC11                                                         | RXD2/SMISO2/<br>SSCL2/<br>SCL0[FM+]                                         |                                                                           | LCD_TC<br>ON1-A  | IRQ2      |             |
| N6         |                                         | PJ0      |                              | MTIOC6B                                                                  | SCK8/SSLC1-B                                                                |                                                                           | LCD_DA<br>TA0-A  |           |             |
| N7         |                                         | P84      |                              | MTIOC6D                                                                  |                                                                             |                                                                           | LCD_DA<br>TA2-A  |           |             |
| N8         |                                         | P54      | D1[A1/D1]/<br>EDACK0/<br>ALE | MTIOC4B/<br>TMC11                                                        | ET0_LINKSTA/<br>CTS2#/RTS2#/<br>SS2#/MOSIC-B/<br>CTX1                       |                                                                           | LCD_DA<br>TA6-A  |           |             |
| N9         |                                         | P51      | WR1#/<br>BC1#/<br>WAIT#      |                                                                          | SCK2/SSLB2-A                                                                |                                                                           |                  |           |             |
| N10        | UB                                      | PC7      | A23/CS0#                     | MTIOC3A/<br>MTCLKB/<br>TMO2/PO31/<br>TOC0/<br>CACREF                     | ET0_COL/TXD8/<br>SMOSI8/SSDA8/<br>SMOSI10/<br>SSDA10/TXD10/<br>MISOA-A      | MMC_D7-A                                                                  | LCD_DA<br>TA9-A  | IRQ14     |             |
| N11        |                                         | P82      | EDREQ1                       | MTIOC4A/<br>PO28                                                         | ET0_ETXD1/<br>RMII0_TXD1/<br>SMOSI10/<br>SSDA10/TXD10                       | MMC_D4-A                                                                  | LCD_DA<br>TA12-A |           |             |
| N12        |                                         | PC3      | A19                          | MTIOC4D/<br>TCLKB/PO24                                                   | ET0_TX_ER/<br>TXD5/SMOSI5/<br>SSDA5                                         | QMO-A/QIO0-A/<br>SDHI_D0-A/<br>SDSI_D0-A/<br>MMC_D0-A                     | LCD_DA<br>TA16-A |           |             |
| N13        |                                         | PC0      | A16                          | MTIOC3C/<br>TCLKC/PO17                                                   | ET0_ERXD3/<br>CTS5#/RTS5#/<br>SS5#/SSLA1-A                                  |                                                                           |                  | IRQ14     |             |
| N14        |                                         | P73      | CS3#                         | PO16                                                                     | ET0_WOL                                                                     |                                                                           | LCD_EX<br>TCLK-A |           |             |
| N15        | VSS                                     |          |                              |                                                                          |                                                                             |                                                                           |                  |           |             |
| P1         | VSS                                     |          |                              |                                                                          |                                                                             |                                                                           |                  |           |             |
| P2         |                                         | P17      |                              | MTIOC3A/<br>MTIOC3B/<br>MTIOC4B/<br>TIOCB0/<br>TCLKD/TMO1/<br>PO15/POE8# | SCK1/TXD3/<br>SMOSI3/SSDA3/<br>SDA2-DS                                      | SDHI_D3-C/PIXD3                                                           |                  | IRQ7      | ADTRG1<br># |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (7/8)**

| Pin Number<br>177-Pin<br>TFLGA<br>176-Pin<br>LFBGA | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC)  | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)                                                 | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC            | Interrupt | A/D<br>D/A  |
|----------------------------------------------------|-----------------------------------------|----------|-------------------------|--------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------|------------------|-----------|-------------|
| P3                                                 |                                         | P87      |                         | MTIOC4C/<br>TIOCA2                                           | SMOSI10/<br>SSDA10/TXD10                                                                                   | SDHI_D2-C/PIXD2                                                            |                  |           |             |
| P4                                                 |                                         | P14      |                         | MTIOC3A/<br>MTCLKA/<br>TIOCB5/<br>TCLKA/TMRI2/<br>PO15       | CTS1#/RTS1#/<br>SS1#/CTX1/<br>USB0_OVRCUR<br>A                                                             |                                                                            | LCD_CL<br>K-A    | IRQ4      |             |
| P5                                                 | VCC_USB                                 |          |                         |                                                              |                                                                                                            |                                                                            |                  |           |             |
| P6                                                 | VSS_USB                                 |          |                         |                                                              |                                                                                                            |                                                                            |                  |           |             |
| P7                                                 |                                         | P57      |                         |                                                              | RXD7/SMISO7/<br>SSCL7/SSLC0-B                                                                              |                                                                            | LCD_DA<br>TA3-A  |           |             |
| P8                                                 |                                         | P10      | ALE                     | MTIC5W/<br>TMRI3                                             |                                                                                                            |                                                                            |                  | IRQ0      |             |
| P9                                                 |                                         | P52      | RD#                     |                                                              | RXD2/SMISO2/<br>SSCL2/SSLB3-A                                                                              |                                                                            |                  |           |             |
| P10                                                |                                         | P83      | EDACK1                  | MTIOC4C                                                      | ET0_CRS/<br>RMII0_CRS_DV/<br>SCK10/SS10#/<br>CTS10#                                                        |                                                                            | LCD_DA<br>TA8-A  |           |             |
| P11                                                |                                         | PC6      | D2[A2/D2]/<br>A22/CS1#  | MTIOC3C/<br>MTCLKA/<br>TMC12/PO30/<br>TIC0                   | ET0_ETXD3/<br>RXD8/SMISO8/<br>SSCL8/<br>SMISO10/<br>SSCL10/RXD10/<br>MOSIA-A                               | MMC_D6-A                                                                   | LCD_DA<br>TA10-A | IRQ13     |             |
| P12                                                |                                         | PC4      | A20/CS3#                | MTIOC3D/<br>MTCLKC/<br>TMC11/PO25/<br>POE0#                  | ET0_TX_CLK/<br>SCK5/CTS8#/<br>RTS8#/SS8#/<br>SS10#/CTS10#/<br>RTS10#/SSLA0-<br>A                           | QMI-A/QIO1-A/<br>SDHI_D1-A/<br>SDSI_D1-A/<br>MMC_D1-A                      | LCD_DA<br>TA15-A |           |             |
| P13                                                |                                         | PC2      | A18                     | MTIOC4B/<br>TCLKA/PO21                                       | ET0_RX_DV/<br>RXD5/SMISO5/<br>SSCL5/SSLA3-A                                                                | SDHI_D3-A/<br>SDSI_D3-A/<br>MMC_CD-A                                       | LCD_DA<br>TA19-A |           |             |
| P14                                                |                                         | P75      | CS5#                    | PO20                                                         | ET0_ERXD0/<br>RMII0_RXD0/<br>SCK11/RTS11#                                                                  | SDHI_D2-A/<br>SDSI_D2-A/<br>MMC_RES#-A                                     | LCD_DA<br>TA20-A |           |             |
| P15                                                | VCC                                     |          |                         |                                                              |                                                                                                            |                                                                            |                  |           |             |
| R1                                                 |                                         | P21      |                         | MTIOC1B/<br>MTIOC4A/<br>TIOCA3/<br>TMC10/PO1                 | RXD0/SMISO0/<br>SSCL0/SCL1/<br>USB0_EXICEN                                                                 | SDHI_CLK-C/<br>PIXD5                                                       |                  | IRQ9      |             |
| R2                                                 |                                         | P20      |                         | MTIOC1A/<br>TIOCB3/<br>TMRI0/PO0                             | TXD0/SMOSI0/<br>SSDA0/SDA1/<br>USB0_ID                                                                     | SDHI_CMD-C/<br>PIXD4                                                       |                  | IRQ8      |             |
| R3                                                 |                                         | P16      |                         | MTIOC3C/<br>MTIOC3D/<br>TIOCB1/<br>TCLKC/TMO2/<br>PO14/RTCOU | TXD1/SMOSI1/<br>SSDA1/RXD3/<br>SMISO3/SSCL3/<br>SCL2-DS/<br>USB0_VBUSEN/<br>USB0_VBUS/<br>USB0_OVRCUR<br>B |                                                                            |                  | IRQ6      | ADTRG0<br># |
| R4                                                 |                                         | P13      | WR2#/BC2#               | MTIOC0B/<br>TIOCA5/TMO3/<br>PO13                             | TXD2/SMOSI2/<br>SSDA2/<br>SDA0[FM+]                                                                        |                                                                            | LCD_TC<br>ON0-A  | IRQ3      | ADTRG1<br># |
| R5                                                 |                                         |          |                         |                                                              | USB0_DM                                                                                                    |                                                                            |                  |           |             |
| R6                                                 |                                         |          |                         |                                                              | USB0_DP                                                                                                    |                                                                            |                  |           |             |
| R7                                                 |                                         | P56      | EDACK1                  | MTIOC3C/<br>TIOCA1                                           | SCK7/RSPCKC-<br>B                                                                                          |                                                                            | LCD_DA<br>TA4-A  |           |             |
| R8                                                 |                                         | P11      |                         | MTIC5V/TMC13                                                 | SCK2                                                                                                       |                                                                            | LCD_DA<br>TA7-A  | IRQ1      |             |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (8/8)**

| Pin Number<br>177-Pin TFLGA<br>176-Pin LFBGA | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB) | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC            | Interrupt | A/D<br>D/A |
|----------------------------------------------|-----------------------------------------|----------|-------------------------|-------------------------------------------------------------|------------------------------------------------------------|----------------------------------------------------------------------------|------------------|-----------|------------|
| R9                                           |                                         | P53*2    | BCLK                    |                                                             |                                                            |                                                                            |                  |           |            |
| R10                                          | VSS                                     |          |                         |                                                             |                                                            |                                                                            |                  |           |            |
| R11                                          | VCC                                     |          |                         |                                                             |                                                            |                                                                            |                  |           |            |
| R12                                          |                                         | P80      | EDREQ0                  | MTIOC3B/<br>PO26                                            | ET0_TX_EN/<br>RMII0_TXD_EN/<br>SCK10/RTS10#                | QIO2-A/SDHI_WP/<br>MMC_D2-A                                                | LCD_DA<br>TA14-A |           |            |
| R13                                          |                                         | P76      | CS6#                    | PO22                                                        | ET0_RX_CLK/<br>REF50CK0/<br>SMISO11/<br>SSCL11/RXD11       | QSSL-A/<br>SDHI_CMD-A/<br>SDSI_CMD-A/<br>MMC_CMD-A                         | LCD_DA<br>TA18-A |           |            |
| R14                                          |                                         | P74      | A20/CS4#                | PO19                                                        | ET0_ERXD1/<br>RMII0_RXD1/<br>SS11#/CTS11#                  |                                                                            | LCD_DA<br>TA21-A |           |            |
| R15                                          |                                         | PC1      | A17                     | MTIOC3A/<br>TCLKD/PO18                                      | ET0_ERXD2/<br>SCK5/SSLA2-A                                 |                                                                            | LCD_DA<br>TA22-A | IRQ12     |            |

Note 1. The 176-pin LFBGA does not include the E5 pin.

Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

## 1.6.2 176-Pin LFQFP

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (1/8)

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC)                 | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)           | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|-------------------------|-----------------------------------------------------------------------------|----------------------------------------------------------------------|----------------------------------------------------------------------------|-------|-----------|------------|
| 1          | AVSS0                                   |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 2          |                                         | P05      |                         |                                                                             |                                                                      |                                                                            |       | IRQ13     | DA1        |
| 3          | AVCC1                                   |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 4          |                                         | P03      |                         |                                                                             |                                                                      |                                                                            |       | IRQ11     | DA0        |
| 5          | AVSS1                                   |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 6          |                                         | P02      |                         | TMCI1                                                                       | SCK6                                                                 |                                                                            |       | IRQ10     | AN120      |
| 7          |                                         | P01      |                         | TMC10                                                                       | RXD6/SMISO6/<br>SSCL6                                                |                                                                            |       | IRQ9      | AN119      |
| 8          |                                         | P00      |                         | TMR10                                                                       | TXD6/SMOSI6/<br>SSDA6                                                |                                                                            |       | IRQ8      | AN118      |
| 9          |                                         | PF5      |                         |                                                                             |                                                                      |                                                                            |       | IRQ4      |            |
| 10         | EMLE                                    |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 11         |                                         | PJ5      |                         | POE8#                                                                       | CTS2#/RTS2#/<br>SS2#                                                 |                                                                            |       |           |            |
| 12         | VSS                                     |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 13         |                                         | PJ3      | EDACK1                  | MTIOC3C                                                                     | ET0_EXOUT/<br>CTS6#/RTS6#/<br>SS6#/CTS0#/<br>RTS0#/SS0#              |                                                                            |       |           |            |
| 14         | VCL                                     |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 15         | VBATT                                   |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 16         | NC                                      |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 17         | TRST#                                   | PF4      |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 18         | MD/FINED                                |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 19         | XCIN                                    |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 20         | XCOUT                                   |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 21         | RES#                                    |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 22         | XTAL                                    | P37      |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 23         | VSS                                     |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 24         | EXTAL                                   | P36      |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 25         | VCC                                     |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 26         | UPSEL                                   | P35      |                         |                                                                             |                                                                      |                                                                            |       | NMI       |            |
| 27         |                                         | P34      |                         | MTIOC0A/<br>TMCI3/PO12/<br>POE10#                                           | ET0_LINKSTA/<br>SCK6/SCK0                                            |                                                                            |       | IRQ4      |            |
| 28         |                                         | P33      | EDREQ1                  | MTIOC0D/<br>TIOC0D/<br>TMR13/PO11/<br>POE4#/<br>POE11#                      | RXD6/SMISO6/<br>SSCL6/RXD0/<br>SMISO0/SSCL0/<br>CRX0                 | PCKO                                                                       |       | IRQ3-DS   |            |
| 29         |                                         | P32      |                         | MTIOC0C/<br>TIOC0C/<br>TMO3/PO10/<br>RTCIC2/<br>RTCOUT/<br>POE0#/<br>POE10# | TXD6/SMOSI6/<br>SSDA6/TXD0/<br>SMOSI0/SSDA0/<br>CTX0/<br>USB0_VBUSEN | VSYNC                                                                      |       | IRQ2-DS   |            |
| 30         | TMS                                     | PF3      |                         |                                                                             |                                                                      |                                                                            |       |           |            |

**Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (2/8)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC)              | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)                                                 | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSI,<br>MMCIF, PDC) | GLCDC | Interrupt | A/D<br>D/A  |
|------------|-----------------------------------------|----------|-------------------------|--------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------|-------|-----------|-------------|
| 31         | TDI                                     | PF2      |                         |                                                                          | RXD1/SMISO1/<br>SSCL1                                                                                      |                                                                           |       |           |             |
| 32         |                                         | P31      |                         | MTIOC4D/<br>TMC12/PO9/<br>RTCIC1                                         | CTS1#/RTS1#/<br>SS1#/SSLB0-A                                                                               |                                                                           |       | IRQ1-DS   |             |
| 33         |                                         | P30      |                         | MTIOC4B/<br>TMRI3/PO8/<br>RTCIC0/<br>POE8#                               | RXD1/SMISO1/<br>SSCL1/MISOB-A                                                                              |                                                                           |       | IRQ0-DS   |             |
| 34         | TCK                                     | PF1      |                         |                                                                          | SCK1                                                                                                       |                                                                           |       |           |             |
| 35         | TDO                                     | PF0      |                         |                                                                          | TXD1/SMOSI1/<br>SSDA1                                                                                      |                                                                           |       |           |             |
| 36         |                                         | P27      | CS7#                    | MTIOC2B/<br>TMC13/PO7                                                    | SCK1/RSPCKB-<br>A                                                                                          |                                                                           |       |           |             |
| 37         |                                         | P26      | CS6#                    | MTIOC2A/<br>TMO1/PO6                                                     | TXD1/SMOSI1/<br>SSDA1/CTS3#/<br>RTS3#/SS3#/<br>MOSIB-A                                                     |                                                                           |       |           |             |
| 38         |                                         | P25      | CS5#/<br>EDACK1         | MTIOC4C/<br>MTCLKB/<br>TIOCA4/PO5                                        | RXD3/SMISO3/<br>SSCL3                                                                                      | SDHI_CD/HSYNC                                                             |       |           | ADTRG0<br># |
| 39         | VCC                                     |          |                         |                                                                          |                                                                                                            |                                                                           |       |           |             |
| 40         |                                         | P24      | CS4#/<br>EDREQ1         | MTIOC4A/<br>MTCLKA/<br>TIOCB4/<br>TMRI1/PO4                              | SCK3/<br>USB0_VBUSEN                                                                                       | SDHI_WP/PIXCLK                                                            |       |           |             |
| 41         | VSS                                     |          |                         |                                                                          |                                                                                                            |                                                                           |       |           |             |
| 42         |                                         | P23      | EDACK0                  | MTIOC3D/<br>MTCLKD/<br>TIOCD3/PO3                                        | TXD3/SMOSI3/<br>SSDA3/CTS0#/<br>RTS0#/SS0#                                                                 | SDHI_D1-C/PIXD7                                                           |       |           |             |
| 43         |                                         | P22      | EDREQ0                  | MTIOC3B/<br>MTCLKC/<br>TIOCC3/<br>TMO0/PO2                               | SCK0/<br>USB0_OVRCUR<br>B                                                                                  | SDHI_D0-C/PIXD6                                                           |       |           |             |
| 44         |                                         | P21      |                         | MTIOC1B/<br>MTIOC4A/<br>TIOCA3/<br>TMC10/PO1                             | RXD0/SMISO0/<br>SSCL0/SCL1/<br>USB0_EXICEN                                                                 | SDHI_CLK-C/<br>PIXD5                                                      |       | IRQ9      |             |
| 45         |                                         | P20      |                         | MTIOC1A/<br>TIOCB3/<br>TMRI0/PO0                                         | TXD0/SMOSI0/<br>SSDA0/SDA1/<br>USB0_ID                                                                     | SDHI_CMD-C/<br>PIXD4                                                      |       | IRQ8      |             |
| 46         |                                         | P17      |                         | MTIOC3A/<br>MTIOC3B/<br>MTIOC4B/<br>TIOCB0/<br>TCLKD/TMO1/<br>PO15/POE8# | SCK1/TXD3/<br>SMOSI3/SSDA3/<br>SDA2-DS                                                                     | SDHI_D3-C/PIXD3                                                           |       | IRQ7      | ADTRG1<br># |
| 47         |                                         | P87      |                         | MTIOC4C/<br>TIOCA2                                                       | SMOSI10/<br>SSDA10/TXD10                                                                                   | SDHI_D2-C/PIXD2                                                           |       |           |             |
| 48         |                                         | P16      |                         | MTIOC3C/<br>MTIOC3D/<br>TIOCB1/<br>TCLKC/TMO2/<br>PO14/RTCOU             | TXD1/SMOSI1/<br>SSDA1/RXD3/<br>SMISO3/SSCL3/<br>SCL2-DS/<br>USB0_VBUSEN/<br>USB0_VBUS/<br>USB0_OVRCUR<br>B |                                                                           |       | IRQ6      | ADTRG0<br># |
| 49         |                                         | P86      |                         | MTIOC4D/<br>TIOCA0                                                       | SMISO10/<br>SSCL10/RXD10                                                                                   | PIXD1                                                                     |       |           |             |

**Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (3/8)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC        | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB) | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC           | Interrupt | A/D<br>D/A  |
|------------|-----------------------------------------|----------|--------------------------------|-------------------------------------------------------------|------------------------------------------------------------|----------------------------------------------------------------------------|-----------------|-----------|-------------|
| 50         |                                         | P15      |                                | MTIOC0B/<br>MTCLKB/<br>TIOCB2/<br>TCLKB/TMC12/<br>PO13      | RXD1/SMISO1/<br>SSCL1/SCK3/<br>CRX1-DS                     | PIXD0                                                                      |                 | IRQ5      |             |
| 51         |                                         | P14      |                                | MTIOC3A/<br>MTCLKA/<br>TIOCB5/<br>TCLKA/TMRI2/<br>PO15      | CTS1#/RTS1#/<br>SS1#/CTX1/<br>USB0_OVRCUR<br>A             |                                                                            | LCD_CL<br>K-A   | IRQ4      |             |
| 52         |                                         | P13      | WR2#/BC2#                      | MTIOC0B/<br>TIOCA5/TMO3/<br>PO13                            | TXD2/SMOSI2/<br>SSDA2/<br>SDA0[FM+]                        |                                                                            | LCD_TC<br>ON0-A | IRQ3      | ADTRG1<br># |
| 53         |                                         | P12      | WR3#/<br>BC3#                  | MTIC5U/<br>TMC11                                            | RXD2/SMISO2/<br>SSCL2/<br>SCL0[FM+]                        |                                                                            | LCD_TC<br>ON1-A | IRQ2      |             |
| 54         | VCC_USB                                 |          |                                |                                                             |                                                            |                                                                            |                 |           |             |
| 55         |                                         |          |                                |                                                             | USB0_DM                                                    |                                                                            |                 |           |             |
| 56         |                                         |          |                                |                                                             | USB0_DP                                                    |                                                                            |                 |           |             |
| 57         | VSS_USB                                 |          |                                |                                                             |                                                            |                                                                            |                 |           |             |
| 58         |                                         | PJ2      |                                |                                                             | TXD8/SMOSI8/<br>SSDA8/SSLC3-B                              |                                                                            | LCD_TC<br>ON2-A |           |             |
| 59         |                                         | PJ1      |                                | MTIOC6A                                                     | RXD8/SMISO8/<br>SSCL8/SSLC2-B                              |                                                                            | LCD_TC<br>ON3-A |           |             |
| 60         |                                         | PJ0      |                                | MTIOC6B                                                     | SCK8/SSLC1-B                                               |                                                                            | LCD_DA<br>TA0-A |           |             |
| 61         |                                         | P85      |                                | MTIOC6C/<br>TIOCC0                                          |                                                            |                                                                            | LCD_DA<br>TA1-A |           |             |
| 62         |                                         | P84      |                                | MTIOC6D                                                     |                                                            |                                                                            | LCD_DA<br>TA2-A |           |             |
| 63         |                                         | P57      |                                |                                                             | RXD7/SMISO7/<br>SSCL7/SSLC0-B                              |                                                                            | LCD_DA<br>TA3-A |           |             |
| 64         |                                         | P56      | EDACK1                         | MTIOC3C/<br>TIOCA1                                          | SCK7/RSPCKC-<br>B                                          |                                                                            | LCD_DA<br>TA4-A |           |             |
| 65         |                                         | P55      | D0[A0/D0]/<br>EDREQ0/<br>WAIT# | MTIOC4D/<br>TMO3                                            | ET0_EXOUT/<br>TXD7/SMOSI7/<br>SSDA7/MISOC-<br>B/CRX1       |                                                                            | LCD_DA<br>TA5-A | IRQ10     |             |
| 66         |                                         | P54      | D1[A1/D1]/<br>EDACK0/<br>ALE   | MTIOC4B/<br>TMC11                                           | ET0_LINKSTA/<br>CTS2#/RTS2#/<br>SS2#/MOSIC-B/<br>CTX1      |                                                                            | LCD_DA<br>TA6-A |           |             |
| 67         |                                         | P11      |                                | MTIC5V/TMC13                                                | SCK2                                                       |                                                                            | LCD_DA<br>TA7-A | IRQ1      |             |
| 68         |                                         | P10      | ALE                            | MTIC5W/<br>TMRI3                                            |                                                            |                                                                            |                 | IRQ0      |             |
| 69         |                                         | P53*1    | BCLK                           |                                                             |                                                            |                                                                            |                 |           |             |
| 70         |                                         | P52      | RD#                            |                                                             | RXD2/SMISO2/<br>SSCL2/SSLB3-A                              |                                                                            |                 |           |             |
| 71         |                                         | P51      | WR1#/<br>BC1#/<br>WAIT#        |                                                             | SCK2/SSLB2-A                                               |                                                                            |                 |           |             |

**Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (4/8)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC          | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)                   | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC            | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|----------------------------------|-------------------------------------------------------------|------------------------------------------------------------------------------|----------------------------------------------------------------------------|------------------|-----------|------------|
| 72         |                                         | P50      | WR0#/WR#                         |                                                             | TXD2/SMOSI2/<br>SSDA2/SSLB1-A                                                |                                                                            |                  |           |            |
| 73         | VSS                                     |          |                                  |                                                             |                                                                              |                                                                            |                  |           |            |
| 74         |                                         | P83      | EDACK1                           | MTIOC4C                                                     | ET0_CRS/<br>RMII0_CRS_DV/<br>SCK10/SS10#/<br>CTS10#                          |                                                                            | LCD_DA<br>TA8-A  |           |            |
| 75         | VCC                                     |          |                                  |                                                             |                                                                              |                                                                            |                  |           |            |
| 76         | UB                                      | PC7      | A23/CS0#                         | MTIOC3A/<br>MTCLKB/<br>TMO2/PO31/<br>TOC0/<br>CACREF        | ET0_COL/TXD8/<br>SMOSI8/SSDA8/<br>SMOSI10/<br>SSDA10/TXD10/<br>MISOA-A       | MMC_D7-A                                                                   | LCD_DA<br>TA9-A  | IRQ14     |            |
| 77         |                                         | PC6      | D2[A2/D2]/<br>A22/CS1#           | MTIOC3C/<br>MTCLKA/<br>TMC12/PO30/<br>TIC0                  | ET0_ETXD3/<br>RXD8/SMISO8/<br>SSCL8/<br>SMISO10/<br>SSCL10/RXD10/<br>MOSIA-A | MMC_D6-A                                                                   | LCD_DA<br>TA10-A | IRQ13     |            |
| 78         |                                         | PC5      | D3[A3/D3]/<br>A21/CS2#/<br>WAIT# | MTIOC3B/<br>MTCLKD/<br>TMRI2/PO29                           | ET0_ETXD2/<br>SCK8/SCK10/<br>RSPCKA-A                                        | MMC_D5-A                                                                   | LCD_DA<br>TA11-A |           |            |
| 79         |                                         | P82      | EDREQ1                           | MTIOC4A/<br>PO28                                            | ET0_ETXD1/<br>RMII0_TXD1/<br>SMOSI10/<br>SSDA10/TXD10                        | MMC_D4-A                                                                   | LCD_DA<br>TA12-A |           |            |
| 80         |                                         | P81      | EDACK0                           | MTIOC3D/<br>PO27                                            | ET0_ETXD0/<br>RMII0_TXD0/<br>SMISO10/<br>SSCL10/RXD10                        | QIO3-A/SDHI_CD/<br>MMC_D3-A                                                | LCD_DA<br>TA13-A |           |            |
| 81         |                                         | P80      | EDREQ0                           | MTIOC3B/<br>PO26                                            | ET0_TX_EN/<br>RMII0_TXD_EN/<br>SCK10/RTS10#                                  | QIO2-A/SDHI_WP/<br>MMC_D2-A                                                | LCD_DA<br>TA14-A |           |            |
| 82         |                                         | PC4      | A20/CS3#                         | MTIOC3D/<br>MTCLKC/<br>TMC11/PO25/<br>POE0#                 | ET0_TX_CLK/<br>SCK5/CTS8#/<br>RTS8#/SS8#/<br>SS10#/CTS10#/<br>RTS10#/SSLA0-A | QMI-A/QIO1-A/<br>SDHI_D1-A/<br>SDSI_D1-A/<br>MMC_D1-A                      | LCD_DA<br>TA15-A |           |            |
| 83         |                                         | PC3      | A19                              | MTIOC4D/<br>TCLKB/PO24                                      | ET0_TX_ER/<br>TXD5/SMOSI5/<br>SSDA5                                          | QMO-A/QIO0-A/<br>SDHI_D0-A/<br>SDSI_D0-A/<br>MMC_D0-A                      | LCD_DA<br>TA16-A |           |            |
| 84         |                                         | P77      | CS7#                             | PO23                                                        | ET0_RX_ER/<br>RMII0_RX_ER/<br>SMOSI11/<br>SSDA11/TXD11                       | QSPCLK-A/<br>SDHI_CLK-A/<br>SDSI_CLK-A/<br>MMC_CLK-A                       | LCD_DA<br>TA17-A |           |            |
| 85         |                                         | P76      | CS6#                             | PO22                                                        | ET0_RX_CLK/<br>REF50CK0/<br>SMISO11/<br>SSCL11/RXD11                         | QSSL-A/<br>SDHI_CMD-A/<br>SDSI_CMD-A/<br>MMC_CMD-A                         | LCD_DA<br>TA18-A |           |            |
| 86         |                                         | PC2      | A18                              | MTIOC4B/<br>TCLKA/PO21                                      | ET0_RX_DV/<br>RXD5/SMISO5/<br>SSCL5/SSLA3-A                                  | SDHI_D3-A/<br>SDSI_D3-A/<br>MMC_CD-A                                       | LCD_DA<br>TA19-A |           |            |
| 87         |                                         | P75      | CS5#                             | PO20                                                        | ET0_ERXD0/<br>RMII0_RXD0/<br>SCK11/RTS11#                                    | SDHI_D2-A/<br>SDSI_D2-A/<br>MMC_RES#-A                                     | LCD_DA<br>TA20-A |           |            |
| 88         |                                         | P74      | A20/CS4#                         | PO19                                                        | ET0_ERXD1/<br>RMII0_RXD1/<br>SS11#/CTS11#                                    |                                                                            | LCD_DA<br>TA21-A |           |            |
| 89         |                                         | PC1      | A17                              | MTIOC3A/<br>TCLKD/PO18                                      | ET0_ERXD2/<br>SCK5/SSLA2-A                                                   |                                                                            | LCD_DA<br>TA22-A | IRQ12     |            |
| 90         | VCC                                     |          |                                  |                                                             |                                                                              |                                                                            |                  |           |            |

**Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (5/8)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC)   | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)                      | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC            | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|-------------------------|---------------------------------------------------------------|---------------------------------------------------------------------------------|----------------------------------------------------------------------------|------------------|-----------|------------|
| 91         |                                         | PC0      | A16                     | MTIOC3C/<br>TCLKC/PO17                                        | ET0_ERXD3/<br>CTS5#/RTS5#/<br>SS5#/SSLA1-A                                      |                                                                            |                  | IRQ14     |            |
| 92         | VSS                                     |          |                         |                                                               |                                                                                 |                                                                            |                  |           |            |
| 93         |                                         | P73      | CS3#                    | PO16                                                          | ET0_WOL                                                                         |                                                                            | LCD_EX<br>TCLK-A |           |            |
| 94         |                                         | PB7      | A15                     | MTIOC3B/<br>TIOCB5/PO31                                       | ET0_CRS/<br>RMII0_CRS_DV/<br>TXD9/SMOSI9/<br>SSDA9/<br>SMOSI11/<br>SSDA11/TXD11 | SDSI_D1-B                                                                  |                  |           |            |
| 95         |                                         | PB6      | A14                     | MTIOC3D/<br>TIOCA5/PO30                                       | ET0_ETXD1/<br>RMII0_TXD1/<br>RXD9/SMISO9/<br>SSCL9/<br>SMISO11/<br>SSCL11/RXD11 | SDSI_D0-B                                                                  |                  |           |            |
| 96         |                                         | PB5      | A13                     | MTIOC2A/<br>MTIOC1B/<br>TIOCB4/<br>TMRI1/PO29/<br>POE4#       | ET0_ETXD0/<br>RMII0_TXD0/<br>SCK9/SCK11                                         | SDSI_CLK-B                                                                 | LCD_CL<br>K-B    |           |            |
| 97         |                                         | PB4      | A12                     | TIOCA4/PO28                                                   | ET0_TX_EN/<br>RMII0_TXD_EN/<br>CTS9#/RTS9#/<br>SS9#/SS11#/<br>CTS11#/RTS11#     | SDSI_CMD-B                                                                 | LCD_TC<br>ON0-B  |           |            |
| 98         |                                         | PB3      | A11                     | MTIOC0A/<br>MTIOC4A/<br>TIOC3D/<br>TCLKD/TMO0/<br>PO27/POE11# | ET0_RX_ER/<br>RMII0_RX_ER/<br>SCK4/SCK6                                         | SDSI_D3-B                                                                  | LCD_TC<br>ON1-B  |           |            |
| 99         |                                         | PB2      | A10                     | TIOCC3/<br>TCLKC/PO26                                         | ET0_RX_CLK/<br>REF50CK0/<br>CTS4#/RTS4#/<br>SS4#/CTS6#/<br>RTS6#/SS6#           | SDSI_D2-B                                                                  | LCD_TC<br>ON2-B  |           |            |
| 100        |                                         | PB1      | A9                      | MTIOC0C/<br>MTIOC4C/<br>TIOCB3/<br>TMCI0/PO25                 | ET0_ERXD0/<br>RMII0_RXD0/<br>TXD4/SMOSI4/<br>SSDA4/TXD6/<br>SMOSI6/SSDA6        |                                                                            | LCD_TC<br>ON3-B  | IRQ4-DS   |            |
| 101        |                                         | P72      | A19/CS2#                |                                                               | ET0_MDC                                                                         |                                                                            | LCD_DA<br>TA23-A |           |            |
| 102        |                                         | P71      | A18/CS1#                |                                                               | ET0_MDIO                                                                        |                                                                            |                  |           |            |
| 103        | VCC                                     |          |                         |                                                               |                                                                                 |                                                                            |                  |           |            |
| 104        |                                         | PB0      | A8                      | MTIC5W/<br>TIOCA3/PO24                                        | ET0_ERXD1/<br>RMII0_RXD1/<br>RXD4/SMISO4/<br>SSCL4/RXD6/<br>SMISO6/SSCL6        |                                                                            | LCD_DA<br>TA0-B  | IRQ12     |            |
| 105        | VSS                                     |          |                         |                                                               |                                                                                 |                                                                            |                  |           |            |
| 106        |                                         | PA7      | A7                      | TIOCB2/PO23                                                   | ET0_WOL/<br>MISOA-B                                                             |                                                                            | LCD_DA<br>TA1-B  |           |            |
| 107        |                                         | PA6      | A6                      | MTIC5V/<br>MTCLKB/<br>TIOCA2/<br>TMCI3/PO22/<br>POE10#        | ET0_EXOUT/<br>CTS5#/RTS5#/<br>SS5#/MOSIA-B                                      |                                                                            | LCD_DA<br>TA2-B  |           |            |

**Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (6/8)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC        | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB) | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSI,<br>MMCIF, PDC) | GLCDC            | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|--------------------------------|-------------------------------------------------------------|------------------------------------------------------------|---------------------------------------------------------------------------|------------------|-----------|------------|
| 108        |                                         | PA5      | A5                             | MTIOC6B/<br>TIOCB1/PO21                                     | ET0_LINKSTA/<br>RSPCKA-B                                   |                                                                           | LCD_DA<br>TA3-B  |           |            |
| 109        |                                         | PA4      | A4                             | MTIC5U/<br>MTCLKA/<br>TIOCA1/<br>TMRI0/PO20                 | ET0_MDC/TXD5/<br>SMOSI5/SSDA5/<br>SSLA0-B                  |                                                                           | LCD_DA<br>TA4-B  | IRQ5-DS   |            |
| 110        |                                         | PA3      | A3                             | MTIOC0D/<br>MTCLKD/<br>TIOC0D/<br>TCLKB/PO19                | ET0_MDIO/<br>RXD5/SMISO5/<br>SSCL5                         |                                                                           | LCD_DA<br>TA5-B  | IRQ6-DS   |            |
| 111        | TRDATA3                                 | PG7      | D31                            |                                                             |                                                            |                                                                           |                  |           |            |
| 112        |                                         | PA2      | A2                             | MTIOC7A/<br>PO18                                            | RXD5/SMISO5/<br>SSCL5/SSLA3-B                              |                                                                           | LCD_DA<br>TA6-B  |           |            |
| 113        | TRDATA2                                 | PG6      | D30                            |                                                             |                                                            |                                                                           |                  |           |            |
| 114        |                                         | PA1      | DQM3/A1                        | MTIOC0B/<br>MTCLKC/<br>MTIOC7B/<br>TIOCB0/PO17              | ET0_WOL/<br>SCK5/SSLA2-B                                   |                                                                           | LCD_DA<br>TA7-B  | IRQ11     |            |
| 115        | VCC                                     |          |                                |                                                             |                                                            |                                                                           |                  |           |            |
| 116        | TRCLK                                   | PG5      | D29                            |                                                             |                                                            |                                                                           |                  |           |            |
| 117        | VSS                                     |          |                                |                                                             |                                                            |                                                                           |                  |           |            |
| 118        |                                         | PA0      | DQM2/<br>BC0#/A0               | MTIOC4A/<br>MTIOC6D/<br>TIOCA0/PO16/<br>CACREF              | ET0_TX_EN/<br>RMII0_TXD_EN/<br>SSLA1-B                     |                                                                           | LCD_DA<br>TA8-B  |           |            |
| 119        | TRSYNC                                  | PG4      | D28                            |                                                             |                                                            |                                                                           |                  |           |            |
| 120        |                                         | P67      | DQM1/CS7#                      | MTIOC7C                                                     |                                                            |                                                                           |                  | IRQ15     |            |
| 121        | TRDATA1                                 | PG3      | D27                            |                                                             |                                                            |                                                                           |                  |           |            |
| 122        |                                         | P66      | DQM0/CS6#                      | MTIOC7D                                                     |                                                            |                                                                           |                  |           |            |
| 123        | TRDATA0                                 | PG2      | D26                            |                                                             |                                                            |                                                                           |                  |           |            |
| 124        |                                         | P65      | CKE/CS5#                       |                                                             |                                                            |                                                                           |                  |           |            |
| 125        |                                         | PE7      | D15[A15/<br>D15]/D7[A7/<br>D7] | MTIOC6A/<br>TOC1                                            | MISOB-B                                                    | SDHI_WP/<br>MMC_RES#-B                                                    | LCD_DA<br>TA9-B  | IRQ7      | AN105      |
| 126        |                                         | PE6      | D14[A14/<br>D14]/D6[A6/<br>D6] | MTIOC6C/TIC1                                                | MOSIB-B                                                    | SDHI_CD/<br>MMC_CD-B                                                      | LCD_DA<br>TA10-B | IRQ6      | AN104      |
| 127        | VCC                                     |          |                                |                                                             |                                                            |                                                                           |                  |           |            |
| 128        |                                         | P70      | SDCLK                          |                                                             |                                                            |                                                                           |                  |           |            |
| 129        | VSS                                     |          |                                |                                                             |                                                            |                                                                           |                  |           |            |
| 130        |                                         | PE5      | D13[A13/<br>D13]/D5[A5/<br>D5] | MTIOC4C/<br>MTIOC2B                                         | ET0_RX_CLK/<br>REF50CK0/<br>RSPCKB-B                       |                                                                           | LCD_DA<br>TA11-B | IRQ5      | AN103      |
| 131        |                                         | PE4      | D12[A12/<br>D12]/D4[A4/<br>D4] | MTIOC4D/<br>MTIOC1A/<br>PO28                                | ET0_ERXD2/<br>SSLB0-B                                      |                                                                           | LCD_DA<br>TA12-B |           | AN102      |
| 132        |                                         | PE3      | D11[A11/<br>D11]/D3[A3/<br>D3] | MTIOC4B/<br>PO26/TOC3/<br>POE8#                             | ET0_ERXD3/<br>CTS12#/<br>RTS12#SS12#                       | MMC_D7-B                                                                  | LCD_DA<br>TA13-B |           | AN101      |
| 133        |                                         | PE2      | D10[A10/<br>D10]/D2[A2/<br>D2] | MTIOC4A/<br>PO23/TIC3                                       | RXD12/<br>SMISO12/<br>SSCL12/<br>RXDX12/SSLB3-<br>B        | MMC_D6-B                                                                  | LCD_DA<br>TA14-B | IRQ7-DS   | AN100      |

**Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (7/8)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC      | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)     | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC            | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|------------------------------|-------------------------------------------------------------|----------------------------------------------------------------|----------------------------------------------------------------------------|------------------|-----------|------------|
| 134        |                                         | PE1      | D9[A9/D9]/<br>D1[A1/D1]      | MTIOC4C/<br>MTIOC3B/<br>PO18                                | TXD12/<br>SMOSI12/<br>SSDA12/<br>TXDX12/<br>SIOX12/SSLB2-<br>B | MMC_D5-B                                                                   | LCD_DA<br>TA15-B |           | ANEX1      |
| 135        |                                         | PE0      | D8[A8/D8]/<br>D0[A0/D0]      | MTIOC3D                                                     | SCK12/SSLB1-B                                                  | MMC_D4-B                                                                   | LCD_DA<br>TA16-B |           | ANEX0      |
| 136        |                                         | P64      | WE#/D3[A3/<br>D3]/CS4#       |                                                             |                                                                |                                                                            |                  |           |            |
| 137        |                                         | P63      | CAS#/<br>D2[A2/D2]/<br>CS3#  |                                                             |                                                                |                                                                            |                  |           |            |
| 138        |                                         | P62      | RAS#/<br>D1[A1/D1]/<br>CS2#  |                                                             |                                                                |                                                                            |                  |           |            |
| 139        |                                         | P61      | SDCS#/<br>D0[A0/D0]/<br>CS1# |                                                             |                                                                |                                                                            |                  |           |            |
| 140        | VSS                                     |          |                              |                                                             |                                                                |                                                                            |                  |           |            |
| 141        |                                         | P60      | CS0#                         |                                                             |                                                                |                                                                            |                  |           |            |
| 142        | VCC                                     |          |                              |                                                             |                                                                |                                                                            |                  |           |            |
| 143        |                                         | PD7      | D7[A7/D7]                    | MTIC5U/<br>POE0#                                            | SSLC3-A                                                        | QMI-B/QIO1-B/<br>SDHI_D1-B/<br>MMC_D1-B                                    | LCD_DA<br>TA17-B | IRQ7      | AN107      |
| 144        | TRDATA7                                 | PG1      | D25                          |                                                             |                                                                |                                                                            |                  |           |            |
| 145        |                                         | PD6      | D6[A6/D6]                    | MTIC5V/<br>MTIOC8A/<br>POE4#                                | SSLC2-A                                                        | QMO-B/QIO0-B/<br>SDHI_D0-B/<br>MMC_D0-B                                    | LCD_DA<br>TA18-B | IRQ6      | AN106      |
| 146        | TRDATA6                                 | PG0      | D24                          |                                                             |                                                                |                                                                            |                  |           |            |
| 147        |                                         | PD5      | D5[A5/D5]                    | MTIC5W/<br>MTIOC8C/<br>POE10#                               | SSLC1-A                                                        | QSPCLK-B/<br>SDHI_CLK-B/<br>MMC_CLK-B                                      | LCD_DA<br>TA19-B | IRQ5      | AN113      |
| 148        |                                         | PD4      | D4[A4/D4]                    | MTIOC8B/<br>POE11#                                          | SSLC0-A                                                        | QSSL-B/<br>SDHI_CMD-B/<br>MMC_CMD-B                                        | LCD_DA<br>TA20-B | IRQ4      | AN112      |
| 149        | TRSYNC1                                 | P97      | D23/A23                      |                                                             |                                                                |                                                                            |                  |           |            |
| 150        |                                         | PD3      | D3[A3/D3]                    | MTIOC8D/<br>TOC2/POE8#                                      | RSPCKC-A                                                       | QIO3-B/SDHI_D3-<br>B/MMC_D3-B                                              | LCD_DA<br>TA21-B | IRQ3      | AN111      |
| 151        | VSS                                     |          |                              |                                                             |                                                                |                                                                            |                  |           |            |
| 152        | TRDATA5                                 | P96      | D22/A22                      |                                                             |                                                                |                                                                            |                  |           |            |
| 153        | VCC                                     |          |                              |                                                             |                                                                |                                                                            |                  |           |            |
| 154        |                                         | PD2      | D2[A2/D2]                    | MTIOC4D/TIC2                                                | MISOC-A/CRX0                                                   | QIO2-B/SDHI_D2-<br>B/MMC_D2-B                                              | LCD_DA<br>TA22-B | IRQ2      | AN110      |
| 155        | TRDATA4                                 | P95      | D21/A21                      |                                                             |                                                                |                                                                            |                  |           |            |
| 156        |                                         | PD1      | D1[A1/D1]                    | MTIOC4B/<br>POE0#                                           | MOSIC-A/CTX0                                                   |                                                                            | LCD_DA<br>TA23-B | IRQ1      | AN109      |
| 157        |                                         | P94      | D20/A20                      |                                                             |                                                                |                                                                            |                  |           |            |
| 158        |                                         | PD0      | D0[A0/D0]                    | POE4#                                                       |                                                                |                                                                            | LCD_EX<br>TCLK-B | IRQ0      | AN108      |
| 159        |                                         | P93      | D19/A19                      | POE0#                                                       | CTS7#/RTS7#/<br>SS7#                                           |                                                                            |                  |           | AN117      |

**Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (8/8)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB) | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC | Interrupt    | A/D<br>D/A  |
|------------|-----------------------------------------|----------|-------------------------|-------------------------------------------------------------|------------------------------------------------------------|----------------------------------------------------------------------------|-------|--------------|-------------|
| 160        |                                         | P92      | D18/A18                 | POE4#                                                       | RXD7/SMISO7/<br>SSCL7                                      |                                                                            |       |              | AN116       |
| 161        |                                         | P91      | D17/A17                 |                                                             | SCK7                                                       |                                                                            |       |              | AN115       |
| 162        | VSS                                     |          |                         |                                                             |                                                            |                                                                            |       |              |             |
| 163        |                                         | P90      | D16/A16                 |                                                             | TXD7/SMOSI7/<br>SSDA7                                      |                                                                            |       |              | AN114       |
| 164        | VCC                                     |          |                         |                                                             |                                                            |                                                                            |       |              |             |
| 165        |                                         | P47      |                         |                                                             |                                                            |                                                                            |       | IRQ15-<br>DS | AN007       |
| 166        |                                         | P46      |                         |                                                             |                                                            |                                                                            |       | IRQ14-<br>DS | AN006       |
| 167        |                                         | P45      |                         |                                                             |                                                            |                                                                            |       | IRQ13-<br>DS | AN005       |
| 168        |                                         | P44      |                         |                                                             |                                                            |                                                                            |       | IRQ12-<br>DS | AN004       |
| 169        |                                         | P43      |                         |                                                             |                                                            |                                                                            |       | IRQ11-<br>DS | AN003       |
| 170        |                                         | P42      |                         |                                                             |                                                            |                                                                            |       | IRQ10-<br>DS | AN002       |
| 171        |                                         | P41      |                         |                                                             |                                                            |                                                                            |       | IRQ9-DS      | AN001       |
| 172        | VREFL0                                  |          |                         |                                                             |                                                            |                                                                            |       |              |             |
| 173        |                                         | P40      |                         |                                                             |                                                            |                                                                            |       | IRQ8-DS      | AN000       |
| 174        | VREFH0                                  |          |                         |                                                             |                                                            |                                                                            |       |              |             |
| 175        | AVCC0                                   |          |                         |                                                             |                                                            |                                                                            |       |              |             |
| 176        |                                         | P07      |                         |                                                             |                                                            |                                                                            |       | IRQ15        | ADTRG0<br># |

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

## 1.6.3 145-Pin TFLGA

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (1/7)

| Pin Number    |                                   |          |                          | Timer                                     | Communication                              | Memory Interface                                 |                 |           |          |
|---------------|-----------------------------------|----------|--------------------------|-------------------------------------------|--------------------------------------------|--------------------------------------------------|-----------------|-----------|----------|
| 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC        | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (ETHERC, SCI, RSPI, RIIC, CAN, USB)        | Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC) | GLCDC           | Interrupt | A/D D/A  |
| A1            | AVSS0                             |          |                          |                                           |                                            |                                                  |                 |           |          |
| A2            |                                   | P07      |                          |                                           |                                            |                                                  |                 | IRQ15     | ADTRG0 # |
| A3            |                                   | P40      |                          |                                           |                                            |                                                  |                 | IRQ8-DS   | AN000    |
| A4            |                                   | P42      |                          |                                           |                                            |                                                  |                 | IRQ10-DS  | AN002    |
| A5            |                                   | P45      |                          |                                           |                                            |                                                  |                 | IRQ13-DS  | AN005    |
| A6            |                                   | P90      | A16                      |                                           | TXD7/SMOSI7/SSDA7                          |                                                  |                 |           | AN114    |
| A7            |                                   | P92      | A18                      | POE4#                                     | RXD7/SMISO7/SSCL7                          |                                                  |                 |           | AN116    |
| A8            |                                   | PD2      | D2[A2/D2]                | MTIOC4D/TIC2                              | MISOC-A/CRX0                               | QIO2-B/SDHI_D2-B/MMC_D2-B                        | LCD_DA TA22-B*1 | IRQ2      | AN110    |
| A9            |                                   | PD6      | D6[A6/D6]                | MTIC5V/MTIOC8A/POE4#                      | SSLC2-A                                    | QMO-B/QIO0-B/SDHI_D0-B/MMC_D0-B                  | LCD_DA TA18-B*1 | IRQ6      | AN106    |
| A10           | VSS                               |          |                          |                                           |                                            |                                                  |                 |           |          |
| A11           |                                   | P62      | RAS#/D1[A1/D1]*1/CS2#    |                                           |                                            |                                                  |                 |           |          |
| A12           |                                   | PE1      | D9[A9/D9]/D1[A1/D1]*1    | MTIOC4C/MTIOC3B/PO18                      | TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B | MMC_D5-B                                         | LCD_DA TA15-B*1 |           | ANEX1    |
| A13           |                                   | PE3      | D11[A11/D11]/D3[A3/D3]*1 | MTIOC4B/PO26/TOC3/POE8#                   | ET0_ERXD3/CTS12#/RTS12#/SS12#              | MMC_D7-B                                         | LCD_DA TA13-B*1 |           | AN101    |
| B1            | AVCC1                             |          |                          |                                           |                                            |                                                  |                 |           |          |
| B2            | AVCC0                             |          |                          |                                           |                                            |                                                  |                 |           |          |
| B3            |                                   | P05      |                          |                                           |                                            |                                                  |                 | IRQ13     | DA1      |
| B4            | VREFL0                            |          |                          |                                           |                                            |                                                  |                 |           |          |
| B5            |                                   | P43      |                          |                                           |                                            |                                                  |                 | IRQ11-DS  | AN003    |
| B6            |                                   | P47      |                          |                                           |                                            |                                                  |                 | IRQ15-DS  | AN007    |
| B7            |                                   | P91      | A17                      |                                           | SCK7                                       |                                                  |                 |           | AN115    |
| B8            |                                   | PD0      | D0[A0/D0]                | POE4#                                     |                                            |                                                  | LCD_EX TCLK-B*1 | IRQ0      | AN108    |
| B9            |                                   | PD4      | D4[A4/D4]                | MTIOC8B/POE11#                            | SSLC0-A                                    | QSSL-B/SDHI_CMD-B/MMC_CMD-B                      | LCD_DA TA20-B*1 | IRQ4      | AN112    |
| B10           | VCC                               |          |                          |                                           |                                            |                                                  |                 |           |          |
| B11           |                                   | P61      | SDCS#/D0[A0/D0]*1/CS1#   |                                           |                                            |                                                  |                 |           |          |
| B12           |                                   | PE2      | D10[A10/D10]/D2[A2/D2]*1 | MTIOC4A/PO23/TIC3                         | RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B        | MMC_D6-B                                         | LCD_DA TA14-B*1 | IRQ7-DS   | AN100    |

**Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (2/7)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC          | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB) | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC              | Interrupt    | A/D<br>D/A |
|------------|-----------------------------------------|----------|----------------------------------|-------------------------------------------------------------|------------------------------------------------------------|----------------------------------------------------------------------------|--------------------|--------------|------------|
| B13        |                                         | PE4      | D12[A12/<br>D12]/D4[A4/<br>D4]*1 | MTIOC4D/<br>MTIOC1A/<br>PO28                                | ET0_ERXD2/<br>SSLB0-B                                      |                                                                            | LCD_DA<br>TA12-B*1 |              | AN102      |
| C1         | AVSS1                                   |          |                                  |                                                             |                                                            |                                                                            |                    |              |            |
| C2         |                                         | P02      |                                  | TMCI1                                                       | SCK6                                                       |                                                                            |                    | IRQ10        | AN120      |
| C3         | VREFH0                                  |          |                                  |                                                             |                                                            |                                                                            |                    |              |            |
| C4         |                                         | P41      |                                  |                                                             |                                                            |                                                                            |                    | IRQ9-DS      | AN001      |
| C5         |                                         | P46      |                                  |                                                             |                                                            |                                                                            |                    | IRQ14-<br>DS | AN006      |
| C6         | VSS                                     |          |                                  |                                                             |                                                            |                                                                            |                    |              |            |
| C7         |                                         | PD1      | D1[A1/D1]                        | MTIOC4B/<br>POE0#                                           | MOSIC-A/CTX0                                               |                                                                            | LCD_DA<br>TA23-B*1 | IRQ1         | AN109      |
| C8         |                                         | PD3      | D3[A3/D3]                        | MTIOC8D/<br>TOC2/POE8#                                      | RSPCKC-A                                                   | QIO3-B/SDHI_D3-<br>B/MMC_D3-B                                              | LCD_DA<br>TA21-B*1 | IRQ3         | AN111      |
| C9         |                                         | PD7      | D7[A7/D7]                        | MTIC5U/<br>POE0#                                            | SSLC3-A                                                    | QMI-B/QIO1-B/<br>SDHI_D1-B/<br>MMC_D1-B                                    | LCD_DA<br>TA17-B*1 | IRQ7         | AN107      |
| C10        |                                         | P63      | CAS#/<br>D2[A2/D2]*1/<br>CS3#    |                                                             |                                                            |                                                                            |                    |              |            |
| C11        |                                         | PE0      | D8[A8/D8]/<br>D0[A0/D0]*1        | MTIOC3D                                                     | SCK12/SSLB1-B                                              | MMC_D4-B                                                                   | LCD_DA<br>TA16-B*1 |              | ANEX0      |
| C12        |                                         | P70      | SDCLK                            |                                                             |                                                            |                                                                            |                    |              |            |
| C13        | VSS                                     |          |                                  |                                                             |                                                            |                                                                            |                    |              |            |
| D1         |                                         | P00      |                                  | TMRI0                                                       | TXD6/SMOSI6/<br>SSDA6                                      |                                                                            |                    | IRQ8         | AN118      |
| D2         |                                         | PF5      |                                  |                                                             |                                                            |                                                                            |                    | IRQ4         |            |
| D3         |                                         | P03      |                                  |                                                             |                                                            |                                                                            |                    | IRQ11        | DA0        |
| D4         |                                         | P01      |                                  | TMCI0                                                       | RXD6/SMISO6/<br>SSCL6                                      |                                                                            |                    | IRQ9         | AN119      |
| D5         | VCC                                     |          |                                  |                                                             |                                                            |                                                                            |                    |              |            |
| D6         |                                         | P93      | A19                              | POE0#                                                       | CTS7#/RTS7#/<br>SS7#                                       |                                                                            |                    |              | AN117      |
| D7         |                                         | PD5      | D5[A5/D5]                        | MTIC5W/<br>MTIOC8C/<br>POE10#                               | SSLC1-A                                                    | QSPCLK-B/<br>SDHI_CLK-B/<br>MMC_CLK-B                                      | LCD_DA<br>TA19-B*1 | IRQ5         | AN113      |
| D8         |                                         | P60      | CS0#                             |                                                             |                                                            |                                                                            |                    |              |            |
| D9         |                                         | P64      | WE#/D3[A3/<br>D3]*1/CS4#         |                                                             |                                                            |                                                                            |                    |              |            |
| D10        |                                         | PE7      | D15[A15/<br>D15]/D7[A7/<br>D7]*1 | MTIOC6A/<br>TOC1                                            | MISOB-B                                                    | SDHI_WP/<br>MMC_RES#-B                                                     | LCD_DA<br>TA9-B*1  | IRQ7         | AN105      |
| D11        | VCC                                     |          |                                  |                                                             |                                                            |                                                                            |                    |              |            |
| D12        |                                         | PE5      | D13[A13/<br>D13]/D5[A5/<br>D5]*1 | MTIOC4C/<br>MTIOC2B                                         | ET0_RX_CLK/<br>REF50CK0/<br>RSPCKB-B                       |                                                                            | LCD_DA<br>TA11-B*1 | IRQ5         | AN103      |
| D13        |                                         | PE6      | D14[A14/<br>D14]/D6[A6/<br>D6]*1 | MTIOC6C/TIC1                                                | MOSIB-B                                                    | SDHI_CD/<br>MMC_CD-B                                                       | LCD_DA<br>TA10-B*1 | IRQ6         | AN104      |
| E1         | VSS                                     |          |                                  |                                                             |                                                            |                                                                            |                    |              |            |
| E2         | VCL                                     |          |                                  |                                                             |                                                            |                                                                            |                    |              |            |
| E3         |                                         | PJ5      |                                  | POE8#                                                       | CTS2#/RTS2#/<br>SS2#                                       |                                                                            |                    |              |            |

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (3/7)

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB) | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSI,<br>MMCIF, PDC) | GLCDC             | Interrupt    | A/D<br>D/A |
|------------|-----------------------------------------|----------|-------------------------|-------------------------------------------------------------|------------------------------------------------------------|---------------------------------------------------------------------------|-------------------|--------------|------------|
| E4         | EMLE                                    |          |                         |                                                             |                                                            |                                                                           |                   |              |            |
| E5         |                                         | P44      |                         |                                                             |                                                            |                                                                           |                   | IRQ12-<br>DS | AN004      |
| E10        |                                         | PA0      | BC0#/A0                 | MTIOC4A/<br>MTIOC6D/<br>TIOCA0/PO16/<br>CACREF              | ET0_TX_EN/<br>RMII0_TXD_EN/<br>SSLA1-B                     |                                                                           | LCD_DA<br>TA8-B*1 |              |            |
| E11        |                                         | P66      | DQM0/CS6#               | MTIOC7D                                                     |                                                            |                                                                           |                   |              |            |
| E12        |                                         | P65      | CKE/CS5#                |                                                             |                                                            |                                                                           |                   |              |            |
| E13        |                                         | P67      | DQM1/CS7#               | MTIOC7C                                                     |                                                            |                                                                           |                   | IRQ15        |            |
| F1         | XCIN                                    |          |                         |                                                             |                                                            |                                                                           |                   |              |            |
| F2         | XCOUT                                   |          |                         |                                                             |                                                            |                                                                           |                   |              |            |
| F3         |                                         | PJ3      | EDACK1                  | MTIOC3C                                                     | ET0_EXOUT/<br>CTS6#/RTS6#/<br>SS6#/CTS0#/<br>RTS0#/SS0#    |                                                                           |                   |              |            |
| F4         | VBATT                                   |          |                         |                                                             |                                                            |                                                                           |                   |              |            |
| F10        |                                         | PA3      | A3                      | MTIOC0D/<br>MTCLKD/<br>TIOC0D/<br>TCLKB/PO19                | ET0_MDIO/<br>RXD5/SMISO5/<br>SSCL5                         |                                                                           | LCD_DA<br>TA5-B*1 | IRQ6-DS      |            |
| F11        | VSS                                     |          |                         |                                                             |                                                            |                                                                           |                   |              |            |
| F12        |                                         | PA1      | A1                      | MTIOC0B/<br>MTCLKC/<br>MTIOC7B/<br>TIOCB0/PO17              | ET0_WOL/<br>SCK5/SSLA2-B                                   |                                                                           | LCD_DA<br>TA7-B*1 | IRQ11        |            |
| F13        |                                         | PA2      | A2                      | MTIOC7A/<br>PO18                                            | RXD5/SMISO5/<br>SSCL5/SSLA3-B                              |                                                                           | LCD_DA<br>TA6-B*1 |              |            |
| G1         | XTAL                                    | P37      |                         |                                                             |                                                            |                                                                           |                   |              |            |
| G2         | RES#                                    |          |                         |                                                             |                                                            |                                                                           |                   |              |            |
| G3         | MD/FINED                                |          |                         |                                                             |                                                            |                                                                           |                   |              |            |
| G4         | BSCANP                                  |          |                         |                                                             |                                                            |                                                                           |                   |              |            |
| G10        |                                         | PA5      | A5                      | MTIOC6B/<br>TIOCB1/PO21                                     | ET0_LINKSTA/<br>RSPCKA-B                                   |                                                                           | LCD_DA<br>TA3-B*1 |              |            |
| G11        |                                         | PA6      | A6                      | MTIC5V/<br>MTCLKB/<br>TIOCA2/<br>TMC13/PO22/<br>POE10#      | ET0_EXOUT/<br>CTS5#/RTS5#/<br>SS5#/MOSIA-B                 |                                                                           | LCD_DA<br>TA2-B*1 |              |            |
| G12        | VCC                                     |          |                         |                                                             |                                                            |                                                                           |                   |              |            |
| G13        |                                         | PA4      | A4                      | MTIC5U/<br>MTCLKA/<br>TIOCA1/<br>TMRI0/PO20                 | ET0_MDC/TXD5/<br>SMOSI5/SSDA5/<br>SSLA0-B                  |                                                                           | LCD_DA<br>TA4-B*1 | IRQ5-DS      |            |
| H1         | EXTAL                                   | P36      |                         |                                                             |                                                            |                                                                           |                   |              |            |
| H2         | VCC                                     |          |                         |                                                             |                                                            |                                                                           |                   |              |            |
| H3         | VSS                                     |          |                         |                                                             |                                                            |                                                                           |                   |              |            |
| H4         | UPSEL                                   | P35      |                         |                                                             |                                                            |                                                                           |                   | NMI          |            |
| H10        |                                         | P72      | A19/CS2#                |                                                             | ET0_MDC                                                    |                                                                           |                   |              |            |
| H11        |                                         | P71      | A18/CS1#                |                                                             | ET0_MDIO                                                   |                                                                           |                   |              |            |

**Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (4/7)**

| Pin Number       |                                         |          |                                | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC)                 | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)                  | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSI,<br>MMCIF, PDC) | GLCDC             | Interrupt | A/D<br>D/A |
|------------------|-----------------------------------------|----------|--------------------------------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------------|---------------------------------------------------------------------------|-------------------|-----------|------------|
| 145-Pin<br>TFLGA | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC        |                                                                             |                                                                             |                                                                           |                   |           |            |
| H12              |                                         | PB0      | A8                             | MTIC5W/<br>TIOCA3/PO24                                                      | ET0_ERXD1/<br>RMII0_RXD1/<br>RXD4/SMISO4/<br>SSCL4/RXD6/<br>SMISO6/SSCL6    |                                                                           | LCD_DA<br>TA0-B*1 | IRQ12     |            |
| H13              |                                         | PA7      | A7                             | TIOCB2/PO23                                                                 | ET0_WOL/<br>MISOA-B                                                         |                                                                           | LCD_DA<br>TA1-B*1 |           |            |
| J1               | TRST#                                   | P34      |                                | MTIOC0A/<br>TMC13/PO12/<br>POE10#                                           | ET0_LINKSTA/<br>SCK6/SCK0                                                   |                                                                           |                   | IRQ4      |            |
| J2               |                                         | P33      | EDREQ1                         | MTIOC0D/<br>TIOCD0/<br>TMRI3/PO11/<br>POE4#/<br>POE11#                      | RXD6/SMISO6/<br>SSCL6/RXD0/<br>SMISO0/SSCL0/<br>CRX0                        | PCKO                                                                      |                   | IRQ3-DS   |            |
| J3               |                                         | P32      |                                | MTIOC0C/<br>TIOCC0/<br>TMO3/PO10/<br>RTIC2/<br>RTICOUT/<br>POE0#/<br>POE10# | TXD6/SMOSI6/<br>SSDA6/TXD0/<br>SMOSI0/SSDA0/<br>CTX0/<br>USB0_VBUSEN        | VSYNC                                                                     |                   | IRQ2-DS   |            |
| J4               | TDI                                     | P30      |                                | MTIOC4B/<br>TMRI3/PO8/<br>RTIC0/<br>POE8#                                   | RXD1/SMISO1/<br>SSCL1/MISOB-A                                               |                                                                           |                   | IRQ0-DS   |            |
| J10              |                                         | PB3      | A11                            | MTIOC0A/<br>MTIOC4A/<br>TIOCD3/<br>TCLKD/TMO0/<br>PO27/POE11#               | ET0_RX_ER/<br>RMII0_RX_ER/<br>SCK4/SCK6                                     | SDSI_D3-B                                                                 | LCD_TC<br>ON1-B*1 |           |            |
| J11              |                                         | PB4      | A12                            | TIOCA4/PO28                                                                 | ET0_TX_EN/<br>RMII0_TXD_EN/<br>CTS9#/RTS9#/<br>SS9#/SS11#/<br>CTS11#/RTS11# | SDSI_CMD-B                                                                | LCD_TC<br>ON0-B*1 |           |            |
| J12              |                                         | PB2      | A10                            | TIOCC3/<br>TCLKC/PO26                                                       | ET0_RX_CLK/<br>REF50CK0/<br>CTS4#/RTS4#/<br>SS4#/CTS6#/<br>RTS6#/SS6#       | SDSI_D2-B                                                                 | LCD_TC<br>ON2-B*1 |           |            |
| J13              |                                         | PB1      | A9                             | MTIOC0C/<br>MTIOC4C/<br>TIOCB3/<br>TMC10/PO25                               | ET0_ERXD0/<br>RMII0_RXD0/<br>TXD4/SMOSI4/<br>SSDA4/TXD6/<br>SMOSI6/SSDA6    |                                                                           | LCD_TC<br>ON3-B*1 | IRQ4-DS   |            |
| K1               | TCK                                     | P27      | CS7#                           | MTIOC2B/<br>TMC13/PO7                                                       | SCK1/RSPCKB-A                                                               |                                                                           |                   |           |            |
| K2               | TDO                                     | P26      | CS6#                           | MTIOC2A/<br>TMO1/PO6                                                        | TXD1/SMOSI1/<br>SSDA1/CTS3#/<br>RTS3#/SS3#/<br>MOSIB-A                      |                                                                           |                   |           |            |
| K3               | TMS                                     | P31      |                                | MTIOC4D/<br>TMC12/PO9/<br>RTIC1                                             | CTS1#/RTS1#/<br>SS1#/SSLB0-A                                                |                                                                           |                   | IRQ1-DS   |            |
| K4               |                                         | P15      |                                | MTIOC0B/<br>MTCLKB/<br>TIOCB2/<br>TCLKB/TMC12/<br>PO13                      | RXD1/SMISO1/<br>SSCL1/SCK3/<br>CRX1-DS                                      | PIXD0                                                                     |                   | IRQ5      |            |
| K5               | TRDATA2                                 | P54      | ALE/<br>D1[A1/D1]*1/<br>EDACK0 | MTIOC4B/<br>TMC1                                                            | ET0_LINKSTA/<br>CTS2#/RTS2#/<br>SS2#/CTX1                                   |                                                                           |                   |           |            |
| K6               |                                         | P53*2    | BCLK                           |                                                                             |                                                                             |                                                                           |                   |           |            |

**Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (5/7)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC                         | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC)  | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)                                                 | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC                       | Interrupt | A/D<br>D/A  |
|------------|-----------------------------------------|----------|-------------------------------------------------|--------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------|-----------------------------|-----------|-------------|
| K7         |                                         | P51      | WR1#/<br>BC1#/<br>WAIT#                         |                                                              | SCK2/SSLB2-A                                                                                               |                                                                            |                             |           |             |
| K8         | VCC                                     |          |                                                 |                                                              |                                                                                                            |                                                                            |                             |           |             |
| K9         | TRDATA0                                 | P80      | EDREQ0                                          | MTIOC3B/<br>PO26                                             | ET0_TX_EN/<br>RMII0_TXD_EN/<br>SCK10/RTS10#                                                                | QIO2-A/SDHI_WP/<br>MMC_D2-A                                                |                             |           |             |
| K10        | TRDATA6                                 | P76      | CS6#                                            | PO22                                                         | ET0_RX_CLK/<br>REF50CK0/<br>SMISO11/<br>SSCL11/RXD11                                                       | QSSL-A/<br>SDHI_CMD-A/<br>SDSI_CMD-A/<br>MMC_CMD-A                         |                             |           |             |
| K11        |                                         | PB7      | A15                                             | MTIOC3B/<br>TIOCB5/PO31                                      | ET0_CRS/<br>RMII0_CRS_DV/<br>TXD9/SMOSI9/<br>SSDA9/<br>SMOSI11/<br>SSDA11/TXD11                            | SDSI_D1-B                                                                  |                             |           |             |
| K12        |                                         | PB6      | A14                                             | MTIOC3D/<br>TIOCA5/PO30                                      | ET0_ETXD1/<br>RMII0_TXD1/<br>RXD9/SMISO9/<br>SSCL9/<br>SMISO11/<br>SSCL11/RXD11                            | SDSI_D0-B                                                                  |                             |           |             |
| K13        |                                         | PB5      | A13                                             | MTIOC2A/<br>MTIOC1B/<br>TIOCB4/<br>TMRI1/PO29/<br>POE4#      | ET0_ETXD0/<br>RMII0_TXD0/<br>SCK9/SCK11                                                                    | SDSI_CLK-B                                                                 | LCD_CL<br>K-B* <sup>†</sup> |           |             |
| L1         |                                         | P25      | CS5#/<br>EDACK1                                 | MTIOC4C/<br>MTCLKB/<br>TIOCA4/PO5                            | RXD3/SMISO3/<br>SSCL3                                                                                      | SDHI_CD* <sup>1</sup> /<br>HSYNC                                           |                             |           | ADTRG0<br># |
| L2         |                                         | P23      | EDACK0                                          | MTIOC3D/<br>MTCLKD/<br>TIOCD3/PO3                            | TXD3/SMOSI3/<br>SSDA3/CTS0#/<br>RTS0#SS0#                                                                  | SDHI_D1-C* <sup>1</sup> /<br>PIXD7                                         |                             |           |             |
| L3         |                                         | P16      |                                                 | MTIOC3C/<br>MTIOC3D/<br>TIOCB1/<br>TCLKC/TMO2/<br>PO14/RTCOU | TXD1/SMOSI1/<br>SSDA1/RXD3/<br>SMISO3/SSCL3/<br>SCL2-DS/<br>USB0_VBUSEN/<br>USB0_VBUS/<br>USB0_OVRCUR<br>B |                                                                            |                             | IRQ6      | ADTRG0<br># |
| L4         |                                         | P24      | CS4#/<br>EDREQ1                                 | MTIOC4A/<br>MTCLKA/<br>TIOCB4/<br>TMRI1/PO4                  | SCK3/<br>USB0_VBUSEN                                                                                       | SDHI_WP* <sup>1</sup> /<br>PIXCLK                                          |                             |           |             |
| L5         |                                         | P13      |                                                 | MTIOC0B/<br>TIOCA5/TMO3/<br>PO13                             | TXD2/SMOSI2/<br>SSDA2/<br>SDA0[FM+]                                                                        |                                                                            |                             | IRQ3      | ADTRG1<br># |
| L6         |                                         | P56      | EDACK1                                          | MTIOC3C/<br>TIOCA1                                           | SCK7* <sup>1</sup>                                                                                         |                                                                            |                             |           |             |
| L7         |                                         | P52      | RD#                                             |                                                              | RXD2/SMISO2/<br>SSCL2/SSLB3-A                                                                              |                                                                            |                             |           |             |
| L8         | TRCLK                                   | P83      | EDACK1                                          | MTIOC4C                                                      | ET0_CRS/<br>RMII0_CRS_DV/<br>SCK10/SS10#/<br>CTS10#                                                        |                                                                            |                             |           |             |
| L9         |                                         | PC5      | D3[A3/D3]* <sup>1</sup> /<br>A21/CS2#/<br>WAIT# | MTIOC3B/<br>MTCLKD/<br>TMRI2/PO29                            | ET0_ETXD2/<br>SCK8/SCK10/<br>RSPCKA-A                                                                      | MMC_D5-A                                                                   |                             |           |             |
| L10        |                                         | PC4      | A20/CS3#                                        | MTIOC3D/<br>MTCLKC/<br>TMCI1/PO25/<br>POE0#                  | ET0_TX_CLK/<br>SCK5/CTS8#/<br>RTS8#SS8#/<br>SS10#CTS10#/<br>RTS10#SSLA0-<br>A                              | QMI-A/QIO1-A/<br>SDHI_D1-A/<br>SDSI_D1-A/<br>MMC_D1-A                      |                             |           |             |

**Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (6/7)**

| Pin Number       |                                         |          |                          | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC)              | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)                   | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) |       |           |             |
|------------------|-----------------------------------------|----------|--------------------------|--------------------------------------------------------------------------|------------------------------------------------------------------------------|----------------------------------------------------------------------------|-------|-----------|-------------|
| 145-Pin<br>TFLGA | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC  |                                                                          |                                                                              |                                                                            | GLCDC | Interrupt | A/D<br>D/A  |
| L11              |                                         | PC2      | A18                      | MTIOC4B/<br>TCLKA/PO21                                                   | ET0_RX_DV/<br>RXD5/SMISO5/<br>SSCL5/SSLA3-A                                  | SDHI_D3-A/<br>SDSDI_D3-A/<br>MMC_CD-A                                      |       |           |             |
| L12              | TRDATA4                                 | P73      | CS3#                     | PO16                                                                     | ET0_WOL                                                                      |                                                                            |       |           |             |
| L13              | VSS                                     |          |                          |                                                                          |                                                                              |                                                                            |       |           |             |
| M1               |                                         | P22      | EDREQ0                   | MTIOC3B/<br>MTCLKC/<br>TIOCC3/<br>TMO0/PO2                               | SCK0/<br>USB0_OVRCUR<br>B                                                    | SDHI_D0-C*1/<br>PIXD6                                                      |       |           |             |
| M2               |                                         | P17      |                          | MTIOC3A/<br>MTIOC3B/<br>MTIOC4B/<br>TIOCB0/<br>TCLKD/TMO1/<br>PO15/POE8# | SCK1/TXD3/<br>SMOSI3/SSDA3/<br>SDA2-DS                                       | SDHI_D3-C*1/<br>PIXD3                                                      |       | IRQ7      | ADTRG1<br># |
| M3               |                                         | P86      |                          | MTIOC4D/<br>TIOCA0                                                       | SMISO10/<br>SSCL10/RXD10                                                     | PIXD1                                                                      |       |           |             |
| M4               |                                         | P12      |                          | TMC11                                                                    | RXD2/SMISO2/<br>SSCL2/<br>SCL0[FM+]                                          |                                                                            |       | IRQ2      |             |
| M5               | VCC_USB                                 |          |                          |                                                                          |                                                                              |                                                                            |       |           |             |
| M6               | VSS_USB                                 |          |                          |                                                                          |                                                                              |                                                                            |       |           |             |
| M7               |                                         | P50      | WR0#/WR#                 |                                                                          | TXD2/SMOSI2/<br>SSDA2/SSLB1-A                                                |                                                                            |       |           |             |
| M8               |                                         | PC6      | D2[A2/D2]*1/<br>A22/CS1# | MTIOC3C/<br>MTCLKA/<br>TMC12/PO30/<br>TIC0                               | ET0_ETXD3/<br>RXD8/SMISO8/<br>SSCL8/<br>SMISO10/<br>SSCL10/RXD10/<br>MOSIA-A | MMC_D6-A                                                                   |       | IRQ13     |             |
| M9               | TRDATA1                                 | P81      | EDACK0                   | MTIOC3D/<br>PO27                                                         | ET0_ETXD0/<br>RMII0_TXD0/<br>SMISO10/<br>SSCL10/RXD10                        | QIO3-A/SDHI_CD/<br>MMC_D3-A                                                |       |           |             |
| M10              | TRDATA7                                 | P77      | CS7#                     | PO23                                                                     | ET0_RX_ER/<br>RMII0_RX_ER/<br>SMOSI11/<br>SSDA11/TXD11                       | QSPCLK-A/<br>SDHI_CLK-A/<br>SDSDI_CLK-A/<br>MMC_CLK-A                      |       |           |             |
| M11              |                                         | PC0      | A16                      | MTIOC3C/<br>TCLKC/PO17                                                   | ET0_ERXD3/<br>CTS5#/RTS5#/<br>SS5#/SSLA1-A                                   |                                                                            |       | IRQ14     |             |
| M12              |                                         | PC1      | A17                      | MTIOC3A/<br>TCLKD/PO18                                                   | ET0_ERXD2/<br>SCK5/SSLA2-A                                                   |                                                                            |       | IRQ12     |             |
| M13              | VCC                                     |          |                          |                                                                          |                                                                              |                                                                            |       |           |             |
| N1               |                                         | P21      |                          | MTIOC1B/<br>MTIOC4A/<br>TIOCA3/<br>TMC10/PO1                             | RXD0/SMISO0/<br>SSCL0/SCL1*1/<br>USB0_EXICEN                                 | SDHI_CLK-C*1/<br>PIXD5                                                     |       | IRQ9      |             |
| N2               |                                         | P20      |                          | MTIOC1A/<br>TIOCB3/<br>TMRI0/PO0                                         | TXD0/SMOSI0/<br>SSDA0/SDA1*1/<br>USB0_ID                                     | SDHI_CMD-C*1/<br>PIXD4                                                     |       | IRQ8      |             |
| N3               |                                         | P87      |                          | MTIOC4C/<br>TIOCA2                                                       | SMOSI10/<br>SSDA10/TXD10                                                     | SDHI_D2-C*1/<br>PIXD2                                                      |       |           |             |
| N4               |                                         | P14      |                          | MTIOC3A/<br>MTCLKA/<br>TIOCB5/<br>TCLKA/TMRI2/<br>PO15                   | CTS1#/RTS1#/<br>SS1#/CTX1/<br>USB0_OVRCUR<br>A                               |                                                                            |       | IRQ4      |             |
| N5               |                                         |          |                          |                                                                          | USB0_DM                                                                      |                                                                            |       |           |             |
| N6               |                                         |          |                          |                                                                          | USB0_DP                                                                      |                                                                            |       |           |             |

**Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (7/7)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC          | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)             | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSI,<br>MMCIF, PDC) | GLCDC | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|----------------------------------|-------------------------------------------------------------|------------------------------------------------------------------------|---------------------------------------------------------------------------|-------|-----------|------------|
| N7         | TRDATA3                                 | P55      | D0[A0/D0]*1/<br>WAIT#/<br>EDREQ0 | MTIOC4D/<br>TMO3                                            | ET0_EXOUT/<br>TXD7*1/<br>SMOSI7*1/<br>SSDA7*1/CRX1                     |                                                                           |       | IRQ10     |            |
| N8         | VSS                                     |          |                                  |                                                             |                                                                        |                                                                           |       |           |            |
| N9         | UB                                      | PC7      | A23/CS0#                         | MTIOC3A/<br>MTCLKB/<br>TMO2/PO31/<br>TOC0/<br>CACREF        | ET0_COL/TXD8/<br>SMOSI8/SSDA8/<br>SMOSI10/<br>SSDA10/TXD10/<br>MISOA-A | MMC_D7-A                                                                  |       | IRQ14     |            |
| N10        | TRSYNC                                  | P82      | EDREQ1                           | MTIOC4A/<br>PO28                                            | ET0_ETXD1/<br>RMII0_TXD1/<br>SMOSI10/<br>SSDA10/TXD10                  | MMC_D4-A                                                                  |       |           |            |
| N11        |                                         | PC3      | A19                              | MTIOC4D/<br>TCLKB/PO24                                      | ET0_TX_ER/<br>TXD5/SMOSI5/<br>SSDA5                                    | QMO-A/QIO0-A/<br>SDHI_D0-A/<br>SDSI_D0-A/<br>MMC_D0-A                     |       |           |            |
| N12        | TRSYNC1                                 | P75      | CS5#                             | PO20                                                        | ET0_ERXD0/<br>RMII0_RXD0/<br>SCK11/RTS11#                              | SDHI_D2-A/<br>SDSI_D2-A/<br>MMC_RES#-A                                    |       |           |            |
| N13        | TRDATA5                                 | P74      | A20/CS4#                         | PO19                                                        | ET0_ERXD1/<br>RMII0_RXD1/<br>SS11#/CTS11#                              |                                                                           |       |           |            |

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.

Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

## 1.6.4 144-Pin LFQFP

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (1/7)

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC)                 | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)           | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|-------------------------|-----------------------------------------------------------------------------|----------------------------------------------------------------------|----------------------------------------------------------------------------|-------|-----------|------------|
| 1          | AVSS0                                   |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 2          |                                         | P05      |                         |                                                                             |                                                                      |                                                                            |       | IRQ13     | DA1        |
| 3          | AVCC1                                   |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 4          |                                         | P03      |                         |                                                                             |                                                                      |                                                                            |       | IRQ11     | DA0        |
| 5          | AVSS1                                   |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 6          |                                         | P02      |                         | TMCI1                                                                       | SCK6                                                                 |                                                                            |       | IRQ10     | AN120      |
| 7          |                                         | P01      |                         | TMC10                                                                       | RXD6/SMISO6/<br>SSCL6                                                |                                                                            |       | IRQ9      | AN119      |
| 8          |                                         | P00      |                         | TMRI0                                                                       | TXD6/SMOSI6/<br>SSDA6                                                |                                                                            |       | IRQ8      | AN118      |
| 9          |                                         | PF5      |                         |                                                                             |                                                                      |                                                                            |       | IRQ4      |            |
| 10         | EMLE                                    |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 11         |                                         | PJ5      |                         | POE8#                                                                       | CTS2#/RTS2#/<br>SS2#                                                 |                                                                            |       |           |            |
| 12         | VSS                                     |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 13         |                                         | PJ3      | EDACK1                  | MTIOC3C                                                                     | ET0_EXOUT/<br>CTS6#/RTS6#/<br>SS6#/CTS0#/<br>RTS0#/SS0#              |                                                                            |       |           |            |
| 14         | VCL                                     |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 15         | VBATT                                   |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 16         | MD/FINED                                |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 17         | XCIN                                    |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 18         | XCOUT                                   |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 19         | RES#                                    |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 20         | XTAL                                    | P37      |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 21         | VSS                                     |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 22         | EXTAL                                   | P36      |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 23         | VCC                                     |          |                         |                                                                             |                                                                      |                                                                            |       |           |            |
| 24         | UPSEL                                   | P35      |                         |                                                                             |                                                                      |                                                                            |       | NMI       |            |
| 25         | TRST#                                   | P34      |                         | MTIOC0A/<br>TMCI3/PO12/<br>POE10#                                           | ET0_LINKSTA/<br>SCK6/SCK0                                            |                                                                            |       | IRQ4      |            |
| 26         |                                         | P33      | EDREQ1                  | MTIOC0D/<br>TIOC0D/<br>TMRI3/PO11/<br>POE4#/<br>POE11#                      | RXD6/SMISO6/<br>SSCL6/RXD0/<br>SMISO0/SSCL0/<br>CRX0                 | PCKO                                                                       |       | IRQ3-DS   |            |
| 27         |                                         | P32      |                         | MTIOC0C/<br>TIOC0C/<br>TMO3/PO10/<br>RTCIC2/<br>RTCOUT/<br>POE0#/<br>POE10# | TXD6/SMOSI6/<br>SSDA6/TXD0/<br>SMOSI0/SSDA0/<br>CTX0/<br>USB0_VBUSEN | VSYNC                                                                      |       | IRQ2-DS   |            |
| 28         | TMS                                     | P31      |                         | MTIOC4D/<br>TMCI2/PO9/<br>RTCIC1                                            | CTS1#/RTS1#/<br>SS1#/SSLB0-A                                         |                                                                            |       | IRQ1-DS   |            |

**Table 1.8 List of Pin and Pin Functions (144-Pin LQFP) (2/7)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC)              | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)                                                 | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC | Interrupt | A/D<br>D/A  |
|------------|-----------------------------------------|----------|-------------------------|--------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------|-------|-----------|-------------|
| 29         | TDI                                     | P30      |                         | MTIOC4B/<br>TMRI3/PO8/<br>RTCIC0/<br>POE8#                               | RXD1/SMISO1/<br>SSCL1/MISOB-A                                                                              |                                                                            |       | IRQ0-DS   |             |
| 30         | TCK                                     | P27      | CS7#                    | MTIOC2B/<br>TMCI3/PO7                                                    | SCK1/RSPCKB-A                                                                                              |                                                                            |       |           |             |
| 31         | TDO                                     | P26      | CS6#                    | MTIOC2A/<br>TMO1/PO6                                                     | TXD1/SMOSI1/<br>SSDA1/CTS3#/<br>RTS3#/SS3#/<br>MOSIB-A                                                     |                                                                            |       |           |             |
| 32         |                                         | P25      | CS5#/<br>EDACK1         | MTIOC4C/<br>MTCLKB/<br>TIOCA4/PO5                                        | RXD3/SMISO3/<br>SSCL3                                                                                      | SDHI_CD*1/<br>HSYNC                                                        |       |           | ADTRG0<br># |
| 33         |                                         | P24      | CS4#/<br>EDREQ1         | MTIOC4A/<br>MTCLKA/<br>TIOCB4/<br>TMRI1/PO4                              | SCK3/<br>USB0_VBUSEN                                                                                       | SDHI_WP*1/<br>PIXCLK                                                       |       |           |             |
| 34         |                                         | P23      | EDACK0                  | MTIOC3D/<br>MTCLKD/<br>TIOCD3/PO3                                        | TXD3/SMOSI3/<br>SSDA3/CTS0#/<br>RTS0#/SS0#                                                                 | SDHI_D1-C*1/<br>PIXD7                                                      |       |           |             |
| 35         |                                         | P22      | EDREQ0                  | MTIOC3B/<br>MTCLKC/<br>TIOCC3/<br>TMO0/PO2                               | SCK0/<br>USB0_OVRCUR<br>B                                                                                  | SDHI_D0-C*1/<br>PIXD6                                                      |       |           |             |
| 36         |                                         | P21      |                         | MTIOC1B/<br>MTIOC4A/<br>TIOCA3/<br>TMCI0/PO1                             | RXD0/SMISO0/<br>SSCL0/SCL1*1/<br>USB0_EXICEN                                                               | SDHI_CLK-C*1/<br>PIXD5                                                     |       | IRQ9      |             |
| 37         |                                         | P20      |                         | MTIOC1A/<br>TIOCB3/<br>TMRI0/PO0                                         | TXD0/SMOSI0/<br>SSDA0/SDA1*1/<br>USB0_ID                                                                   | SDHI_CMD-C*1/<br>PIXD4                                                     |       | IRQ8      |             |
| 38         |                                         | P17      |                         | MTIOC3A/<br>MTIOC3B/<br>MTIOC4B/<br>TIOCB0/<br>TCLKD/TMO1/<br>PO15/POE8# | SCK1/TXD3/<br>SMOSI3/SSDA3/<br>SDA2-DS                                                                     | SDHI_D3-C*1/<br>PIXD3                                                      |       | IRQ7      | ADTRG1<br># |
| 39         |                                         | P87      |                         | MTIOC4C/<br>TIOCA2                                                       | SMOSI10/<br>SSDA10/TXD10                                                                                   | SDHI_D2-C*1/<br>PIXD2                                                      |       |           |             |
| 40         |                                         | P16      |                         | MTIOC3C/<br>MTIOC3D/<br>TIOCB1/<br>TCLKC/TMO2/<br>PO14/RTCOU             | TXD1/SMOSI1/<br>SSDA1/RXD3/<br>SMISO3/SSCL3/<br>SCL2-DS/<br>USB0_VBUSEN/<br>USB0_VBUS/<br>USB0_OVRCUR<br>B |                                                                            |       | IRQ6      | ADTRG0<br># |
| 41         |                                         | P86      |                         | MTIOC4D/<br>TIOCA0                                                       | SMISO10/<br>SSCL10/RXD10                                                                                   | PIXD1                                                                      |       |           |             |
| 42         |                                         | P15      |                         | MTIOC0B/<br>MTCLKB/<br>TIOCB2/<br>TCLKB/TMCI2/<br>PO13                   | RXD1/SMISO1/<br>SSCL1/SCK3/<br>CRX1-DS                                                                     | PIXD0                                                                      |       | IRQ5      |             |
| 43         |                                         | P14      |                         | MTIOC3A/<br>MTCLKA/<br>TIOCB5/<br>TCLKA/TMRI2/<br>PO15                   | CTS1#/RTS1#/<br>SS1#/CTX1/<br>USB0_OVRCUR<br>A                                                             |                                                                            |       | IRQ4      |             |
| 44         |                                         | P13      |                         | MTIOC0B/<br>TIOCA5/TMO3/<br>PO13                                         | TXD2/SMOSI2/<br>SSDA2/<br>SDA0[FM+]                                                                        |                                                                            |       | IRQ3      | ADTRG1<br># |
| 45         |                                         | P12      |                         | TMCI1                                                                    | RXD2/SMISO2/<br>SSCL2/<br>SCL0[FM+]                                                                        |                                                                            |       | IRQ2      |             |

**Table 1.8 List of Pin and Pin Functions (144-Pin LQFP) (3/7)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC            | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)                   | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDI,<br>MMCIF, PDC) | GLCDC | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|------------------------------------|-------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------------------|-------|-----------|------------|
| 46         | VCC_USB                                 |          |                                    |                                                             |                                                                              |                                                                          |       |           |            |
| 47         |                                         |          |                                    |                                                             | USB0_DM                                                                      |                                                                          |       |           |            |
| 48         |                                         |          |                                    |                                                             | USB0_DP                                                                      |                                                                          |       |           |            |
| 49         | VSS_USB                                 |          |                                    |                                                             |                                                                              |                                                                          |       |           |            |
| 50         |                                         | P56      | EDACK1                             | MTIOC3C/<br>TIOCA1                                          | SCK7*1                                                                       |                                                                          |       |           |            |
| 51         | TRDATA3                                 | P55      | D0[A0/D0]*1/<br>WAIT#/<br>EDREQ0   | MTIOC4D/<br>TMO3                                            | ET0_EXOUT/<br>TXD7*1/<br>SMOSI7*1/<br>SSDA7*1/CRX1                           |                                                                          |       | IRQ10     |            |
| 52         | TRDATA2                                 | P54      | ALE/D1[A1/<br>D1]*1/<br>EDACK0     | MTIOC4B/<br>TMC1                                            | ET0_LINKSTA/<br>CTS2#/RTS2#/<br>SS2#/CTX1                                    |                                                                          |       |           |            |
| 53         |                                         | P53*2    | BCLK                               |                                                             |                                                                              |                                                                          |       |           |            |
| 54         |                                         | P52      | RD#                                |                                                             | RXD2/SMISO2/<br>SSCL2/SSLB3-A                                                |                                                                          |       |           |            |
| 55         |                                         | P51      | WR1#/<br>BC1#/<br>WAIT#            |                                                             | SCK2/SSLB2-A                                                                 |                                                                          |       |           |            |
| 56         |                                         | P50      | WR0#/WR#                           |                                                             | TXD2/SMOSI2/<br>SSDA2/SSLB1-A                                                |                                                                          |       |           |            |
| 57         | VSS                                     |          |                                    |                                                             |                                                                              |                                                                          |       |           |            |
| 58         | TRCLK                                   | P83      | EDACK1                             | MTIOC4C                                                     | ET0_CRS/<br>RMII0_CRS_DV/<br>SCK10/SS10#/<br>CTS10#                          |                                                                          |       |           |            |
| 59         | VCC                                     |          |                                    |                                                             |                                                                              |                                                                          |       |           |            |
| 60         | UB                                      | PC7      | A23/CS0#                           | MTIOC3A/<br>MTCLKB/<br>TMO2/PO31/<br>TOC0/<br>CACREF        | ET0_COL/TXD8/<br>SMOSI8/SSDA8/<br>SMOSI10/<br>SSDA10/TXD10/<br>MISOA-A       | MMC_D7-A                                                                 |       | IRQ14     |            |
| 61         |                                         | PC6      | D2[A2/D2]*1/<br>A22/CS1#           | MTIOC3C/<br>MTCLKA/<br>TMC12/PO30/<br>TIC0                  | ET0_ETXD3/<br>RXD8/SMISO8/<br>SSCL8/<br>SMISO10/<br>SSCL10/RXD10/<br>MOSIA-A | MMC_D6-A                                                                 |       | IRQ13     |            |
| 62         |                                         | PC5      | D3[A3/D3]*1/<br>A21/CS2#/<br>WAIT# | MTIOC3B/<br>MTCLKD/<br>TMRI2/PO29                           | ET0_ETXD2/<br>SCK8/SCK10/<br>RSPCKA-A                                        | MMC_D5-A                                                                 |       |           |            |
| 63         | TRSYNC                                  | P82      | EDREQ1                             | MTIOC4A/<br>PO28                                            | ET0_ETXD1/<br>RMII0_TXD1/<br>SMOSI10/<br>SSDA10/TXD10                        | MMC_D4-A                                                                 |       |           |            |
| 64         | TRDATA1                                 | P81      | EDACK0                             | MTIOC3D/<br>PO27                                            | ET0_ETXD0/<br>RMII0_TXD0/<br>SMISO10/<br>SSCL10/RXD10                        | QIO3-A/SDHI_CD/<br>MMC_D3-A                                              |       |           |            |
| 65         | TRDATA0                                 | P80      | EDREQ0                             | MTIOC3B/<br>PO26                                            | ET0_TX_EN/<br>RMII0_TXD_EN/<br>SCK10/RTS10#                                  | QIO2-A/SDHI_WP/<br>MMC_D2-A                                              |       |           |            |
| 66         |                                         | PC4      | A20/CS3#                           | MTIOC3D/<br>MTCLKC/<br>TMC11/PO25/<br>POE0#                 | ET0_TX_CLK/<br>SCK5/CTS8#/<br>RTS8#/SS8#/<br>SS10#/CTS10#/<br>RTS10#/SSLA0-A | QMI-A/QIO1-A/<br>SDHI_D1-A/<br>SDSI_D1-A/<br>MMC_D1-A                    |       |           |            |

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (4/7)

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC)   | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)                      | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC             | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|-------------------------|---------------------------------------------------------------|---------------------------------------------------------------------------------|----------------------------------------------------------------------------|-------------------|-----------|------------|
| 67         |                                         | PC3      | A19                     | MTIOC4D/<br>TCLKB/PO24                                        | ET0_TX_ER/<br>TXD5/SMOSI5/<br>SSDA5                                             | QMO-A/QIO0-A/<br>SDHI_D0-A/<br>SDSDI_D0-A/<br>MMC_D0-A                     |                   |           |            |
| 68         | TRDATA7                                 | P77      | CS7#                    | PO23                                                          | ET0_RX_ER/<br>RMII0_RX_ER/<br>SMOSI11/<br>SSDA11/TXD11                          | QSPCLK-A/<br>SDHI_CLK-A/<br>SDSDI_CLK-A/<br>MMC_CLK-A                      |                   |           |            |
| 69         | TRDATA6                                 | P76      | CS6#                    | PO22                                                          | ET0_RX_CLK/<br>REF50CK0/<br>SMISO11/<br>SSCL11/RXD11                            | QSSL-A/<br>SDHI_CMD-A/<br>SDSDI_CMD-A/<br>MMC_CMD-A                        |                   |           |            |
| 70         |                                         | PC2      | A18                     | MTIOC4B/<br>TCLKA/PO21                                        | ET0_RX_DV/<br>RXD5/SMISO5/<br>SSCL5/SSLA3-A                                     | SDHI_D3-A/<br>SDSDI_D3-A/<br>MMC_CD-A                                      |                   |           |            |
| 71         | TRSYNC1                                 | P75      | CS5#                    | PO20                                                          | ET0_ERXD0/<br>RMII0_RXD0/<br>SCK11/RTS11#                                       | SDHI_D2-A/<br>SDSDI_D2-A/<br>MMC_RES#-A                                    |                   |           |            |
| 72         | TRDATA5                                 | P74      | A20/CS4#                | PO19                                                          | ET0_ERXD1/<br>RMII0_RXD1/<br>SS11#/CTS11#                                       |                                                                            |                   |           |            |
| 73         |                                         | PC1      | A17                     | MTIOC3A/<br>TCLKD/PO18                                        | ET0_ERXD2/<br>SCK5/SSLA2-A                                                      |                                                                            |                   | IRQ12     |            |
| 74         | VCC                                     |          |                         |                                                               |                                                                                 |                                                                            |                   |           |            |
| 75         |                                         | PC0      | A16                     | MTIOC3C/<br>TCLKC/PO17                                        | ET0_ERXD3/<br>CTS5#/RTS5#/<br>SS5#/SSLA1-A                                      |                                                                            |                   | IRQ14     |            |
| 76         | VSS                                     |          |                         |                                                               |                                                                                 |                                                                            |                   |           |            |
| 77         | TRDATA4                                 | P73      | CS3#                    | PO16                                                          | ET0_WOL                                                                         |                                                                            |                   |           |            |
| 78         |                                         | PB7      | A15                     | MTIOC3B/<br>TIOCB5/PO31                                       | ET0_CRS/<br>RMII0_CRS_DV/<br>TXD9/SMOSI9/<br>SSDA9/<br>SMOSI11/<br>SSDA11/TXD11 | SDSDI_D1-B                                                                 |                   |           |            |
| 79         |                                         | PB6      | A14                     | MTIOC3D/<br>TIOCA5/PO30                                       | ET0_ETXD1/<br>RMII0_TXD1/<br>RXD9/SMISO9/<br>SSCL9/<br>SMISO11/<br>SSCL11/RXD11 | SDSDI_D0-B                                                                 |                   |           |            |
| 80         |                                         | PB5      | A13                     | MTIOC2A/<br>MTIOC1B/<br>TIOCB4/<br>TMRI1/PO29/<br>POE4#       | ET0_ETXD0/<br>RMII0_TXD0/<br>SCK9/SCK11                                         | SDSDI_CLK-B                                                                | LCD_CL<br>K-B*1   |           |            |
| 81         |                                         | PB4      | A12                     | TIOCA4/PO28                                                   | ET0_TX_EN/<br>RMII0_TXD_EN/<br>CTS9#/RTS9#/<br>SS9#/SS11#/<br>CTS11#/RTS11#     | SDSDI_CMD-B                                                                | LCD_TC<br>ON0-B*1 |           |            |
| 82         |                                         | PB3      | A11                     | MTIOC0A/<br>MTIOC4A/<br>TIOC3D/<br>TCLKD/TMO0/<br>PO27/POE11# | ET0_RX_ER/<br>RMII0_RX_ER/<br>SCK4/SCK6                                         | SDSDI_D3-B                                                                 | LCD_TC<br>ON1-B*1 |           |            |
| 83         |                                         | PB2      | A10                     | TIOCC3/<br>TCLKC/PO26                                         | ET0_RX_CLK/<br>REF50CK0/<br>CTS4#/RTS4#/<br>SS4#/CTS6#/<br>RTS6#/SS6#           | SDSDI_D2-B                                                                 | LCD_TC<br>ON2-B*1 |           |            |

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (5/7)

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC          | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)               | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC              | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|----------------------------------|-------------------------------------------------------------|--------------------------------------------------------------------------|----------------------------------------------------------------------------|--------------------|-----------|------------|
| 84         |                                         | PB1      | A9                               | MTIOC0C/<br>MTIOC4C/<br>TIOCB3/<br>TMCI0/PO25               | ET0_ERXD0/<br>RMII0_RXD0/<br>TXD4/SMOSI4/<br>SSDA4/TXD6/<br>SMOSI6/SSDA6 |                                                                            | LCD_TC<br>ON3-B*1  | IRQ4-DS   |            |
| 85         |                                         | P72      | A19/CS2#                         |                                                             | ET0_MDC                                                                  |                                                                            |                    |           |            |
| 86         |                                         | P71      | A18/CS1#                         |                                                             | ET0_MDIO                                                                 |                                                                            |                    |           |            |
| 87         |                                         | PB0      | A8                               | MTIC5W/<br>TIOCA3/PO24                                      | ET0_ERXD1/<br>RMII0_RXD1/<br>RXD4/SMISO4/<br>SSCL4/RXD6/<br>SMISO6/SSCL6 |                                                                            | LCD_DA<br>TA0-B*1  | IRQ12     |            |
| 88         |                                         | PA7      | A7                               | TIOCB2/PO23                                                 | ET0_WOL/<br>MISOA-B                                                      |                                                                            | LCD_DA<br>TA1-B*1  |           |            |
| 89         |                                         | PA6      | A6                               | MTIC5V/<br>MTCLKB/<br>TIOCA2/<br>TMCI3/PO22/<br>POE10#      | ET0_EXOUT/<br>CTS5#/RTS5#/<br>SS5#/MOSIA-B                               |                                                                            | LCD_DA<br>TA2-B*1  |           |            |
| 90         |                                         | PA5      | A5                               | MTIOC6B/<br>TIOCB1/PO21                                     | ET0_LINKSTA/<br>RSPCKA-B                                                 |                                                                            | LCD_DA<br>TA3-B*1  |           |            |
| 91         | VCC                                     |          |                                  |                                                             |                                                                          |                                                                            |                    |           |            |
| 92         |                                         | PA4      | A4                               | MTIC5U/<br>MTCLKA/<br>TIOCA1/<br>TMRI0/PO20                 | ET0_MDC/TXD5/<br>SMOSI5/SSDA5/<br>SSLA0-B                                |                                                                            | LCD_DA<br>TA4-B*1  | IRQ5-DS   |            |
| 93         | VSS                                     |          |                                  |                                                             |                                                                          |                                                                            |                    |           |            |
| 94         |                                         | PA3      | A3                               | MTIOC0D/<br>MTCLKD/<br>TIOCDO/<br>TCLKB/PO19                | ET0_MDIO/<br>RXD5/SMISO5/<br>SSCL5                                       |                                                                            | LCD_DA<br>TA5-B*1  | IRQ6-DS   |            |
| 95         |                                         | PA2      | A2                               | MTIOC7A/<br>PO18                                            | RXD5/SMISO5/<br>SSCL5/SSLA3-B                                            |                                                                            | LCD_DA<br>TA6-B*1  |           |            |
| 96         |                                         | PA1      | A1                               | MTIOC0B/<br>MTCLKC/<br>MTIOC7B/<br>TIOCB0/PO17              | ET0_WOL/<br>SCK5/SSLA2-B                                                 |                                                                            | LCD_DA<br>TA7-B*1  | IRQ11     |            |
| 97         |                                         | PA0      | BC0#/A0                          | MTIOC4A/<br>MTIOC6D/<br>TIOCA0/PO16/<br>CACREF              | ET0_TX_EN/<br>RMII0_TXD_EN/<br>SSLA1-B                                   |                                                                            | LCD_DA<br>TA8-B*1  |           |            |
| 98         |                                         | P67      | DQM1/CS7#                        | MTIOC7C                                                     |                                                                          |                                                                            |                    | IRQ15     |            |
| 99         |                                         | P66      | DQM0/CS6#                        | MTIOC7D                                                     |                                                                          |                                                                            |                    |           |            |
| 100        |                                         | P65      | CKE/CS5#                         |                                                             |                                                                          |                                                                            |                    |           |            |
| 101        |                                         | PE7      | D15[A15/<br>D15]/D7[A7/<br>D7]*1 | MTIOC6A/<br>TOC1                                            | MISOB-B                                                                  | SDHI_WP/<br>MMC_RES#-B                                                     | LCD_DA<br>TA9-B*1  | IRQ7      | AN105      |
| 102        |                                         | PE6      | D14[A14/<br>D14]/D6[A6/<br>D6]*1 | MTIOC6C/TIC1                                                | MOSIB-B                                                                  | SDHI_CD/<br>MMC_CD-B                                                       | LCD_DA<br>TA10-B*1 | IRQ6      | AN104      |
| 103        | VCC                                     |          |                                  |                                                             |                                                                          |                                                                            |                    |           |            |
| 104        |                                         | P70      | SDCLK                            |                                                             |                                                                          |                                                                            |                    |           |            |
| 105        | VSS                                     |          |                                  |                                                             |                                                                          |                                                                            |                    |           |            |
| 106        |                                         | PE5      | D13[A13/<br>D13]/D5[A5/<br>D5]*1 | MTIOC4C/<br>MTIOC2B                                         | ET0_RX_CLK/<br>REF50CK0/<br>RSPCKB-B                                     |                                                                            | LCD_DA<br>TA11-B*1 | IRQ5      | AN103      |
| 107        |                                         | PE4      | D12[A12/<br>D12]/D4[A4/<br>D4]*1 | MTIOC4D/<br>MTIOC1A/<br>PO28                                | ET0_ERXD2/<br>SSLB0-B                                                    |                                                                            | LCD_DA<br>TA12-B*1 |           | AN102      |

**Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (6/7)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC          | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)    | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF, PDC) | GLCDC                  | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|----------------------------------|-------------------------------------------------------------|---------------------------------------------------------------|----------------------------------------------------------------------------|------------------------|-----------|------------|
| 108        |                                         | PE3      | D11[A11/<br>D11]/D3[A3/<br>D3]*1 | MTIOC4B/<br>PO26/TOC3/<br>POE8#                             | ET0_ERXD3/<br>CTS12#/<br>RTS12#/SS12#                         | MMC_D7-B                                                                   | LCD_DA<br>TA13-B*1     |           | AN101      |
| 109        |                                         | PE2      | D10[A10/<br>D10]/D2[A2/<br>D2]*1 | MTIOC4A/<br>PO23/TIC3                                       | RXD12/<br>SMISO12/<br>SSCL12/<br>RXDX12/SSLB3-<br>B           | MMC_D6-B                                                                   | LCD_DA<br>TA14-B*1     | IRQ7-DS   | AN100      |
| 110        |                                         | PE1      | D9[A9/D9]/<br>D1[A1/D1]*1        | MTIOC4C/<br>MTIOC3B/<br>PO18                                | TXD12/<br>SMOS12/<br>SSDA12/<br>TXDX12/<br>SIOX12/SSLB2-<br>B | MMC_D5-B                                                                   | LCD_DA<br>TA15-B*1     |           | ANEX1      |
| 111        |                                         | PE0      | D8[A8/D8]/<br>D0[A0/D0]*1        | MTIOC3D                                                     | SCK12/SSLB1-B                                                 | MMC_D4-B                                                                   | LCD_DA<br>TA16-B*1     |           | ANEX0      |
| 112        |                                         | P64      | WE#D3[A3/<br>D3]*1/CS4#          |                                                             |                                                               |                                                                            |                        |           |            |
| 113        |                                         | P63      | CAS#/<br>D2[A2/D2]*1/<br>CS3#    |                                                             |                                                               |                                                                            |                        |           |            |
| 114        |                                         | P62      | RAS#/<br>D1[A1/D1]*1/<br>CS2#    |                                                             |                                                               |                                                                            |                        |           |            |
| 115        |                                         | P61      | SDCS#/<br>D0[A0/D0]*1/<br>CS1#   |                                                             |                                                               |                                                                            |                        |           |            |
| 116        | VSS                                     |          |                                  |                                                             |                                                               |                                                                            |                        |           |            |
| 117        |                                         | P60      | CS0#                             |                                                             |                                                               |                                                                            |                        |           |            |
| 118        | VCC                                     |          |                                  |                                                             |                                                               |                                                                            |                        |           |            |
| 119        |                                         | PD7      | D7[A7/D7]                        | MTIC5U/<br>POE0#                                            | SSLC3-A                                                       | QMI-B/QIO1-B/<br>SDHI_D1-B/<br>MMC_D1-B                                    | LCD_DA<br>TA17-B*1     | IRQ7      | AN107      |
| 120        |                                         | PD6      | D6[A6/D6]                        | MTIC5V/<br>MTIOC8A/<br>POE4#                                | SSLC2-A                                                       | QMO-B/QIO0-B/<br>SDHI_D0-B/<br>MMC_D0-B                                    | LCD_DA<br>TA18-B*1     | IRQ6      | AN106      |
| 121        |                                         | PD5      | D5[A5/D5]                        | MTIC5W/<br>MTIOC8C/<br>POE10#                               | SSLC1-A                                                       | QSPCLK-B/<br>SDHI_CLK-B/<br>MMC_CLK-B                                      | LCD_DA<br>TA19-B*1     | IRQ5      | AN113      |
| 122        |                                         | PD4      | D4[A4/D4]                        | MTIOC8B/<br>POE11#                                          | SSLC0-A                                                       | QSSL-B/<br>SDHI_CMD-B/<br>MMC_CMD-B                                        | LCD_DA<br>TA20-B*1     | IRQ4      | AN112      |
| 123        |                                         | PD3      | D3[A3/D3]                        | MTIOC8D/<br>TOC2/POE8#                                      | RSPCKC-A                                                      | QIO3-B/SDHI_D3-<br>B/MMC_D3-B                                              | LCD_DA<br>TA21-B*1     | IRQ3      | AN111      |
| 124        |                                         | PD2      | D2[A2/D2]                        | MTIOC4D/TIC2                                                | MISOC-A/CRX0                                                  | QIO2-B/SDHI_D2-<br>B/MMC_D2-B                                              | LCD_DA<br>TA22-B*1     | IRQ2      | AN110      |
| 125        |                                         | PD1      | D1[A1/D1]                        | MTIOC4B/<br>POE0#                                           | MOSIC-A/CTX0                                                  |                                                                            | LCD_DA<br>TA23-B*1     | IRQ1      | AN109      |
| 126        |                                         | PD0      | D0[A0/D0]                        | POE4#                                                       |                                                               |                                                                            | LCD_EX<br>TCLK-B<br>*1 | IRQ0      | AN108      |
| 127        |                                         | P93      | A19                              | POE0#                                                       | CTS7#/RTS7#/<br>SS7#                                          |                                                                            |                        |           | AN117      |
| 128        |                                         | P92      | A18                              | POE4#                                                       | RXD7/SMISO7/<br>SSCL7                                         |                                                                            |                        |           | AN116      |
| 129        |                                         | P91      | A17                              |                                                             | SCK7                                                          |                                                                            |                        |           | AN115      |
| 130        | VSS                                     |          |                                  |                                                             |                                                               |                                                                            |                        |           |            |
| 131        |                                         | P90      | A16                              |                                                             | TXD7/SMOSI7/<br>SSDA7                                         |                                                                            |                        |           | AN114      |

**Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (7/7)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC<br>SDRAMC | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB) | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSI,<br>MMCIF, PDC) | GLCDC | Interrupt    | A/D<br>D/A  |
|------------|-----------------------------------------|----------|-------------------------|-------------------------------------------------------------|------------------------------------------------------------|---------------------------------------------------------------------------|-------|--------------|-------------|
| 132        | VCC                                     |          |                         |                                                             |                                                            |                                                                           |       |              |             |
| 133        |                                         | P47      |                         |                                                             |                                                            |                                                                           |       | IRQ15-<br>DS | AN007       |
| 134        |                                         | P46      |                         |                                                             |                                                            |                                                                           |       | IRQ14-<br>DS | AN006       |
| 135        |                                         | P45      |                         |                                                             |                                                            |                                                                           |       | IRQ13-<br>DS | AN005       |
| 136        |                                         | P44      |                         |                                                             |                                                            |                                                                           |       | IRQ12-<br>DS | AN004       |
| 137        |                                         | P43      |                         |                                                             |                                                            |                                                                           |       | IRQ11-<br>DS | AN003       |
| 138        |                                         | P42      |                         |                                                             |                                                            |                                                                           |       | IRQ10-<br>DS | AN002       |
| 139        |                                         | P41      |                         |                                                             |                                                            |                                                                           |       | IRQ9-DS      | AN001       |
| 140        | VREFL0                                  |          |                         |                                                             |                                                            |                                                                           |       |              |             |
| 141        |                                         | P40      |                         |                                                             |                                                            |                                                                           |       | IRQ8-DS      | AN000       |
| 142        | VREFH0                                  |          |                         |                                                             |                                                            |                                                                           |       |              |             |
| 143        | AVCC0                                   |          |                         |                                                             |                                                            |                                                                           |       |              |             |
| 144        |                                         | P07      |                         |                                                             |                                                            |                                                                           |       | IRQ15        | ADTRG0<br># |

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.

Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

## 1.6.5 100-Pin TFLGA

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (1/5)

| Pin Number       |                                         |          |                                  | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)    | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF) |                        |              |             |
|------------------|-----------------------------------------|----------|----------------------------------|-------------------------------------------------------------|---------------------------------------------------------------|-----------------------------------------------------------------------|------------------------|--------------|-------------|
| 100-Pin<br>TFLGA | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC                    |                                                             |                                                               |                                                                       | GLCDC                  | Interrupt    | A/D<br>D/A  |
| A1               |                                         | P05      |                                  |                                                             |                                                               |                                                                       |                        | IRQ13        | DA1         |
| A2               | AVCC1                                   |          |                                  |                                                             |                                                               |                                                                       |                        |              |             |
| A3               |                                         | P07      |                                  |                                                             |                                                               |                                                                       |                        | IRQ15        | ADTRG0<br># |
| A4               | VREFL0                                  |          |                                  |                                                             |                                                               |                                                                       |                        |              |             |
| A5               |                                         | P43      |                                  |                                                             |                                                               |                                                                       |                        | IRQ11-<br>DS | AN003       |
| A6               |                                         | PD0      | D0[A0/D0]                        | POE4#                                                       |                                                               |                                                                       | LCD_EX<br>TCLK-B<br>*1 | IRQ0         | AN108       |
| A7               |                                         | PD4      | D4[A4/D4]                        | MTIOC8B/<br>POE11#                                          | SSLC0-A                                                       | QSSL-B/<br>SDHI_CMD-B/<br>MMC_CMD-B                                   | LCD_DA<br>TA20-B*1     | IRQ4         | AN112       |
| A8               |                                         | PE0      | D8[A8/D8]/<br>D0[A0/D0]*1        | MTIOC3D                                                     | SCK12/SSLB1-B                                                 | MMC_D4-B                                                              | LCD_DA<br>TA16-B*1     |              | ANEX0       |
| A9               |                                         | PE1      | D9[A9/D9]/<br>D1[A1/D1]*1        | MTIOC4C/<br>MTIOC3B/<br>PO18                                | TXD12/<br>SMOS12/<br>SSDA12/<br>TXDX12/<br>SIOX12/SSLB2-<br>B | MMC_D5-B                                                              | LCD_DA<br>TA15-B*1     |              | ANEX1       |
| A10              |                                         | PE2      | D10[A10/<br>D10]/D2[A2/<br>D2]*1 | MTIOC4A/<br>PO23/TIC3                                       | RXD12/<br>SMISO12/<br>SSCL12/<br>RXDX12/SSLB3-<br>B           | MMC_D6-B                                                              | LCD_DA<br>TA14-B*1     | IRQ7-DS      | AN100       |
| B1               | EMLE                                    |          |                                  |                                                             |                                                               |                                                                       |                        |              |             |
| B2               | AVSS0                                   |          |                                  |                                                             |                                                               |                                                                       |                        |              |             |
| B3               | AVCC0                                   |          |                                  |                                                             |                                                               |                                                                       |                        |              |             |
| B4               |                                         | P40      |                                  |                                                             |                                                               |                                                                       |                        | IRQ8-DS      | AN000       |
| B5               |                                         | P44      |                                  |                                                             |                                                               |                                                                       |                        | IRQ12-<br>DS | AN004       |
| B6               |                                         | PD1      | D1[A1/D1]                        | MTIOC4B/<br>POE0#                                           | MOSIC-A/CTX0                                                  |                                                                       | LCD_DA<br>TA23-B*1     | IRQ1         | AN109       |
| B7               |                                         | PD3      | D3[A3/D3]                        | MTIOC8D/<br>TOC2/POE8#                                      | RSPCKC-A                                                      | QIO3-B/SDHI_D3-<br>B/MMC_D3-B                                         | LCD_DA<br>TA21-B*1     | IRQ3         | AN111       |
| B8               |                                         | PD6      | D6[A6/D6]                        | MTIC5V/<br>MTIOC8A/<br>POE4#                                | SSLC2-A                                                       | QMO-B/QIO0-B/<br>SDHI_D0-B/<br>MMC_D0-B                               | LCD_DA<br>TA18-B*1     | IRQ6         | AN106       |
| B9               |                                         | PD7      | D7[A7/D7]                        | MTIC5U/<br>POE0#                                            | SSLC3-A                                                       | QMI-B/QIO1-B/<br>SDHI_D1-B/<br>MMC_D1-B                               | LCD_DA<br>TA17-B*1     | IRQ7         | AN107       |
| B10              |                                         | PE3      | D11[A11/<br>D11]/D3[A3/<br>D3]*1 | MTIOC4B/<br>PO26/TOC3/<br>POE8#                             | ET0_ERXD3/<br>CTS12#/<br>RTS12#/SS12#                         | MMC_D7-B                                                              | LCD_DA<br>TA13-B*1     |              | AN101       |
| C1               | VCL                                     |          |                                  |                                                             |                                                               |                                                                       |                        |              |             |
| C2               | AVSS1                                   |          |                                  |                                                             |                                                               |                                                                       |                        |              |             |
| C3               |                                         | PJ3      | EDACK1                           | MTIOC3C                                                     | ET0_EXOUT/<br>CTS6#/RTS6#/<br>SS6#/CTS0#/<br>RTS0#/SS0#       |                                                                       |                        |              |             |
| C4               | VREFH0                                  |          |                                  |                                                             |                                                               |                                                                       |                        |              |             |
| C5               |                                         | P42      |                                  |                                                             |                                                               |                                                                       |                        | IRQ10-<br>DS | AN002       |

**Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (2/5)**

| Pin Number       |                                         |          |                                  | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB) | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSI,<br>MMCIF) |                    |              |            |
|------------------|-----------------------------------------|----------|----------------------------------|-------------------------------------------------------------|------------------------------------------------------------|----------------------------------------------------------------------|--------------------|--------------|------------|
| 100-Pin<br>TFLGA | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC                    |                                                             |                                                            |                                                                      | GLCDC              | Interrupt    | A/D<br>D/A |
| C6               |                                         | P47      |                                  |                                                             |                                                            |                                                                      |                    | IRQ15-<br>DS | AN007      |
| C7               |                                         | PD2      | D2[A2/D2]                        | MTIOC4D/TIC2                                                | MISOC-A/CRX0                                               | QIO2-B/SDHI_D2-<br>B/MMC_D2-B                                        | LCD_DA<br>TA22-B*1 | IRQ2         | AN110      |
| C8               |                                         | PD5      | D5[A5/D5]                        | MTIC5W/<br>MTIOC8C/<br>POE10#                               | SSLC1-A                                                    | QSPCLK-B/<br>SDHI_CLK-B/<br>MMC_CLK-B                                | LCD_DA<br>TA19-B*1 | IRQ5         | AN113      |
| C9               |                                         | PE5      | D13[A13/<br>D13]/D5[A5/<br>D5]*1 | MTIOC4C/<br>MTIOC2B                                         | ET0_RX_CLK/<br>REF50CK0/<br>RSPCKB-B                       |                                                                      | LCD_DA<br>TA11-B*1 | IRQ5         | AN103      |
| C10              |                                         | PE4      | D12[A12/<br>D12]/D4[A4/<br>D4]*1 | MTIOC4D/<br>MTIOC1A/<br>PO28                                | ET0_ERXD2/<br>SSLB0-B                                      |                                                                      | LCD_DA<br>TA12-B*1 |              | AN102      |
| D1               | XCIN                                    |          |                                  |                                                             |                                                            |                                                                      |                    |              |            |
| D2               | XCOUT                                   |          |                                  |                                                             |                                                            |                                                                      |                    |              |            |
| D3               | MD/FINED                                |          |                                  |                                                             |                                                            |                                                                      |                    |              |            |
| D4               | VBATT                                   |          |                                  |                                                             |                                                            |                                                                      |                    |              |            |
| D5               |                                         | P45      |                                  |                                                             |                                                            |                                                                      |                    | IRQ13-<br>DS | AN005      |
| D6               |                                         | P46      |                                  |                                                             |                                                            |                                                                      |                    | IRQ14-<br>DS | AN006      |
| D7               |                                         | PE6      | D14[A14/<br>D14]/D6[A6/<br>D6]*1 | MTIOC6C/TIC1                                                | MOSIB-B                                                    | SDHI_CD/<br>MMC_CD-B                                                 | LCD_DA<br>TA10-B*1 | IRQ6         | AN104      |
| D8               |                                         | PE7      | D15[A15/<br>D15]/D7[A7/<br>D7]*1 | MTIOC6A/<br>TOC1                                            | MISOB-B                                                    | SDHI_WP/<br>MMC_RES#-B                                               | LCD_DA<br>TA9-B*1  | IRQ7         | AN105      |
| D9               |                                         | PA1      | A1                               | MTIOC0B/<br>MTCLKC/<br>MTIOC7B/<br>TIOC80/PO17              | ET0_WOL/<br>SCK5/SSLA2-B                                   |                                                                      | LCD_DA<br>TA7-B*1  | IRQ11        |            |
| D10              |                                         | PA0      | BC0#/A0                          | MTIOC4A/<br>MTIOC6D/<br>TIOCA0/PO16/<br>CACREF              | ET0_TX_EN/<br>RMII0_TXD_EN/<br>SSLA1-B                     |                                                                      | LCD_DA<br>TA8-B*1  |              |            |
| E1               | XTAL                                    | P37      |                                  |                                                             |                                                            |                                                                      |                    |              |            |
| E2               | VSS                                     |          |                                  |                                                             |                                                            |                                                                      |                    |              |            |
| E3               | RES#                                    |          |                                  |                                                             |                                                            |                                                                      |                    |              |            |
| E4               | TRST#                                   | P34      |                                  | MTIOC0A/<br>TMCI3/PO12/<br>POE10#                           | ET0_LINKSTA/<br>SCK6/SCK0                                  |                                                                      |                    | IRQ4         |            |
| E5               |                                         | P41      |                                  |                                                             |                                                            |                                                                      |                    | IRQ9-DS      | AN001      |
| E6               |                                         | PA2      | A2                               | MTIOC7A/<br>PO18                                            | RXD5/SMISO5/<br>SSCL5/SSLA3-B                              |                                                                      | LCD_DA<br>TA6-B*1  |              |            |
| E7               |                                         | PA6      | A6                               | MTIC5V/<br>MTCLKB/<br>TIOCA2/<br>TMCI3/PO22/<br>POE10#      | ET0_EXOUT/<br>CTS5#/RTS5#/<br>SS5#/MOSIA-B                 |                                                                      | LCD_DA<br>TA2-B*1  |              |            |
| E8               |                                         | PA4      | A4                               | MTIC5U/<br>MTCLKA/<br>TIOCA1/<br>TMRI0/PO20                 | ET0_MDC/TXD5/<br>SMOSI5/SSDA5/<br>SSLA0-B                  |                                                                      | LCD_DA<br>TA4-B*1  | IRQ5-DS      |            |
| E9               |                                         | PA5      | A5                               | MTIOC6B/<br>TIOC81/PO21                                     | ET0_LINKSTA/<br>RSPCKA-B                                   |                                                                      | LCD_DA<br>TA3-B*1  |              |            |
| E10              |                                         | PA3      | A3                               | MTIOC0D/<br>MTCLKD/<br>TIOC00/<br>TCLKB/PO19                | ET0_MDIO/<br>RXD5/SMISO5/<br>SSCL5                         |                                                                      | LCD_DA<br>TA5-B*1  | IRQ6-DS      |            |

**Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (3/5)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC)                 | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)                  | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSI,<br>MMCIF) | GLCDC             | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|---------------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------------|----------------------------------------------------------------------|-------------------|-----------|------------|
| F1         | EXTAL                                   | P36      |               |                                                                             |                                                                             |                                                                      |                   |           |            |
| F2         | VCC                                     |          |               |                                                                             |                                                                             |                                                                      |                   |           |            |
| F3         | UPSEL                                   | P35      |               |                                                                             |                                                                             |                                                                      |                   | NMI       |            |
| F4         |                                         | P32      |               | MTIOC0C/<br>TIOCC0/<br>TMO3/PO10/<br>RTCIC2/<br>RTCOUT/<br>POE0#/<br>POE10# | TXD6/SMOSI6/<br>SSDA6/TXD0/<br>SMOSI0/SSDA0/<br>CTX0/<br>USB0_VBUSEN        |                                                                      |                   | IRQ2-DS   |            |
| F5         |                                         | P12      |               | TMC11                                                                       | RXD2/SMISO2/<br>SSCL2/<br>SCL0[FM+]                                         |                                                                      |                   | IRQ2      |            |
| F6         |                                         | PB3      | A11           | MTIOC0A/<br>MTIOC4A/<br>TIOCD3/<br>TCLKD/TMO0/<br>PO27/POE11#               | ET0_RX_ER/<br>RMII0_RX_ER/<br>SCK6                                          | SDSI_D3-B                                                            | LCD_TC<br>ON1-B*1 |           |            |
| F7         |                                         | PB2      | A10           | TIOCC3/<br>TCLKC/PO26                                                       | ET0_RX_CLK/<br>REF50CK0/<br>CTS6#/RTS6#/<br>SS6#                            | SDSI_D2-B                                                            | LCD_TC<br>ON2-B*1 |           |            |
| F8         |                                         | PB0      | A8            | MTIC5W/<br>TIOCA3/PO24                                                      | ET0_ERXD1/<br>RMII0_RXD1/<br>RXD6/SMISO6/<br>SSCL6                          |                                                                      | LCD_DA<br>TA0-B*1 | IRQ12     |            |
| F9         |                                         | PA7      | A7            | TIOCB2/PO23                                                                 | ET0_WOL/<br>MISOA-B                                                         |                                                                      | LCD_DA<br>TA1-B*1 |           |            |
| F10        | VSS                                     |          |               |                                                                             |                                                                             |                                                                      |                   |           |            |
| G1         |                                         | P33      | EDREQ1        | MTIOC0D/<br>TIOCD0/<br>TMRI3/PO11/<br>POE4#/<br>POE11#                      | RXD6/SMISO6/<br>SSCL6/RXD0/<br>SMISO0/SSCL0/<br>CRX0                        |                                                                      |                   | IRQ3-DS   |            |
| G2         | TMS                                     | P31      |               | MTIOC4D/<br>TMC12/PO9/<br>RTCIC1                                            | CTS1#/RTS1#/<br>SS1#/SSLB0-A                                                |                                                                      |                   | IRQ1-DS   |            |
| G3         | TDI                                     | P30      |               | MTIOC4B/<br>TMRI3/PO8/<br>RTCIC0/<br>POE8#                                  | RXD1/SMISO1/<br>SSCL1/MISOB-A                                               |                                                                      |                   | IRQ0-DS   |            |
| G4         | TCK                                     | P27      | CS7#          | MTIOC2B/<br>TMC13/PO7                                                       | SCK1/RSPCKB-A                                                               |                                                                      |                   |           |            |
| G5         |                                         | P53*2    | BCLK          |                                                                             |                                                                             |                                                                      |                   |           |            |
| G6         |                                         | P52      | RD#           |                                                                             | RXD2/SMISO2/<br>SSCL2/SSLB3-A                                               |                                                                      |                   |           |            |
| G7         |                                         | PB5      | A13           | MTIOC2A/<br>MTIOC1B/<br>TIOCB4/<br>TMRI1/PO29/<br>POE4#                     | ET0_ETXD0/<br>RMII0_TXD0/<br>SCK9/SCK11                                     | SDSI_CLK-B                                                           | LCD_CL<br>K-B*1   |           |            |
| G8         |                                         | PB4      | A12           | TIOCA4/PO28                                                                 | ET0_TX_EN/<br>RMII0_TXD_EN/<br>CTS9#/RTS9#/<br>SS9#/SS11#/<br>CTS11#/RTS11# | SDSI_CMD-B                                                           | LCD_TC<br>ON0-B*1 |           |            |
| G9         |                                         | PB1      | A9            | MTIOC0C/<br>MTIOC4C/<br>TIOCB3/<br>TMC10/PO25                               | ET0_ERXD0/<br>RMII0_RXD0/<br>TXD6/SMOSI6/<br>SSDA6                          |                                                                      | LCD_TC<br>ON3-B*1 | IRQ4-DS   |            |
| G10        | VCC                                     |          |               |                                                                             |                                                                             |                                                                      |                   |           |            |

**Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (4/5)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC                       | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)                          | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)                                                          | Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF) | GLCDC | Interrupt | A/D D/A  |
|------------|-----------------------------------|----------|----------------------------------|--------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|-------|-----------|----------|
| H1         | TDO                               | P26      | CS6#                             | MTIOC2A/<br>TMO1/PO6                                                     | TXD1/SMOSI1/<br>SSDA1/CTS3#/<br>RTS3#/SS3#/<br>MOSIB-A                                                     |                                                              |       |           |          |
| H2         |                                   | P25      | CS5#/<br>EDACK1                  | MTIOC4C/<br>MTCLKB/<br>TIOCA4/PO5                                        | RXD3/SMISO3/<br>SSCL3                                                                                      |                                                              |       |           | ADTRG0 # |
| H3         |                                   | P16      |                                  | MTIOC3C/<br>MTIOC3D/<br>TIOCB1/<br>TCLKC/TMO2/<br>PO14/RTCOU             | TXD1/SMOSI1/<br>SSDA1/RXD3/<br>SMISO3/SSCL3/<br>SCL2-DS/<br>USB0_VBUSEN/<br>USB0_VBUS/<br>USB0_OVRCUR<br>B |                                                              |       | IRQ6      | ADTRG0 # |
| H4         |                                   | P15      |                                  | MTIOC0B/<br>MTCLKB/<br>TIOCB2/<br>TCLKB/TMC12/<br>PO13                   | RXD1/SMISO1/<br>SSCL1/SCK3/<br>CRX1-DS                                                                     |                                                              |       | IRQ5      |          |
| H5         |                                   | P55      | D0[A0/D0]*1/<br>WAIT#/<br>EDREQ0 | MTIOC4D/<br>TMO3                                                         | ET0_EXOUT/<br>CRX1                                                                                         |                                                              |       | IRQ10     |          |
| H6         |                                   | P54      | ALE/D1[A1/<br>D1]*1/<br>EDACK0   | MTIOC4B/<br>TMC11                                                        | ET0_LINKSTA/<br>CTS2#/RTS2#/<br>SS2#/CTX1                                                                  |                                                              |       |           |          |
| H7         | UB                                | PC7      | A23/CS0#                         | MTIOC3A/<br>MTCLKB/<br>TMO2/PO31/<br>TOC0/<br>CACREF                     | ET0_COL/TXD8/<br>SMOSI8/SSDA8/<br>SMOSI10/<br>SSDA10/TXD10/<br>MISOA-A                                     |                                                              |       | IRQ14     |          |
| H8         |                                   | PC6      | D2[A2/D2]*1/<br>A22/CS1#         | MTIOC3C/<br>MTCLKA/<br>TMC12/PO30/<br>TIC0                               | ET0_ETXD3/<br>RXD8/SMISO8/<br>SSCL8/<br>SMISO10/<br>SSCL10/RXD10/<br>MOSIA-A                               |                                                              |       | IRQ13     |          |
| H9         |                                   | PB6      | A14                              | MTIOC3D/<br>TIOCA5/PO30                                                  | ET0_ETXD1/<br>RMII0_TXD1/<br>RXD9/SMISO9/<br>SSCL9/<br>SMISO11/<br>SSCL11/RXD11                            | SDSI_D0-B                                                    |       |           |          |
| H10        |                                   | PB7      | A15                              | MTIOC3B/<br>TIOCB5/PO31                                                  | ET0_CRS/<br>RMII0_CRS_DV/<br>TXD9/SMISO9/<br>SSDA9/<br>SMISO11/<br>SSDA11/TXD11                            | SDSI_D1-B                                                    |       |           |          |
| J1         |                                   | P24      | CS4#/<br>EDREQ1                  | MTIOC4A/<br>MTCLKA/<br>TIOCB4/<br>TMRI1/PO4                              | SCK3/<br>USB0_VBUSEN                                                                                       |                                                              |       |           |          |
| J2         |                                   | P21      |                                  | MTIOC1B/<br>MTIOC4A/<br>TIOCA3/<br>TMC10/PO1                             | RXD0/SMISO0/<br>SSCL0/SCL1*1/<br>USB0_EXICEN                                                               |                                                              |       | IRQ9      |          |
| J3         |                                   | P17      |                                  | MTIOC3A/<br>MTIOC3B/<br>MTIOC4B/<br>TIOCB0/<br>TCLKD/TMO1/<br>PO15/POE8# | SCK1/TXD3/<br>SMOSI3/SSDA3/<br>SDA2-DS                                                                     |                                                              |       | IRQ7      | ADTRG1 # |
| J4         |                                   | P13      |                                  | MTIOC0B/<br>TIOCA5/TMO3/<br>PO13                                         | TXD2/SMOSI2/<br>SSDA2/<br>SDA0[FM+]                                                                        |                                                              |       | IRQ3      | ADTRG1 # |
| J5         | VSS_USB                           |          |                                  |                                                                          |                                                                                                            |                                                              |       |           |          |

**Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (5/5)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC                      | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)                   | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDI,<br>MMCIF) | GLCDC | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|------------------------------------|-------------------------------------------------------------|------------------------------------------------------------------------------|---------------------------------------------------------------------|-------|-----------|------------|
| J6         | VCC_USB                                 |          |                                    |                                                             |                                                                              |                                                                     |       |           |            |
| J7         |                                         | P50      | WR0#/WR#                           |                                                             | TXD2/SMOSI2/<br>SSDA2/SSLB1-A                                                |                                                                     |       |           |            |
| J8         |                                         | PC4      | A20/CS3#                           | MTIOC3D/<br>MTCLKC/<br>TMC11/PO25/<br>POE0#                 | ET0_TX_CLK/<br>SCK5/CTS8#/<br>RTS8#/SS8#/<br>SS10#/CTS10#/<br>RTS10#/SSLA0-A |                                                                     |       |           |            |
| J9         |                                         | PC0      | A16                                | MTIOC3C/<br>TCLKC/PO17                                      | ET0_ERXD3/<br>CTS5#/RTS5#/<br>SS5#/SSLA1-A                                   |                                                                     |       | IRQ14     |            |
| J10        |                                         | PC1      | A17                                | MTIOC3A/<br>TCLKD/PO18                                      | ET0_ERXD2/<br>SCK5/SSLA2-A                                                   |                                                                     |       | IRQ12     |            |
| K1         |                                         | P23      | EDACK0                             | MTIOC3D/<br>MTCLKD/<br>TIOC3/PO3                            | TXD3/SMOSI3/<br>SSDA3/CTS0#/<br>RTS0#/SS0#                                   |                                                                     |       |           |            |
| K2         |                                         | P22      | EDREQ0                             | MTIOC3B/<br>MTCLKC/<br>TIOC3/<br>TMO0/PO2                   | SCK0/<br>USB0_OVRCUR<br>B                                                    |                                                                     |       |           |            |
| K3         |                                         | P20      |                                    | MTIOC1A/<br>TIOCB3/<br>TMRI0/PO0                            | TXD0/SMOSI0/<br>SSDA0/SDA1*1/<br>USB0_ID                                     |                                                                     |       | IRQ8      |            |
| K4         |                                         | P14      |                                    | MTIOC3A/<br>MTCLKA/<br>TIOCB5/<br>TCLKA/TMRI2/<br>PO15      | CTS1#/RTS1#/<br>SS1#/CTX1/<br>USB0_OVRCUR<br>A                               |                                                                     |       | IRQ4      |            |
| K5         |                                         |          |                                    |                                                             | USB0_DM                                                                      |                                                                     |       |           |            |
| K6         |                                         |          |                                    |                                                             | USB0_DP                                                                      |                                                                     |       |           |            |
| K7         |                                         | P51      | WR1#/<br>BC1#/<br>WAIT#            |                                                             | SCK2/SSLB2-A                                                                 |                                                                     |       |           |            |
| K8         |                                         | PC5      | D3[A3/D3]*1/<br>A21/CS2#/<br>WAIT# | MTIOC3B/<br>MTCLKD/<br>TMRI2/PO29                           | ET0_ETXD2/<br>SCK8/SCK10/<br>RSPCKA-A                                        |                                                                     |       |           |            |
| K9         |                                         | PC3      | A19                                | MTIOC4D/<br>TCLKB/PO24                                      | ET0_TX_ER/<br>TXD5/SMOSI5/<br>SSDA5                                          |                                                                     |       |           |            |
| K10        |                                         | PC2      | A18                                | MTIOC4B/<br>TCLKA/PO21                                      | ET0_RX_DV/<br>RXD5/SMISO5/<br>SSCL5/SSLA3-A                                  |                                                                     |       |           |            |

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.

Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

## 1.6.6 100-Pin LFQFP

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (1/5)

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC      | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)                              | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)                    | Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF) | GLCDC | Interrupt | A/D D/A  |
|------------|-----------------------------------|----------|-----------------|------------------------------------------------------------------------------|----------------------------------------------------------------------|--------------------------------------------------------------|-------|-----------|----------|
| 1          | AVCC1                             |          |                 |                                                                              |                                                                      |                                                              |       |           |          |
| 2          | EMLE                              |          |                 |                                                                              |                                                                      |                                                              |       |           |          |
| 3          | AVSS1                             |          |                 |                                                                              |                                                                      |                                                              |       |           |          |
| 4          |                                   | PJ3      | EDACK1          | MTIOC3C                                                                      | ET0_EXOUT/<br>CTS6#/RTS6#/<br>SS6#/CTS0#/<br>RTS0#/SS0#              |                                                              |       |           |          |
| 5          | VCL                               |          |                 |                                                                              |                                                                      |                                                              |       |           |          |
| 6          | VBATT                             |          |                 |                                                                              |                                                                      |                                                              |       |           |          |
| 7          | MD/FINED                          |          |                 |                                                                              |                                                                      |                                                              |       |           |          |
| 8          | XCIN                              |          |                 |                                                                              |                                                                      |                                                              |       |           |          |
| 9          | XCOUT                             |          |                 |                                                                              |                                                                      |                                                              |       |           |          |
| 10         | RES#                              |          |                 |                                                                              |                                                                      |                                                              |       |           |          |
| 11         | XTAL                              | P37      |                 |                                                                              |                                                                      |                                                              |       |           |          |
| 12         | VSS                               |          |                 |                                                                              |                                                                      |                                                              |       |           |          |
| 13         | EXTAL                             | P36      |                 |                                                                              |                                                                      |                                                              |       |           |          |
| 14         | VCC                               |          |                 |                                                                              |                                                                      |                                                              |       |           |          |
| 15         | UPSEL                             | P35      |                 |                                                                              |                                                                      |                                                              |       | NMI       |          |
| 16         | TRST#                             | P34      |                 | MTIOC0A/<br>TMCI3/PO12/<br>POE10#                                            | ET0_LINKSTA/<br>SCK6/SCK0                                            |                                                              |       | IRQ4      |          |
| 17         |                                   | P33      | EDREQ1          | MTIOC0D/<br>TIOC0D/<br>TMRI3/PO11/<br>POE4#/<br>POE11#                       | RXD6/SMISO6/<br>SSCL6/RXD0/<br>SMISO0/SSCL0/<br>CRX0                 |                                                              |       | IRQ3-DS   |          |
| 18         |                                   | P32      |                 | MTIOC0C/<br>TIOCC0/<br>TMO3/PO10/<br>RTCIC2/<br>RTCCOUT/<br>POE0#/<br>POE10# | TXD6/SMOSI6/<br>SSDA6/TXD0/<br>SMOSI0/SSDA0/<br>CTX0/<br>USB0_VBUSEN |                                                              |       | IRQ2-DS   |          |
| 19         | TMS                               | P31      |                 | MTIOC4D/<br>TMCI2/PO9/<br>RTCIC1                                             | CTS1#/RTS1#/<br>SS1#/SSLB0-A                                         |                                                              |       | IRQ1-DS   |          |
| 20         | TDI                               | P30      |                 | MTIOC4B/<br>TMRI3/PO8/<br>RTCIC0/<br>POE8#                                   | RXD1/SMISO1/<br>SSCL1/MISOB-A                                        |                                                              |       | IRQ0-DS   |          |
| 21         | TCK                               | P27      | CS7#            | MTIOC2B/<br>TMCI3/PO7                                                        | SCK1/RSPCKB-A                                                        |                                                              |       |           |          |
| 22         | TDO                               | P26      | CS6#            | MTIOC2A/<br>TMO1/PO6                                                         | TXD1/SMOSI1/<br>SSDA1/CTS3#/<br>RTS3#/SS3#/<br>MOSIB-A               |                                                              |       |           |          |
| 23         |                                   | P25      | CS5#/<br>EDACK1 | MTIOC4C/<br>MTCLKB/<br>TIOCA4/PO5                                            | RXD3/SMISO3/<br>SSCL3                                                |                                                              |       |           | ADTRG0 # |
| 24         |                                   | P24      | CS4#/<br>EDREQ1 | MTIOC4A/<br>MTCLKA/<br>TIOCB4/<br>TMRI1/PO4                                  | SCK3/<br>USB0_VBUSEN                                                 |                                                              |       |           |          |

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (2/5)

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC                    | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC)              | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)                                                 | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF) | GLCDC | Interrupt | A/D<br>D/A  |
|------------|-----------------------------------------|----------|----------------------------------|--------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------|-------|-----------|-------------|
| 25         |                                         | P23      | EDACK0                           | MTIOC3D/<br>MTCLKD/<br>TIOCD3/PO3                                        | TXD3/SMOSI3/<br>SSDA3/CTS0#/<br>RTS0#/SS0#                                                                 |                                                                       |       |           |             |
| 26         |                                         | P22      | EDREQ0                           | MTIOC3B/<br>MTCLKC/<br>TIOCC3/<br>TMO0/PO2                               | SCK0/<br>USB0_OVRCUR<br>B                                                                                  |                                                                       |       |           |             |
| 27         |                                         | P21      |                                  | MTIOC1B/<br>MTIOC4A/<br>TIOCA3/<br>TMCI0/PO1                             | RXD0/SMISO0/<br>SSCL0/SCL1*1/<br>USB0_EXICEN                                                               |                                                                       |       | IRQ9      |             |
| 28         |                                         | P20      |                                  | MTIOC1A/<br>TIOCB3/<br>TMRI0/PO0                                         | TXD0/SMOSI0/<br>SSDA0/SDA1*1/<br>USB0_ID                                                                   |                                                                       |       | IRQ8      |             |
| 29         |                                         | P17      |                                  | MTIOC3A/<br>MTIOC3B/<br>MTIOC4B/<br>TIOCB0/<br>TCLKD/TMO1/<br>PO15/POE8# | SCK1/TXD3/<br>SMOSI3/SSDA3/<br>SDA2-DS                                                                     |                                                                       |       | IRQ7      | ADTRG1<br># |
| 30         |                                         | P16      |                                  | MTIOC3C/<br>MTIOC3D/<br>TIOCB1/<br>TCLKC/TMO2/<br>PO14/RTCOU             | TXD1/SMOSI1/<br>SSDA1/RXD3/<br>SMISO3/SSCL3/<br>SCL2-DS/<br>USB0_VBUSEN/<br>USB0_VBUS/<br>USB0_OVRCUR<br>B |                                                                       |       | IRQ6      | ADTRG0<br># |
| 31         |                                         | P15      |                                  | MTIOC0B/<br>MTCLKB/<br>TIOCB2/<br>TCLKB/TMC12/<br>PO13                   | RXD1/SMISO1/<br>SSCL1/SCK3/<br>CRX1-DS                                                                     |                                                                       |       | IRQ5      |             |
| 32         |                                         | P14      |                                  | MTIOC3A/<br>MTCLKA/<br>TIOCB5/<br>TCLKA/TMRI2/<br>PO15                   | CTS1#/RTS1#/<br>SS1#/CTX1/<br>USB0_OVRCUR<br>A                                                             |                                                                       |       | IRQ4      |             |
| 33         |                                         | P13      |                                  | MTIOC0B/<br>TIOCA5/TMO3/<br>PO13                                         | TXD2/SMOSI2/<br>SSDA2/<br>SDA0[FM+]                                                                        |                                                                       |       | IRQ3      | ADTRG1<br># |
| 34         |                                         | P12      |                                  | TMC11                                                                    | RXD2/SMISO2/<br>SSCL2/<br>SCL0[FM+]                                                                        |                                                                       |       | IRQ2      |             |
| 35         | VCC_USB                                 |          |                                  |                                                                          |                                                                                                            |                                                                       |       |           |             |
| 36         |                                         |          |                                  |                                                                          | USB0_DM                                                                                                    |                                                                       |       |           |             |
| 37         |                                         |          |                                  |                                                                          | USB0_DP                                                                                                    |                                                                       |       |           |             |
| 38         | VSS_USB                                 |          |                                  |                                                                          |                                                                                                            |                                                                       |       |           |             |
| 39         |                                         | P55      | D0[A0/D0]*1/<br>WAIT#/<br>EDREQ0 | MTIOC4D/<br>TMO3                                                         | ET0_EXOUT/<br>CRX1                                                                                         |                                                                       |       | IRQ10     |             |
| 40         |                                         | P54      | ALE/D1[A1/<br>D1]*1/<br>EDACK0   | MTIOC4B/<br>TMC11                                                        | ET0_LINKSTA/<br>CTS2#/RTS2#/<br>SS2#/CTX1                                                                  |                                                                       |       |           |             |
| 41         |                                         | P53*2    | BCLK                             |                                                                          |                                                                                                            |                                                                       |       |           |             |
| 42         |                                         | P52      | RD#                              |                                                                          | RXD2/SMISO2/<br>SSCL2/SSLB3-A                                                                              |                                                                       |       |           |             |
| 43         |                                         | P51      | WR1#/<br>BC1#/<br>WAIT#          |                                                                          | SCK2/SSLB2-A                                                                                               |                                                                       |       |           |             |
| 44         |                                         | P50      | WR0#/WR#                         |                                                                          | TXD2/SMOSI2/<br>SSDA2/SSLB1-A                                                                              |                                                                       |       |           |             |

**Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (3/5)**

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC                      | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC)  | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)                      | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF) | GLCDC             | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|------------------------------------|--------------------------------------------------------------|---------------------------------------------------------------------------------|-----------------------------------------------------------------------|-------------------|-----------|------------|
| 45         | UB                                      | PC7      | A23/CS0#                           | MTIOC3A/<br>MTCLKB/<br>TMO2/PO31/<br>TOC0/<br>CACREF         | ET0_COL/TXD8/<br>SMOSI8/SSDA8/<br>SMOSI10/<br>SSDA10/TXD10/<br>MISOA-A          |                                                                       |                   | IRQ14     |            |
| 46         |                                         | PC6      | D2[A2/D2]*1/<br>A22/CS1#           | MTIOC3C/<br>MTCLKA/<br>TMCI2/PO30/<br>TIC0                   | ET0_ETXD3/<br>RXD8/SMISO8/<br>SSCL8/<br>SMISO10/<br>SSCL10/RXD10/<br>MOSIA-A    |                                                                       |                   | IRQ13     |            |
| 47         |                                         | PC5      | D3[A3/D3]*1/<br>A21/CS2#/<br>WAIT# | MTIOC3B/<br>MTCLKD/<br>TMRI2/PO29                            | ET0_ETXD2/<br>SCK8/SCK10/<br>RSPCKA-A                                           |                                                                       |                   |           |            |
| 48         |                                         | PC4      | A20/CS3#                           | MTIOC3D/<br>MTCLKC/<br>TMCI1/PO25/<br>POE0#                  | ET0_TX_CLK/<br>SCK5/CTS8#/<br>RTS8#/SS8#/<br>SS10#/CTS10#/<br>RTS10#/SSLA0-A    |                                                                       |                   |           |            |
| 49         |                                         | PC3      | A19                                | MTIOC4D/<br>TCLKB/PO24                                       | ET0_TX_ER/<br>TXD5/SMOSI5/<br>SSDA5                                             |                                                                       |                   |           |            |
| 50         |                                         | PC2      | A18                                | MTIOC4B/<br>TCLKA/PO21                                       | ET0_RX_DV/<br>RXD5/SMISO5/<br>SSCL5/SSLA3-A                                     |                                                                       |                   |           |            |
| 51         |                                         | PC1      | A17                                | MTIOC3A/<br>TCLKD/PO18                                       | ET0_ERXD2/<br>SCK5/SSLA2-A                                                      |                                                                       |                   | IRQ12     |            |
| 52         |                                         | PC0      | A16                                | MTIOC3C/<br>TCLKC/PO17                                       | ET0_ERXD3/<br>CTS5#/RTS5#/<br>SS5#/SSLA1-A                                      |                                                                       |                   | IRQ14     |            |
| 53         |                                         | PB7      | A15                                | MTIOC3B/<br>TIOCB5/PO31                                      | ET0_CRS/<br>RMII0_CRS_DV/<br>TXD9/SMOSI9/<br>SSDA9/<br>SMOSI11/<br>SSDA11/TXD11 | SDSI_D1-B                                                             |                   |           |            |
| 54         |                                         | PB6      | A14                                | MTIOC3D/<br>TIOCA5/PO30                                      | ET0_ETXD1/<br>RMII0_TXD1/<br>RXD9/SMISO9/<br>SSCL9/<br>SMISO11/<br>SSCL11/RXD11 | SDSI_D0-B                                                             |                   |           |            |
| 55         |                                         | PB5      | A13                                | MTIOC2A/<br>MTIOC1B/<br>TIOCB4/<br>TMRI1/PO29/<br>POE4#      | ET0_ETXD0/<br>RMII0_TXD0/<br>SCK9/SCK11                                         | SDSI_CLK-B                                                            | LCD_CLK-B*1       |           |            |
| 56         |                                         | PB4      | A12                                | TIOCA4/PO28                                                  | ET0_TX_EN/<br>RMII0_TXD_EN/<br>CTS9#/RTS9#/<br>SS9#/SS11#/<br>CTS11#/RTS11#     | SDSI_CMD-B                                                            | LCD_TC<br>ON0-B*1 |           |            |
| 57         |                                         | PB3      | A11                                | MTIOC0A/<br>MTIOC4A/<br>TIOC3/<br>TCLKD/TMO0/<br>PO27/POE11# | ET0_RX_ER/<br>RMII0_RX_ER/<br>SCK6                                              | SDSI_D3-B                                                             | LCD_TC<br>ON1-B*1 |           |            |
| 58         |                                         | PB2      | A10                                | TIOCC3/<br>TCLKC/PO26                                        | ET0_RX_CLK/<br>REF50CK0/<br>CTS6#/RTS6#/<br>SS6#                                | SDSI_D2-B                                                             | LCD_TC<br>ON2-B*1 |           |            |
| 59         |                                         | PB1      | A9                                 | MTIOC0C/<br>MTIOC4C/<br>TIOCB3/<br>TMCI0/PO25                | ET0_ERXD0/<br>RMII0_RXD0/<br>TXD6/SMOSI6/<br>SSDA6                              |                                                                       | LCD_TC<br>ON3-B*1 | IRQ4-DS   |            |

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (4/5)

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC                    | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB)     | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSI,<br>MMCIF) | GLCDC              | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|----------------------------------|-------------------------------------------------------------|----------------------------------------------------------------|----------------------------------------------------------------------|--------------------|-----------|------------|
| 60         | VCC                                     |          |                                  |                                                             |                                                                |                                                                      |                    |           |            |
| 61         |                                         | PB0      | A8                               | MTIC5W/<br>TIOCA3/PO24                                      | ET0_ERXD1/<br>RMII0_RXD1/<br>RXD6/SMISO6/<br>SSCL6             |                                                                      | LCD_DA<br>TA0-B*1  | IRQ12     |            |
| 62         | VSS                                     |          |                                  |                                                             |                                                                |                                                                      |                    |           |            |
| 63         |                                         | PA7      | A7                               | TIOCB2/PO23                                                 | ET0_WOL/<br>MISOA-B                                            |                                                                      | LCD_DA<br>TA1-B*1  |           |            |
| 64         |                                         | PA6      | A6                               | MTIC5V/<br>MTCLKB/<br>TIOCA2/<br>TMCI3/PO22/<br>POE10#      | ET0_EXOUT/<br>CTS5#/RTS5#/<br>SS5#/MOSIA-B                     |                                                                      | LCD_DA<br>TA2-B*1  |           |            |
| 65         |                                         | PA5      | A5                               | MTIOC6B/<br>TIOCB1/PO21                                     | ET0_LINKSTA/<br>RSPCKA-B                                       |                                                                      | LCD_DA<br>TA3-B*1  |           |            |
| 66         |                                         | PA4      | A4                               | MTIC5U/<br>MTCLKA/<br>TIOCA1/<br>TMRI0/PO20                 | ET0_MDC/TXD5/<br>SMOSI5/SSDA5/<br>SSLA0-B                      |                                                                      | LCD_DA<br>TA4-B*1  | IRQ5-DS   |            |
| 67         |                                         | PA3      | A3                               | MTIOC0D/<br>MTCLKD/<br>TIOC0D/<br>TCLKB/PO19                | ET0_MDIO/<br>RXD5/SMISO5/<br>SSCL5                             |                                                                      | LCD_DA<br>TA5-B*1  | IRQ6-DS   |            |
| 68         |                                         | PA2      | A2                               | MTIOC7A/<br>PO18                                            | RXD5/SMISO5/<br>SSCL5/SSLA3-B                                  |                                                                      | LCD_DA<br>TA6-B*1  |           |            |
| 69         |                                         | PA1      | A1                               | MTIOC0B/<br>MTCLKC/<br>MTIOC7B/<br>TIOCB0/PO17              | ET0_WOL/<br>SCK5/SSLA2-B                                       |                                                                      | LCD_DA<br>TA7-B*1  | IRQ11     |            |
| 70         |                                         | PA0      | BC0#/A0                          | MTIOC4A/<br>MTIOC6D/<br>TIOCA0/PO16/<br>CACREF              | ET0_TX_EN/<br>RMII0_TXD_EN/<br>SSLA1-B                         |                                                                      | LCD_DA<br>TA8-B*1  |           |            |
| 71         |                                         | PE7      | D15[A15/<br>D15]/D7[A7/<br>D7]*1 | MTIOC6A/<br>TOC1                                            | MISOB-B                                                        | SDHI_WP/<br>MMC_RES#-B                                               | LCD_DA<br>TA9-B*1  | IRQ7      | AN105      |
| 72         |                                         | PE6      | D14[A14/<br>D14]/D6[A6/<br>D6]*1 | MTIOC6C/TIC1                                                | MOSIB-B                                                        | SDHI_CD/<br>MMC_CD-B                                                 | LCD_DA<br>TA10-B*1 | IRQ6      | AN104      |
| 73         |                                         | PE5      | D13[A13/<br>D13]/D5[A5/<br>D5]*1 | MTIOC4C/<br>MTIOC2B                                         | ET0_RX_CLK/<br>REF50CK0/<br>RSPCKB-B                           |                                                                      | LCD_DA<br>TA11-B*1 | IRQ5      | AN103      |
| 74         |                                         | PE4      | D12[A12/<br>D12]/D4[A4/<br>D4]*1 | MTIOC4D/<br>MTIOC1A/<br>PO28                                | ET0_ERXD2/<br>SSLB0-B                                          |                                                                      | LCD_DA<br>TA12-B*1 |           | AN102      |
| 75         |                                         | PE3      | D11[A11/<br>D11]/D3[A3/<br>D3]*1 | MTIOC4B/<br>PO26/TOC3/<br>POE8#                             | ET0_ERXD3/<br>CTS12#/<br>RTS12#/SS12#                          | MMC_D7-B                                                             | LCD_DA<br>TA13-B*1 |           | AN101      |
| 76         |                                         | PE2      | D10[A10/<br>D10]/D2[A2/<br>D2]*1 | MTIOC4A/<br>PO23/TIC3                                       | RXD12/<br>SMISO12/<br>SSCL12/<br>RXDX12/SSLB3-<br>B            | MMC_D6-B                                                             | LCD_DA<br>TA14-B*1 | IRQ7-DS   | AN100      |
| 77         |                                         | PE1      | D9[A9/D9]/<br>D1[A1/D1]*1        | MTIOC4C/<br>MTIOC3B/<br>PO18                                | TXD12/<br>SMOSI12/<br>SSDA12/<br>TXDX12/<br>SIOX12/SSLB2-<br>B | MMC_D5-B                                                             | LCD_DA<br>TA15-B*1 |           | ANEX1      |
| 78         |                                         | PE0      | D8[A8/D8]/<br>D0[A0/D0]*1        | MTIOC3D                                                     | SCK12/SSLB1-B                                                  | MMC_D4-B                                                             | LCD_DA<br>TA16-B*1 |           | ANEX0      |

**Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (5/5)**

| Pin Number      |                                         |          |               | Timer<br>(MTU, TPU,<br>TMR, PPG,<br>RTC, CMTW,<br>POE, CAC) | Communication<br>(ETHERC, SCI,<br>RSPI, RIIC,<br>CAN, USB) | Memory Interface<br>Camera Interface<br>(QSPI, SDHI, SDSDI,<br>MMCIF) |                        |              |             |
|-----------------|-----------------------------------------|----------|---------------|-------------------------------------------------------------|------------------------------------------------------------|-----------------------------------------------------------------------|------------------------|--------------|-------------|
| 100-Pin<br>LQFP | Power Supply<br>Clock System<br>Control | I/O Port | Bus<br>EXDMAC |                                                             |                                                            |                                                                       | GLCDC                  | Interrupt    | A/D<br>D/A  |
| 79              |                                         | PD7      | D7[A7/D7]     | MTIC5U/<br>POE0#                                            | SSLC3-A                                                    | QMI-B/QIO1-B/<br>SDHI_D1-B/<br>MMC_D1-B                               | LCD_DA<br>TA17-B*1     | IRQ7         | AN107       |
| 80              |                                         | PD6      | D6[A6/D6]     | MTIC5V/<br>MTIOC8A/<br>POE4#                                | SSLC2-A                                                    | QMO-B/QIO0-B/<br>SDHI_D0-B/<br>MMC_D0-B                               | LCD_DA<br>TA18-B*1     | IRQ6         | AN106       |
| 81              |                                         | PD5      | D5[A5/D5]     | MTIC5W/<br>MTIOC8C/<br>POE10#                               | SSLC1-A                                                    | QSPCLK-B/<br>SDHI_CLK-B/<br>MMC_CLK-B                                 | LCD_DA<br>TA19-B*1     | IRQ5         | AN113       |
| 82              |                                         | PD4      | D4[A4/D4]     | MTIOC8B/<br>POE11#                                          | SSLC0-A                                                    | QSSL-B/<br>SDHI_CMD-B/<br>MMC_CMD-B                                   | LCD_DA<br>TA20-B*1     | IRQ4         | AN112       |
| 83              |                                         | PD3      | D3[A3/D3]     | MTIOC8D/<br>TOC2/POE8#                                      | RSPCKC-A                                                   | QIO3-B/SDHI_D3-<br>B/MMC_D3-B                                         | LCD_DA<br>TA21-B*1     | IRQ3         | AN111       |
| 84              |                                         | PD2      | D2[A2/D2]     | MTIOC4D/TIC2                                                | MISOC-A/CRX0                                               | QIO2-B/SDHI_D2-<br>B/MMC_D2-B                                         | LCD_DA<br>TA22-B*1     | IRQ2         | AN110       |
| 85              |                                         | PD1      | D1[A1/D1]     | MTIOC4B/<br>POE0#                                           | MOSIC-A/CTX0                                               |                                                                       | LCD_DA<br>TA23-B*1     | IRQ1         | AN109       |
| 86              |                                         | PD0      | D0[A0/D0]     | POE4#                                                       |                                                            |                                                                       | LCD_EX<br>TCLK-B<br>*1 | IRQ0         | AN108       |
| 87              |                                         | P47      |               |                                                             |                                                            |                                                                       |                        | IRQ15-<br>DS | AN007       |
| 88              |                                         | P46      |               |                                                             |                                                            |                                                                       |                        | IRQ14-<br>DS | AN006       |
| 89              |                                         | P45      |               |                                                             |                                                            |                                                                       |                        | IRQ13-<br>DS | AN005       |
| 90              |                                         | P44      |               |                                                             |                                                            |                                                                       |                        | IRQ12-<br>DS | AN004       |
| 91              |                                         | P43      |               |                                                             |                                                            |                                                                       |                        | IRQ11-<br>DS | AN003       |
| 92              |                                         | P42      |               |                                                             |                                                            |                                                                       |                        | IRQ10-<br>DS | AN002       |
| 93              |                                         | P41      |               |                                                             |                                                            |                                                                       |                        | IRQ9-DS      | AN001       |
| 94              | VREFL0                                  |          |               |                                                             |                                                            |                                                                       |                        |              |             |
| 95              |                                         | P40      |               |                                                             |                                                            |                                                                       |                        | IRQ8-DS      | AN000       |
| 96              | VREFH0                                  |          |               |                                                             |                                                            |                                                                       |                        |              |             |
| 97              | AVCC0                                   |          |               |                                                             |                                                            |                                                                       |                        |              |             |
| 98              |                                         | P07      |               |                                                             |                                                            |                                                                       |                        | IRQ15        | ADTRG0<br># |
| 99              | AVSS0                                   |          |               |                                                             |                                                            |                                                                       |                        |              |             |
| 100             |                                         | P05      |               |                                                             |                                                            |                                                                       |                        | IRQ13        | DA1         |

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.

Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

## 1.6.7 64-Pin TFBGA

Table 1.11 List of Pin and Pin Functions (64-Pin TFBGA) (1/2)

| Pin Number   |                                   |          | Timer                                | Communication             | Memory Interface       |           |         |
|--------------|-----------------------------------|----------|--------------------------------------|---------------------------|------------------------|-----------|---------|
| 64-Pin TFBGA | Power Supply Clock System Control | I/O Port | (MTU, TPU, TMR, RTC, CMTW, POE, CAC) | (SCI, RSPI, RIIC, USB)    | (QSPI, SDHI)           | Interrupt | A/D D/A |
| A1           | AVCC1                             |          |                                      |                           |                        |           |         |
| A2           | AVSS0                             |          |                                      |                           |                        |           |         |
| A3           | VREFH0                            |          |                                      |                           |                        |           |         |
| A4           | VREFL0                            |          |                                      |                           |                        |           |         |
| A5           |                                   | PD2      | MTIOC4D/TIC2                         |                           | QIO2-B/SDHI_D2-B       | IRQ2      | AN110   |
| A6           |                                   | PD7      | MTIC5U/POE0#                         |                           | QMI-B/QIO1-B/SDHI_D1-B | IRQ7      | AN107   |
| A7           |                                   | PE0      | MTIOC3D                              | SCK12                     |                        |           | ANEX0   |
| A8           |                                   | PE2      | MTIOC4A/TIC3                         | RXD12/SSCL12/RXD12        |                        | IRQ7-DS   |         |
| B1           | EMLE                              |          |                                      |                           |                        |           |         |
| B2           | AVSS1                             |          |                                      |                           |                        |           |         |
| B3           | AVCC0                             |          |                                      |                           |                        |           |         |
| B4           |                                   | P42      |                                      |                           |                        | IRQ10-DS  | AN002   |
| B5           |                                   | PD3      | MTIOC8D/TOC2/POE8#                   |                           | QIO3-B/SDHI_D3-B       | IRQ3      | AN111   |
| B6           |                                   | PD6      | MTIC5V/MTIOC8A/POE4#                 |                           | QMO-B/QIO0-B/SDHI_D0-B | IRQ6      | AN106   |
| B7           |                                   | PE1      | MTIOC4C/MTIOC3B                      | TXD12/SSDA12/TXD12/SIOX12 |                        |           | ANEX1   |
| B8           |                                   | PE6      | MTIOC6C/TIC1                         |                           | SDHI_CD                | IRQ6      |         |
| C1           | VCL                               |          |                                      |                           |                        |           |         |
| C2           | VBATT                             |          |                                      |                           |                        |           |         |
| C3           | MD/FINED                          |          |                                      |                           |                        |           |         |
| C4           |                                   | P41      |                                      |                           |                        | IRQ9-DS   | AN001   |
| C5           |                                   | PD4      | MTIOC8B/POE11#                       |                           | QSSL-B/SDHI_CMD-B      | IRQ4      | AN112   |
| C6           |                                   | PD5      | MTIC5W/MTIOC8C/POE10#                |                           | QSPCLK-B/SDHI_CLK-B    | IRQ5      | AN113   |
| C7           |                                   | PA1      | MTIOC0B/MTCLKC/MTIOC7B/TIOCB0        | SCK5                      |                        | IRQ11     |         |
| C8           |                                   | PE7      | MTIOC6A/TOC1                         |                           | SDHI_WP                | IRQ7      |         |
| D1           | XCIN                              |          |                                      |                           |                        |           |         |
| D2           | XCOUT                             |          |                                      |                           |                        |           |         |
| D3           | RES#                              |          |                                      |                           |                        |           |         |
| D4           |                                   | P40      |                                      |                           |                        | IRQ8-DS   | AN000   |
| D5           |                                   | P43      |                                      |                           |                        | IRQ11-DS  | AN003   |
| D6           |                                   | PA6      | MTIC5V/MTCLKB/TIOCA2/TMC13/POE10#    | CTS5#/RTS5#/SS5#          |                        |           |         |
| D7           |                                   | PA2      | MTIOC7A                              | RXD5/SMISO5/SSCL5         |                        |           |         |
| D8           |                                   | PA4      | MTIC5U/MTCLKA/TIOCA1/TMR10           | TXD5/SMOSI5/SSDA5         |                        | IRQ5-DS   |         |
| E1           | XTAL                              | P37      |                                      |                           |                        |           |         |
| E2           | VSS                               |          |                                      |                           |                        |           |         |
| E3           | TRST#                             | P34      | MTIOC0A/TMC13/POE10#                 |                           |                        | IRQ4      |         |

Table 1.11 List of Pin and Pin Functions (64-Pin TFBGA) (2/2)

| Pin Number   |                                         |          | Timer                                                       | Communication                                              | Memory Interface |           |            |
|--------------|-----------------------------------------|----------|-------------------------------------------------------------|------------------------------------------------------------|------------------|-----------|------------|
| 64-Pin TFBGA | Power Supply<br>Clock System<br>Control | I/O Port | (MTU, TPU, TMR,<br>RTC, CMTW, POE,<br>CAC)                  | (SCI, RSPI, RIIC,<br>USB)                                  | (QSPI, SDHI)     | Interrupt | A/D<br>D/A |
| E4           |                                         | P13      | MTIOC0B/TIOCA5/<br>TMO3                                     | TXD2/SSDA2/<br>SDA0[FM+]                                   |                  | IRQ3      | ADTRG1#    |
| E5           | BSCANP                                  |          |                                                             |                                                            |                  |           |            |
| E6           |                                         | PA7      | TIOCB2                                                      |                                                            |                  |           |            |
| E7           | VCC                                     |          |                                                             |                                                            |                  |           |            |
| E8           | VSS                                     |          |                                                             |                                                            |                  |           |            |
| F1           | EXTAL                                   | P36      |                                                             |                                                            |                  |           |            |
| F2           | VCC                                     |          |                                                             |                                                            |                  |           |            |
| F3           | UPSEL                                   | P35      |                                                             |                                                            |                  | NMI       |            |
| F4           |                                         | P12      | TMC11                                                       | RXD2/SSCL2/<br>SCL0[FM+]                                   |                  | IRQ2      |            |
| F5           |                                         | P53      |                                                             |                                                            |                  |           |            |
| F6           |                                         | PB7      | MTIOC3B/TIOCB5                                              | TXD9/SSDA9/<br>SSDA11/TXD11                                |                  |           |            |
| F7           |                                         | PB6      | MTIOC3D/TIOCA5                                              | RXD9/SSCL9/<br>SSCL11/RXD11                                |                  |           |            |
| F8           |                                         | PB5      | MTIOC2A/MTIOC1B/<br>TIOCB4/TMRI1/<br>POE4#                  | SCK9/SCK11                                                 |                  |           |            |
| G1           | TCK                                     | P27      | MTIOC2B/TMC13                                               | SCK1/RSPCKB-A                                              |                  |           |            |
| G2           | TMS                                     | P31      | MTIOC4D/TMC12/<br>RTCIC1                                    | CTS1#/RTS1#/SS1#/<br>SSLB0-A                               |                  | IRQ1-DS   |            |
| G3           | TDI                                     | P30      | MTIOC4B/TMRI3/<br>RTCIC0/POE8#                              | RXD1/SMISO1/<br>SSCL1/MISOB-A                              |                  | IRQ0-DS   |            |
| G4           | VCC_USB                                 |          |                                                             |                                                            |                  |           |            |
| G5           | VSS_USB                                 |          |                                                             |                                                            |                  |           |            |
| G6           | UB                                      | PC7      | MTIOC3A/MTCLKB/<br>TMO2/TOC0/<br>CACREF                     | TXD8/SMOSI8/<br>SSDA8/SMOSI10/<br>SSDA10/TXD10/<br>MISOA-A |                  | IRQ14     |            |
| G7           |                                         | PC5      | MTIOC3B/MTCLKD/<br>TMRI2                                    | SCK8/SCK10/<br>RSPCKA-A                                    |                  |           |            |
| G8           |                                         | PC0      | MTIOC3C/TCLKC                                               | SSLA1-A                                                    |                  | IRQ14     |            |
| H1           | TDO                                     | P26      | MTIOC2A/TMO1                                                | TXD1/SMOSI1/<br>SSDA1/CTS3#/<br>RTS3#/MOSIB-A              |                  |           |            |
| H2           |                                         | P17      | MTIOC3A/MTIOC3B/<br>MTIOC4B/TIOCB0/<br>TCLKD/TMO1/<br>POE8# | SCK1/TXD3/SSDA3/<br>SDA2-DS                                |                  | IRQ7      | ADTRG1#    |
| H3           |                                         | P16      | MTIOC3C/MTIOC3D/<br>TIOCB1/TCLKC/<br>TMO2/RTCOUT            | TXD1/SMOSI1/<br>SSDA1/RXD3/<br>SSCL3/SCL2-DS/<br>USB0_VBUS |                  | IRQ6      | ADTRG0#    |
| H4           |                                         |          |                                                             | USB0_DM                                                    |                  |           |            |
| H5           |                                         |          |                                                             | USB0_DP                                                    |                  |           |            |
| H6           |                                         | PC6      | MTIOC3C/MTCLKA/<br>TMC12/TIC0                               | RXD8/SMISO8/<br>SSCL8/SMISO10/<br>SSCL10/RXD10/<br>MOSIA-A |                  | IRQ13     |            |
| H7           |                                         | PC4      | MTIOC3D/MTCLKC/<br>TMC11/POE0#                              | CTS8#/RTS8#/SS8#/<br>SS10#/CTS10#/<br>RTS10#/SSLA0-A       |                  |           |            |
| H8           |                                         | PC1      | MTIOC3A/TCLKD                                               | SSLA2-A                                                    |                  | IRQ12     |            |

## 1.6.8 64-Pin LFQFP

Table 1.12 List of Pin and Pin Functions (64-Pin LFQFP) (1/2)

| Pin Number | Power Supply<br>Clock System<br>Control | I/O Port | Timer<br>(MTU, TPU, TMR,<br>RTC, CMTW, POE,<br>CAC)         | Communication<br>(SCI, RSPI, RIIC,<br>USB)                 | Memory Interface<br>(QSPI, SDHI) | Interrupt | A/D<br>D/A |
|------------|-----------------------------------------|----------|-------------------------------------------------------------|------------------------------------------------------------|----------------------------------|-----------|------------|
| 1          | AVCC1                                   |          |                                                             |                                                            |                                  |           |            |
| 2          | EMLE                                    |          |                                                             |                                                            |                                  |           |            |
| 3          | AVSS1                                   |          |                                                             |                                                            |                                  |           |            |
| 4          | VCL                                     |          |                                                             |                                                            |                                  |           |            |
| 5          | VBATT                                   |          |                                                             |                                                            |                                  |           |            |
| 6          | MD/FINED                                |          |                                                             |                                                            |                                  |           |            |
| 7          | XCIN                                    |          |                                                             |                                                            |                                  |           |            |
| 8          | XCOUT                                   |          |                                                             |                                                            |                                  |           |            |
| 9          | RES#                                    |          |                                                             |                                                            |                                  |           |            |
| 10         | XTAL                                    | P37      |                                                             |                                                            |                                  |           |            |
| 11         | VSS                                     |          |                                                             |                                                            |                                  |           |            |
| 12         | EXTAL                                   | P36      |                                                             |                                                            |                                  |           |            |
| 13         | VCC                                     |          |                                                             |                                                            |                                  |           |            |
| 14         | UPSEL                                   | P35      |                                                             |                                                            |                                  | NMI       |            |
| 15         | TRST#                                   | P34      | MTIOC0A/TMC13/<br>POE10#                                    |                                                            |                                  | IRQ4      |            |
| 16         | TDI                                     | P30      | MTIOC4B/TMR13/<br>RTCIC0/POE8#                              | RXD1/SMISO1/<br>SSCL1/MISOB-A                              |                                  | IRQ0-DS   |            |
| 17         | TMS                                     | P31      | MTIOC4D/TMC12/<br>RTCIC1                                    | CTS1#/RTS1#/SS1#/<br>SSLB0-A                               |                                  | IRQ1-DS   |            |
| 18         | TDO                                     | P26      | MTIOC2A/TMO1                                                | TXD1/SMOSI1/<br>SSDA1/CTS3#/<br>RTS3#/MOSIB-A              |                                  |           |            |
| 19         | TCK                                     | P27      | MTIOC2B/TMC13                                               | SCK1/RSPCKB-A                                              |                                  |           |            |
| 20         |                                         | P17      | MTIOC3A/MTIOC3B/<br>MTIOC4B/TIOCB0/<br>TCLKD/TMO1/<br>POE8# | SCK1/TXD3/SSDA3/<br>SDA2-DS                                |                                  | IRQ7      | ADTRG1#    |
| 21         |                                         | P16      | MTIOC3C/MTIOC3D/<br>TIOCB1/TCLKC/<br>TMO2/RTCOUT            | TXD1/SMOSI1/<br>SSDA1/RXD3/<br>SSCL3/SCL2-DS/<br>USB0_VBUS |                                  | IRQ6      | ADTRG0#    |
| 22         |                                         | P13      | MTIOC0B/TIOCA5/<br>TMO3                                     | TXD2/SSDA2/<br>SDA0[FM+]                                   |                                  | IRQ3      | ADTRG1#    |
| 23         |                                         | P12      | TMC11                                                       | RXD2/SSCL2/<br>SCL0[FM+]                                   |                                  | IRQ2      |            |
| 24         | VCC_USB                                 |          |                                                             |                                                            |                                  |           |            |
| 25         |                                         |          |                                                             | USB0_DM                                                    |                                  |           |            |
| 26         |                                         |          |                                                             | USB0_DP                                                    |                                  |           |            |
| 27         | VSS_USB                                 |          |                                                             |                                                            |                                  |           |            |
| 28         |                                         | P53      |                                                             |                                                            |                                  |           |            |
| 29         | UB                                      | PC7      | MTIOC3A/MTCLKB/<br>TMO2/TOC0/<br>CACREF                     | TXD8/SMOSI8/<br>SSDA8/SMOSI10/<br>SSDA10/TXD10/<br>MISOA-A |                                  | IRQ14     |            |
| 30         |                                         | PC6      | MTIOC3C/MTCLKA/<br>TMC12/TIC0                               | RXD8/SMISO8/<br>SSCL8/SMISO10/<br>SSCL10/RXD10/<br>MOSIA-A |                                  | IRQ13     |            |
| 31         |                                         | PC5      | MTIOC3B/MTCLKD/<br>TMR12                                    | SCK8/SCK10/<br>RSPCKA-A                                    |                                  |           |            |

Table 1.12 List of Pin and Pin Functions (64-Pin LFQFP) (2/2)

| Pin Number<br>64-Pin LFQFP | Power Supply<br>Clock System<br>Control | I/O Port | Timer<br>(MTU, TPU, TMR,<br>RTC, CMTW, POE,<br>CAC) | Communication<br>(SCI, RSPI, RIIC,<br>USB)           | Memory Interface<br>(QSPI, SDHI) | Interrupt | A/D<br>D/A |
|----------------------------|-----------------------------------------|----------|-----------------------------------------------------|------------------------------------------------------|----------------------------------|-----------|------------|
| 32                         |                                         | PC4      | MTIOC3D/MTCLKC/<br>TMCI1/POE0#                      | CTS8#/RTS8#/SS8#/<br>SS10#/CTS10#/<br>RTS10#/SSLA0-A |                                  |           |            |
| 33                         |                                         | PC1      | MTIOC3A/TCLKD                                       | SSLA2-A                                              |                                  | IRQ12     |            |
| 34                         |                                         | PC0      | MTIOC3C/TCLKC                                       | SSLA1-A                                              |                                  | IRQ14     |            |
| 35                         |                                         | PB7      | MTIOC3B/TIOCB5                                      | TXD9/SSDA9/<br>SSDA11/TXD11                          |                                  |           |            |
| 36                         |                                         | PB6      | MTIOC3D/TIOCA5                                      | RXD9/SSCL9/<br>SSCL11/RXD11                          |                                  |           |            |
| 37                         |                                         | PB5      | MTIOC2A/MTIOC1B/<br>TIOCB4/TMRI1/<br>POE4#          | SCK9/SCK11                                           |                                  |           |            |
| 38                         | VCC                                     |          |                                                     |                                                      |                                  |           |            |
| 39                         | VSS                                     |          |                                                     |                                                      |                                  |           |            |
| 40                         |                                         | PA7      | TIOCB2                                              |                                                      |                                  |           |            |
| 41                         |                                         | PA6      | MTIC5V/MTCLKB/<br>TIOCA2/TMCI3/<br>POE10#           | CTS5#/RTS5#/SS5#                                     |                                  |           |            |
| 42                         |                                         | PA4      | MTIC5U/MTCLKA/<br>TIOCA1/TMRI0                      | TXD5/SMOSI5/<br>SSDA5                                |                                  | IRQ5-DS   |            |
| 43                         |                                         | PA2      | MTIOC7A                                             | RXD5/SMISO5/<br>SSCL5                                |                                  |           |            |
| 44                         |                                         | PA1      | MTIOC0B/MTCLKC/<br>MTIOC7B/TIOCB0                   | SCK5                                                 |                                  | IRQ11     |            |
| 45                         |                                         | PE7      | MTIOC6A/TOC1                                        |                                                      | SDHI_WP                          | IRQ7      |            |
| 46                         |                                         | PE6      | MTIOC6C/TIC1                                        |                                                      | SDHI_CD                          | IRQ6      |            |
| 47                         |                                         | PE2      | MTIOC4A/TIC3                                        | RXD12/SSCL12/<br>RXDX12                              |                                  | IRQ7-DS   |            |
| 48                         |                                         | PE1      | MTIOC4C/MTIOC3B                                     | TXD12/SSDA12/<br>TXDX12/SIOX12                       |                                  |           | ANEX1      |
| 49                         |                                         | PE0      | MTIOC3D                                             | SCK12                                                |                                  |           | ANEX0      |
| 50                         |                                         | PD7      | MTIC5U/POE0#                                        |                                                      | QMI-B/QIO1-B/<br>SDHI_D1-B       | IRQ7      | AN107      |
| 51                         |                                         | PD6      | MTIC5V/MTIOC8A/<br>POE4#                            |                                                      | QMO-B/QIO0-B/<br>SDHI_D0-B       | IRQ6      | AN106      |
| 52                         |                                         | PD5      | MTIC5W/MTIOC8C/<br>POE10#                           |                                                      | QSPCLK-B/<br>SDHI_CLK-B          | IRQ5      | AN113      |
| 53                         |                                         | PD4      | MTIOC8B/POE11#                                      |                                                      | QSSL-B/SDHI_CMD-<br>B            | IRQ4      | AN112      |
| 54                         |                                         | PD3      | MTIOC8D/TOC2/<br>POE8#                              |                                                      | QIO3-B/SDHI_D3-B                 | IRQ3      | AN111      |
| 55                         |                                         | PD2      | MTIOC4D/TIC2                                        |                                                      | QIO2-B/SDHI_D2-B                 | IRQ2      | AN110      |
| 56                         |                                         | P43      |                                                     |                                                      |                                  | IRQ11-DS  | AN003      |
| 57                         |                                         | P42      |                                                     |                                                      |                                  | IRQ10-DS  | AN002      |
| 58                         |                                         | P41      |                                                     |                                                      |                                  | IRQ9-DS   | AN001      |
| 59                         | VREFL0                                  |          |                                                     |                                                      |                                  |           |            |
| 60                         |                                         | P40      |                                                     |                                                      |                                  | IRQ8-DS   | AN000      |
| 61                         | VREFH0                                  |          |                                                     |                                                      |                                  |           |            |
| 62                         | AVCC0                                   |          |                                                     |                                                      |                                  |           |            |
| 63                         | AVSS0                                   |          |                                                     |                                                      |                                  |           |            |
| 64                         |                                         | P05      |                                                     |                                                      |                                  | IRQ13     | DA1        |

## 2. Electrical Characteristics

### 2.1 Absolute Maximum Ratings

**Table 2.1 Absolute Maximum Rating**

Conditions: VSS = AVSS0 = AVSS1 = VREFL0 = VSS\_USB = 0 V

| Item                                                |           | Symbol            | Value                           | Unit |
|-----------------------------------------------------|-----------|-------------------|---------------------------------|------|
| Power supply voltage                                |           | VCC, VCC_USB      | −0.3 to +4.0                    | V    |
| V <sub>BATT</sub> power supply voltage              |           | V <sub>BATT</sub> | −0.3 to +4.0                    | V    |
| Input voltage (except for ports for 5 V tolerant*1) |           | V <sub>in</sub>   | −0.3 to VCC + 0.3 (up to 4.0)   | V    |
| Input voltage (ports for 5 V tolerant*1)            |           | V <sub>in</sub>   | −0.3 to VCC + 4.0 (up to 5.8)   | V    |
| Reference power supply voltage                      |           | VREFH0            | −0.3 to AVCC0 + 0.3 (up to 4.0) | V    |
| Analog power supply voltage                         |           | AVCC0, AVCC1*2    | −0.3 to +4.0                    | V    |
| Analog input voltage                                |           | V <sub>AN</sub>   | −0.3 to AVCC + 0.3 (up to 4.0)  | V    |
| Junction temperature                                | D version | T <sub>j</sub>    | −40 to +105                     | °C   |
|                                                     | G version | T <sub>j</sub>    | −40 to +125                     | °C   |
| Storage temperature                                 |           | T <sub>stg</sub>  | −55 to +125                     | °C   |

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. P07, P11 to P17, P20, P21, P30 to P33, P67, and PC0 to PC3 are 5 V tolerant.

Note 2. Connect the AVCC0, AVCC1, and VCC\_USB pins to VCC, and the AVSS0, AVSS1, and VSS\_USB pins to VSS.

When the A/D converter unit 0 is not to be used, connect the VREFH0 pin to VCC and the VREFL0 pin to VSS, respectively.

Do not leave these pins open. Insert capacitors of high frequency characteristics between the AVCC0 and AVSS0 pins, or AVCC1 and AVSS1 pins. Place capacitors of about 0.1 μF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

## 2.2 Recommended Operating Conditions

**Table 2.2 Recommended Operating Conditions (1)**

| Item                                                                                 | Symbol            | Min.   | Typ. | Max.                    | Unit |
|--------------------------------------------------------------------------------------|-------------------|--------|------|-------------------------|------|
| Power supply voltage*1                                                               | VCC               | 2.7    | —    | 3.6                     | V    |
|                                                                                      | VSS               | —      | 0    | —                       |      |
| V <sub>BATT</sub> power supply voltage                                               | V <sub>BATT</sub> | 1.62*2 | —    | 3.6                     | V    |
| USB power supply voltage                                                             | VCC_USB           | —      | VCC  | —                       | V    |
|                                                                                      | VSS_USB           | —      | 0    | —                       |      |
| Analog power supply voltage*1, *3                                                    | AVCC0             | —      | VCC  | —                       | V    |
|                                                                                      | AVSS0             | —      | 0    | —                       |      |
|                                                                                      | AVCC1             | —      | VCC  | —                       |      |
|                                                                                      | AVSS1             | —      | 0    | —                       |      |
|                                                                                      | VREFH0            | 2.7    | —    | AVCC0                   |      |
|                                                                                      | VREFL0            | —      | 0    | —                       |      |
| Input voltage (except for 5 V tolerant ports, except for P03, P05, and P40 to P47)*4 | V <sub>in</sub>   | −0.3   | —    | VCC + 0.3               | V    |
| Input voltage (P03, P05, and P40 to P47)                                             | V <sub>in</sub>   | −0.3   | —    | AVCC0 + 0.3             | V    |
| Input voltage (5V tolerant: P11 to P17, P20, P21, P30 to P33, P67, and PC0 to PC3)*5 | V <sub>in</sub>   | −0.3   | —    | VCC + 3.6 (up to 5.5)   | V    |
| Input voltage (5V tolerant: P07)                                                     | V <sub>in</sub>   | −0.3   | —    | AVCC0 + 3.6 (up to 5.5) | V    |
| Operating temperature (D version)                                                    | T <sub>opr</sub>  | −40    | —    | 85                      | °C   |
| Operating temperature (G version)                                                    | T <sub>opr</sub>  | −40    | —    | 105                     | °C   |

Note 1. Comply with the following potential condition: VCC = AVCC0 = AVCC1 = VCC\_USB

Note 2. The low CL crystal unit cannot be used when the V<sub>BATT</sub> voltage is less than 2.0 V.

Note 3. For details, see section 53.6.11, Voltage Range of Analog Power Supply Pins in the User's Manual: Hardware.

Note 4. P07, P11 to P17, P20, P21, P30 to P33, P67, and PC0 to PC3 are 5 V tolerant.

Note 5. For P30, P31, and P32, input as follows when the V<sub>BATT</sub> power supply is selected.

V<sub>in</sub> Min. = −0.3, Max. = V<sub>BATT</sub> + 0.3 (V<sub>BATT</sub> = 1.62 to 3.6 V)

**Table 2.3 Recommended Operating Conditions (2)**

| Item                                                        | Symbol           | Value           |
|-------------------------------------------------------------|------------------|-----------------|
| Decoupling capacitance for stabilizing the internal voltage | C <sub>VCL</sub> | 0.22 μF ± 30%*1 |

Note 1. Use a multilayer ceramic capacitor with a nominal capacitance of 0.22 μF, for which the sum of the capacitance tolerance and change in the capacitance under the usage conditions will be no greater than ±30%.

## 2.3 DC Characteristics

**Table 2.4 DC Characteristics (1)**

Conditions:  $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AV_{CC0}$ ,  
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $T_a = T_{opr}$

| Item                                                               |                                                                                                                                                                                                                                       | Symbol           | Min.              | Typ.             | Max.             | Unit | Test Conditions |
|--------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|-------------------|------------------|------------------|------|-----------------|
| Schmitt trigger input voltage                                      | IRQ input pin*1<br>MTU input pin*1<br>POE3 input pin*1<br>TPU input pin*1<br>TMR input pin*1<br>CMTW input pin*1<br>SCI input pin*1<br>CAN input pin*1<br>CAC input pin*1<br>ADTRG# input pin*1<br>QSPI input pin*1<br>RES#, NMI, TCK | $V_{IH}$         | $0.8 \times VCC$  | —                | —                | V    |                 |
|                                                                    |                                                                                                                                                                                                                                       | $V_{IL}$         | —                 | —                | $0.2 \times VCC$ |      |                 |
|                                                                    |                                                                                                                                                                                                                                       | $\Delta V_T$     | $0.06 \times VCC$ | —                | —                |      |                 |
|                                                                    |                                                                                                                                                                                                                                       |                  |                   |                  |                  |      |                 |
|                                                                    |                                                                                                                                                                                                                                       |                  |                   |                  |                  |      |                 |
|                                                                    |                                                                                                                                                                                                                                       |                  |                   |                  |                  |      |                 |
|                                                                    |                                                                                                                                                                                                                                       |                  |                   |                  |                  |      |                 |
|                                                                    |                                                                                                                                                                                                                                       |                  |                   |                  |                  |      |                 |
|                                                                    |                                                                                                                                                                                                                                       |                  |                   |                  |                  |      |                 |
|                                                                    |                                                                                                                                                                                                                                       |                  |                   |                  |                  |      |                 |
|                                                                    | RIIC input pin<br>(except for SMBus)                                                                                                                                                                                                  | $V_{IH}$         | $0.7 \times VCC$  | —                | —                |      |                 |
|                                                                    |                                                                                                                                                                                                                                       | $V_{IL}$         | —                 | —                | $0.3 \times VCC$ |      |                 |
|                                                                    |                                                                                                                                                                                                                                       | $\Delta V_T$     | $0.05 \times VCC$ | —                | —                |      |                 |
|                                                                    | Ports for 5 V tolerant*2                                                                                                                                                                                                              | $V_{IH}$         | $0.8 \times VCC$  | —                | —                |      |                 |
|                                                                    |                                                                                                                                                                                                                                       | $V_{IL}$         | —                 | —                | $0.2 \times VCC$ |      |                 |
| Other input pins excluding ports for 5 V tolerant*3                | $V_{IH}$                                                                                                                                                                                                                              | $0.8 \times VCC$ | —                 | —                |                  |      |                 |
|                                                                    | $V_{IL}$                                                                                                                                                                                                                              | —                | —                 | $0.2 \times VCC$ |                  |      |                 |
| High level input voltage<br>(except for schmitt trigger input pin) | MD pin, EMLE                                                                                                                                                                                                                          | $V_{IH}$         | $0.9 \times VCC$  | —                | —                | V    |                 |
|                                                                    | EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, SDHI input pin, MMC input pin, PDC input pin, SDSI input pin                                                                                                                          |                  | $0.8 \times VCC$  | —                | —                |      |                 |
|                                                                    | ETHERC input pin                                                                                                                                                                                                                      |                  | 2.3               | —                | —                |      |                 |
|                                                                    | D0 to D31                                                                                                                                                                                                                             |                  | $0.7 \times VCC$  | —                | —                |      |                 |
|                                                                    | RIIC (SMBus)                                                                                                                                                                                                                          |                  | 2.1               | —                | —                |      |                 |
|                                                                    |                                                                                                                                                                                                                                       |                  |                   |                  |                  |      |                 |
|                                                                    |                                                                                                                                                                                                                                       |                  |                   |                  |                  |      |                 |
| Low level input voltage<br>(except for schmitt trigger input pin)  | MD pin, EMLE                                                                                                                                                                                                                          | $V_{IL}$         | —                 | —                | $0.1 \times VCC$ | V    |                 |
|                                                                    | EXTAL, RSPI input pin, ETHERC input pin, EXDMAC input pin, WAIT#, SDHI input pin, MMC input pin, PDC input pin, SDSI input pin                                                                                                        |                  | —                 | —                | $0.2 \times VCC$ |      |                 |
|                                                                    | D0 to D31                                                                                                                                                                                                                             |                  | —                 | —                | $0.3 \times VCC$ |      |                 |
|                                                                    | RIIC (SMBus)                                                                                                                                                                                                                          |                  | —                 | —                | 0.8              |      |                 |
|                                                                    |                                                                                                                                                                                                                                       |                  |                   |                  |                  |      |                 |

Note 1. This does not include the pins, which are multiplexed as ports for 5 V tolerant.

Note 2. P07, P11 to P17, P20, P21, P30 to P33, P67, and PC0 to PC3 are 5 V tolerant.

Note 3. For P30, P31, and P32, input as follows when the  $V_{BATT}$  power supply is selected.

$V_{IH}$  Min. =  $0.8 \times V_{BATT}$ ,  $V_{IL}$  Max. =  $0.2 \times V_{BATT}$  ( $V_{BATT} = 1.62$  to  $3.6$  V)

**Table 2.5 DC Characteristics (2)**

Conditions:  $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AV_{CC0}$ ,  
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $T_a = T_{opr}$

| Item                                    |                                                                                                        | Symbol      | Min.        | Typ. | Max. | Unit          | Test Conditions                                                                                       |
|-----------------------------------------|--------------------------------------------------------------------------------------------------------|-------------|-------------|------|------|---------------|-------------------------------------------------------------------------------------------------------|
| High level output voltage               | All output pins                                                                                        | $V_{OH}$    | $VCC - 0.5$ | —    | —    | V             | $I_{OH} = -1\text{ mA}$                                                                               |
| Low level output voltage                | All output pins (except for RIIC pins and ETHERC output pin)                                           | $V_{OL}$    | —           | —    | 0.5  | V             | $I_{OL} = 1.0\text{ mA}$                                                                              |
|                                         | RIIC output pin                                                                                        |             | —           | —    | 0.4  |               | $I_{OL} = 3.0\text{ mA}$                                                                              |
|                                         |                                                                                                        |             | —           | —    | 0.6  |               | $I_{OL} = 6.0\text{ mA}$                                                                              |
|                                         | RIIC output pin (only P12 and P13 in channel 0)                                                        | $V_{OL}$    | —           | —    | 0.4  | V             | $I_{OL} = 15.0\text{ mA}$ (ICFER.FMPE = 1)                                                            |
|                                         |                                                                                                        |             | —           | 0.4  | —    |               | $I_{OL} = 20.0\text{ mA}$ (ICFER.FMPE = 1)                                                            |
|                                         | ETHERC output pin                                                                                      | $V_{OL}$    | —           | —    | 0.4  | V             | $I_{OL} = 1.0\text{ mA}$                                                                              |
| Input leakage current                   | RES#, MD pin, EMLE*1, BSCANP*1, NMI                                                                    | $ I_{in} $  | —           | —    | 1.0  | $\mu\text{A}$ | $V_{in} = 0\text{ V}$<br>$V_{in} = VCC$                                                               |
| Three-state leakage current (off state) | Other than ports for 5 V tolerant                                                                      | $ I_{TSI} $ | —           | —    | 1.0  | $\mu\text{A}$ | $V_{in} = 0\text{ V}$<br>$V_{in} = VCC$                                                               |
|                                         | Ports for 5 V tolerant                                                                                 |             | —           | —    | 5.0  |               | $V_{in} = 0\text{ V}$<br>$V_{in} = 5.5\text{ V}$                                                      |
| Input pull-up resistor current          | Other than P35                                                                                         | $I_p$       | −300        | —    | −10  | $\mu\text{A}$ | $VCC = 2.7\text{ to }3.6\text{ V}$<br>$V_{in} = 0\text{ V}$                                           |
| Input pull-down resistor current        | EMLE, BSCANP                                                                                           | $I_p$       | 10          | —    | 300  | $\mu\text{A}$ | $V_{in} = VCC$                                                                                        |
| Input capacitance                       | All input pins (except for P03, P05, P12, P13, P16, P17, P20, P21, EMLE, BSCANP, USB0_DP, and USB0_DM) | $C_{in}$    | —           | —    | 8    | pF            | $V_{bias} = 0\text{ V}$<br>$V_{amp} = 20\text{ mV}$<br>$f = 1\text{ MHz}$<br>$T_a = 25^\circ\text{C}$ |
|                                         | P03, P05, P12, P13, P16, P17, P20, P21, EMLE, BSCANP, USB0_DP, and USB0_DM                             |             | —           | —    | 16   |               |                                                                                                       |
| Output voltage of the VCL pin           |                                                                                                        | $V_{CL}$    | —           | 1.18 | —    | V             |                                                                                                       |

Note 1. The input leakage current value at the EMLE and BSCANP pins are only when  $V_{in} = 0$  V.

**Table 2.6 DC Characteristics (3) (Products with 1 Mbyte of code flash memory or less)**Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ , $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V, $T_a = T_{opr}$ 

| Item             |                                                           |                                                                                                                                      | Symbol        | D version |      | G version |      | Unit    | Test Conditions                                                                                                                                        |
|------------------|-----------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|---------------|-----------|------|-----------|------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  |                                                           |                                                                                                                                      |               | Typ.      | Max. | Typ.      | Max. |         |                                                                                                                                                        |
| Supply current*1 | High-speed operating mode                                 | Full operation*2                                                                                                                     | $I_{CC}^{*3}$ | —         | 40   | —         | 45   | mA      | ICLK = 120 MHz,<br>PCLKA = 120 MHz,<br>PCLKB = 60 MHz,<br>PCLKC = 60 MHz,<br>PCLKD = 60 MHz,<br>FCLK = 60 MHz,<br>BCLK = 120 MHz,<br>BCLK pin = 60 MHz |
|                  |                                                           | Normal operation                                                                                                                     |               | 22        | —    | 22        | —    |         |                                                                                                                                                        |
|                  |                                                           | Peripheral module clocks are supplied*4                                                                                              |               |           |      |           |      |         |                                                                                                                                                        |
|                  |                                                           | Peripheral module clocks are stopped*4, *5                                                                                           |               | 12        | —    | 12        | —    |         |                                                                                                                                                        |
|                  |                                                           | Core Mark                                                                                                                            |               | 15        | —    | 15        | —    |         |                                                                                                                                                        |
|                  |                                                           | Peripheral module clocks are stopped*4, *5                                                                                           |               |           |      |           |      |         |                                                                                                                                                        |
|                  |                                                           | Sleep mode: Peripheral module clocks are supplied*4                                                                                  |               | 16        | 24   | 16        | 28   |         |                                                                                                                                                        |
|                  |                                                           | All module clock stop mode (reference value)                                                                                         |               | 8         | 15   | 8         | 19   |         |                                                                                                                                                        |
|                  |                                                           | Low-speed operating mode 1: Peripheral module clocks are stopped*4                                                                   |               | 1.1       | —    | 1.1       | —    |         | All clocks 1 MHz                                                                                                                                       |
|                  |                                                           | Low-speed operating mode 2: Peripheral module clocks are stopped*4                                                                   |               | 1.1       | —    | 1.1       | —    |         | All clocks 32.768 kHz                                                                                                                                  |
|                  |                                                           | Software standby mode                                                                                                                |               | 1.6       | 6.4  | 1.6       | 9.8  |         |                                                                                                                                                        |
|                  | Deep software standby mode                                | Power is supplied to the standby RAM and USB resume detecting unit (USB0 only)                                                       |               | 15.5      | 61   | 15.5      | 85   | $\mu$ A |                                                                                                                                                        |
|                  |                                                           | Power is not supplied to the standby RAM and USB resume detecting unit (USB0 only)                                                   |               | 11.5      | 38   | 11.5      | 48   |         |                                                                                                                                                        |
|                  |                                                           | Low power consumption function of the power-on reset circuit is disabled*6                                                           |               |           |      |           |      |         |                                                                                                                                                        |
|                  |                                                           | Low power consumption function of the power-on reset circuit is enabled*7                                                            |               | 4.9       | 29   | 4.9       | 39   |         |                                                                                                                                                        |
|                  |                                                           | Increase current by operating RTC                                                                                                    |               | 1         | —    | 1         | —    |         |                                                                                                                                                        |
|                  |                                                           | When a low $C_L$ crystal is in use                                                                                                   |               |           |      |           |      |         |                                                                                                                                                        |
|                  |                                                           | When a standard $C_L$ crystal is in use                                                                                              |               | 2         | —    | 2         | —    |         |                                                                                                                                                        |
|                  |                                                           | When the RTC is operating while VCC is not supplied (Only the RTC and sub-clock oscillator operate with the battery backup function) |               | 0.9       | —    | 0.9       | —    |         | $V_{BATT} = 2.0$ V,<br>$V_{CC} = 0$ V                                                                                                                  |
|                  |                                                           | When a low $C_L$ crystal is in use                                                                                                   |               | 1.6       | —    | 1.6       | —    |         | $V_{BATT} = 3.3$ V,<br>$V_{CC} = 0$ V                                                                                                                  |
|                  |                                                           | When a standard $C_L$ crystal is in use                                                                                              |               | 1.6       | —    | 1.6       | —    |         | $V_{BATT} = 1.62$ V,<br>$V_{CC} = 0$ V                                                                                                                 |
|                  |                                                           |                                                                                                                                      |               | 1.7       | —    | 1.7       | —    |         | $V_{BATT} = 2.0$ V,<br>$V_{CC} = 0$ V                                                                                                                  |
|                  |                                                           |                                                                                                                                      |               | 3.3       | —    | 3.3       | —    |         | $V_{BATT} = 3.3$ V,<br>$V_{CC} = 0$ V                                                                                                                  |
|                  | Inrush current on release from deep software standby mode | Inrush current*8                                                                                                                     | $I_{RUSH}$    | —         | 70   | —         | 70   | mA      |                                                                                                                                                        |
|                  |                                                           | Total inrush current*8                                                                                                               | $E_{RUSH}$    | —         | 1.0  | —         | 1.0  |         | $\mu$ C                                                                                                                                                |

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.

Note 2. Peripheral module clocks are supplied.

Note 3.  $I_{CC}$  depends on the  $f$  (ICLK) as follows (when ICLK/PCLKA : PCLKB/PCLKC/PCLKD : BCLK : BCLK pin = 2 : 1 : 2 : 1 and EXTAL = 12 MHz).

## • D version

 $I_{CC} \text{ max} = 0.28 \times f + 6.5$  (full operation in high-speed operating mode) $I_{CC} \text{ typ} = 0.16 \times f + 2.8$  (normal operation in high-speed operating mode) $I_{CC} \text{ typ} = 0.1 \times f + 1.0$  (ICLK 1 MHz max) (low-speed operating mode 1) $I_{CC} \text{ max} = 0.15 \times f + 6.5$  (sleep mode)

## • G version

 $I_{CC} \text{ max} = 0.30 \times f + 9.0$  (full operation in high-speed operating mode) $I_{CC} \text{ typ} = 0.16 \times f + 2.8$  (normal operation in high-speed operating mode) $I_{CC} \text{ typ} = 0.1 \times f + 1.0$  (ICLK 1 MHz max) (low-speed operating mode 1) $I_{CC} \text{ max} = 0.16 \times f + 9.0$  (sleep mode)

Note 4. Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control

registers A to D.

Note 5. When the peripheral module clock is stopped, the settings of the clock frequency are as follows:

ICLK = 120 MHz and PCLKA = PCLKB = PCLKC = PCLKD = FCLK = BCLK = BCLK pin = 3.75 MHz (divided by 64).

Note 6. When the low power consumption function is disabled, the DEEPCUT[1:0] bits are set to 01b.

Note 7. When the low power consumption function is enabled, the DEEPCUT[1:0] bits are set to 11b.

Note 8. Reference value

**Table 2.7 DC Characteristics (3) (Products with at least 1.5 Mbytes of code flash memory)**

Conditions: VCC = AVCC0 = AVCC1 = VCC\_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,

VSS = AVSS0 = AVSS1 = VREFL0 = VSS\_USB = 0 V,

T<sub>a</sub> = T<sub>opr</sub>

| Item             |                            |                                                                                                                                      | Symbol                                                                             | D version          |                   | G version |      | Unit | Test Conditions |                                                                                                                                                        |                                          |                       |  |    |
|------------------|----------------------------|--------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|--------------------|-------------------|-----------|------|------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|-----------------------|--|----|
|                  |                            |                                                                                                                                      |                                                                                    | Typ.               | Max.              | Typ.      | Max. |      |                 |                                                                                                                                                        |                                          |                       |  |    |
| Supply current*1 | High-speed operating mode  | Full operation*2                                                                                                                     |                                                                                    | I <sub>CC</sub> *3 | —                 | 60        | —    | 73   | mA              | ICLK = 120 MHz,<br>PCLKA = 120 MHz,<br>PCLKB = 60 MHz,<br>PCLKC = 60 MHz,<br>PCLKD = 60 MHz,<br>FCLK = 60 MHz,<br>BCLK = 120 MHz,<br>BCLK pin = 60 MHz |                                          |                       |  |    |
|                  |                            | Normal operation                                                                                                                     | Peripheral module clocks are supplied*4                                            |                    | 26                | —         | 26   | —    |                 |                                                                                                                                                        |                                          |                       |  |    |
|                  |                            |                                                                                                                                      | Peripheral module clocks are stopped*4, *5                                         |                    | 13                | —         | 13   | —    |                 |                                                                                                                                                        |                                          |                       |  |    |
|                  |                            | Core Mark                                                                                                                            | Peripheral module clocks are stopped*4, *5                                         |                    | 17                | —         | 17   | —    |                 |                                                                                                                                                        |                                          |                       |  |    |
|                  |                            | Sleep mode: Peripheral module clocks are supplied*4                                                                                  |                                                                                    |                    | 20                | 38        | 20   | 52   |                 |                                                                                                                                                        |                                          |                       |  |    |
|                  |                            | All module clock stop mode (reference value)                                                                                         |                                                                                    |                    | 9                 | 26        | 9    | 39   |                 |                                                                                                                                                        |                                          |                       |  |    |
|                  |                            | Increased by BGO operation*8                                                                                                         | Reading from the code flash memory while the data flash memory is being programmed |                    | 6                 | —         | 6    | —    |                 |                                                                                                                                                        |                                          |                       |  |    |
|                  |                            |                                                                                                                                      | Reading from the code flash memory while the code flash memory is being programmed |                    | 7                 | —         | 7    | —    |                 |                                                                                                                                                        |                                          |                       |  |    |
|                  |                            | Increased by Trusted Secure IP operation                                                                                             |                                                                                    |                    | —                 | 12        | —    | 12   |                 |                                                                                                                                                        |                                          |                       |  |    |
|                  |                            | Low-speed operating mode 1: Peripheral module clocks are stopped*4                                                                   |                                                                                    |                    | 1.6               | —         | 1.6  | —    |                 |                                                                                                                                                        | All clocks 1 MHz                         |                       |  |    |
|                  |                            | Low-speed operating mode 2: Peripheral module clocks are stopped*4                                                                   |                                                                                    |                    | 1.6               | —         | 1.6  | —    |                 |                                                                                                                                                        |                                          | All clocks 32.768 kHz |  |    |
|                  |                            | Software standby mode                                                                                                                |                                                                                    |                    | 1.6               | 13        | 1.6  | 22.4 |                 |                                                                                                                                                        |                                          |                       |  |    |
|                  | Deep software standby mode | Power is supplied to the standby RAM and USB resume detecting unit (USB0 only)                                                       |                                                                                    | I <sub>CC</sub>    | 15.5              | 70        | 15.5 | 98   | μA              | V <sub>BATT</sub> = 2.0 V,<br>VCC = 0 V                                                                                                                |                                          |                       |  |    |
|                  |                            | Power is not supplied to the standby RAM and USB resume detecting unit (USB0 only)                                                   | Low power consumption function of the power-on reset circuit is disabled*6         |                    | 11.5              | 42        | 11.5 | 54   |                 |                                                                                                                                                        |                                          |                       |  |    |
|                  |                            |                                                                                                                                      | Low power consumption function of the power-on reset circuit is enabled*7          |                    | 4.9               | 32        | 4.9  | 47   |                 |                                                                                                                                                        |                                          |                       |  |    |
|                  |                            | Increase current by operating RTC                                                                                                    | When a low C <sub>L</sub> crystal is in use                                        |                    | 1                 | —         | 1    | —    |                 |                                                                                                                                                        |                                          |                       |  |    |
|                  |                            |                                                                                                                                      | When a standard C <sub>L</sub> crystal is in use                                   |                    | 2                 | —         | 2    | —    |                 |                                                                                                                                                        |                                          |                       |  |    |
|                  |                            | When the RTC is operating while VCC is not supplied (Only the RTC and sub-clock oscillator operate with the battery backup function) | When a low C <sub>L</sub> crystal is in use                                        |                    | 0.9               | —         | 0.9  | —    |                 |                                                                                                                                                        | V <sub>BATT</sub> = 3.3 V,<br>VCC = 0 V  |                       |  |    |
|                  |                            |                                                                                                                                      |                                                                                    |                    | 1.6               | —         | 1.6  | —    |                 |                                                                                                                                                        | V <sub>BATT</sub> = 1.62 V,<br>VCC = 0 V |                       |  |    |
|                  |                            |                                                                                                                                      |                                                                                    |                    | 1.6               | —         | 1.6  | —    |                 |                                                                                                                                                        | V <sub>BATT</sub> = 2.0 V,<br>VCC = 0 V  |                       |  |    |
|                  |                            |                                                                                                                                      |                                                                                    |                    | 1.7               | —         | 1.7  | —    |                 |                                                                                                                                                        | V <sub>BATT</sub> = 3.3 V,<br>VCC = 0 V  |                       |  |    |
|                  |                            | Inrush current on release from deep software standby mode                                                                            | Inrush current*9                                                                   |                    | I <sub>RUSH</sub> | —         | 130  | —    |                 |                                                                                                                                                        | 130                                      | mA                    |  |    |
|                  |                            |                                                                                                                                      | Total inrush current*9                                                             |                    | E <sub>RUSH</sub> | —         | 1.0  | —    |                 |                                                                                                                                                        | 1.0                                      |                       |  | μC |

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.

Note 2. Peripheral module clocks are supplied.

Note 3. I<sub>CC</sub> depends on the f (ICLK) as follows (when ICLK/PCLKA : PCLKB/PCLKC/PCLKD : BCLK : BCLK pin = 2 : 1 : 2 : 1 and

EXTAL = 12 MHz).

- D version

$I_{CC} \text{ max} = 0.38 \times f + 14$  (full operation in high-speed operating mode)

$I_{CC} \text{ typ} = 0.18 \times f + 4$  (normal operation in high-speed operating mode)

$I_{CC} \text{ typ} = 0.1 \times f + 1.5$  (ICLK 1 MHz max) (low-speed operating mode 1)

$I_{CC} \text{ max} = 0.2 \times f + 14$  (sleep mode)

- G version

$I_{CC} \text{ max} = 0.44 \times f + 20$  (full operation in high-speed operating mode)

$I_{CC} \text{ typ} = 0.18 \times f + 4$  (normal operation in high-speed operating mode)

$I_{CC} \text{ typ} = 0.1 \times f + 1.5$  (ICLK 1 MHz max) (low-speed operating mode 1)

$I_{CC} \text{ max} = 0.27 \times f + 20$  (sleep mode)

Note 4. Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control registers A to D.

Note 5. When the peripheral module clock is stopped, the settings of the clock frequency are as follows:

ICLK = 120 MHz and PCLKA = PCLKB = PCLKC = PCLKD = FCLK = BCLK = BCLK pin = 3.75 MHz (divided by 64).

Note 6. When the low power consumption function is disabled, the DEEPCUT[1:0] bits are set to 01b.

Note 7. When the low power consumption function is enabled, the DEEPCUT[1:0] bits are set to 11b.

Note 8. These are the increases during programming of the code flash memory after the code flash memory (limitations apply to the combinations of address ranges of the program area and the readable area) or the data flash memory has been programmed or erased.

Note 9. Reference value

**Table 2.8 DC Characteristics (4)**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = VCC\_USB = 2.7 \text{ to } 3.6 \text{ V}$ ,  $2.7 \text{ V} \leq VREFH0 \leq AVCC0$ ,

$VSS = AVSS0 = AVSS1 = VREFL0 = VSS\_USB = 0 \text{ V}$ ,

$T_a = T_{opr}$

| Item                                                             |                                                                                                    |                   | Symbol               | D version |      |       | G version |      |                 | Unit            | Test Conditions  |
|------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|-------------------|----------------------|-----------|------|-------|-----------|------|-----------------|-----------------|------------------|
|                                                                  |                                                                                                    |                   |                      | Min.      | Typ. | Max.  | Min.      | Typ. | Max.            |                 |                  |
| Analog power supply current*1                                    | During 12-bit A/D conversion (unit 0)                                                              |                   | AI <sub>CC</sub>     | —         | 0.8  | 1     | —         | 0.8  | 1               | mA              | IAVCC0_AD        |
|                                                                  | During 12-bit A/D conversion (unit 0) with channel dedicated sample-and-hold circuits (3 channels) |                   |                      | —         | 1.7  | 2.5   | —         | 1.7  | 2.5             |                 | IAVCC0_AD + SH   |
|                                                                  | During 12-bit A/D conversion (unit 1)                                                              |                   |                      | —         | 0.6  | 1     | —         | 0.6  | 1               |                 | IAVCC1_AD        |
|                                                                  | During 12-bit A/D conversion (unit 1) + temperature sensor                                         |                   |                      | —         | 0.7  | 1.1   | —         | 0.7  | 1.1             |                 | IAVCC1_AD + TEMP |
|                                                                  | During D/A conversion (per unit)                                                                   | Unbuffered output |                      | —         | 0.25 | 0.4   | —         | 0.25 | 0.4             |                 | IAVCC1_DA        |
|                                                                  |                                                                                                    | Buffered output   |                      | —         | 0.75 | 1.1   | —         | 0.75 | 1.1             |                 |                  |
|                                                                  | Waiting for A/D, D/A, and temperature sensor conversion (all units)                                |                   |                      | —         | 0.9  | 1.4   | —         | 0.9  | 1.4             | IAVCC0 + IAVCC1 |                  |
| A/D, D/A, and temperature sensor are in standby mode (all units) |                                                                                                    | —                 | 1.4                  | 6.7       | —    | 1.4   | 9.0       | μA   | IAVCC0 + IAVCC1 |                 |                  |
| Reference power supply current                                   | During 12-bit A/D conversion (unit 0)                                                              |                   | AI <sub>REFH</sub>   | —         | 38   | 60    | —         | 38   | 60              | μA              | IVREFH0          |
|                                                                  | Waiting for 12-bit A/D conversion (unit 0)                                                         |                   |                      | —         | 0.07 | 0.5   | —         | 0.07 | 0.6             |                 | IVREFH0          |
|                                                                  | 12-bit A/D converter in module stop status (unit 0)                                                |                   |                      | —         | 0.07 | 0.4   | —         | 0.07 | 0.5             |                 | IVREFH0          |
| USB operating current                                            | Low speed                                                                                          | USB0              | I <sub>CCUSBLs</sub> | —         | 3.7  | 6.5   | —         | 3.7  | 6.5             | mA              | VCC_USB          |
|                                                                  | Full speed                                                                                         | USB0              | I <sub>CCUSBFs</sub> | —         | 4.2  | 10    | —         | 4.2  | 10              | mA              | VCC_USB          |
| RAM retention voltage                                            |                                                                                                    |                   | V <sub>RAM</sub>     | 2.7       | —    | —     | 2.7       | —    | —               | V               |                  |
| VCC rising gradient                                              |                                                                                                    |                   | SrVCC                | 8.4       | —    | 20000 | 8.4       | —    | 20000           | μs/V            |                  |
| VCC falling gradient*2                                           |                                                                                                    |                   | SfVCC                | 8.4       | —    | —     | 8.4       | —    | —               | μs/V            |                  |

Note 1. The reference power supply current is included in the power supply current value for 12-bit A/D converter (unit 1) and D/A converter.

Note 2. This applies when  $V_{BATT}$  is used.

**Table 2.9 Permissible Output Currents**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $T_a = T_{opr}$

| Item                                                       |                          |                                 | Symbol          | Min. | Typ. | Max. | Unit |
|------------------------------------------------------------|--------------------------|---------------------------------|-----------------|------|------|------|------|
| Permissible output low current<br>(average value per pin)  | All output pins*1        | Normal drive                    | $I_{OL}$        | —    | —    | 2.0  | mA   |
|                                                            | All output pins*2        | High drive                      |                 | —    | —    | 3.8  |      |
|                                                            | All output pins*3        | High-speed interface high-drive |                 | —    | —    | 7.5  |      |
| Permissible output low current<br>(max. value per pin)     | All output pins*1        | Normal drive                    | $I_{OL}$        | —    | —    | 4.0  | mA   |
|                                                            | All output pins*2        | High drive                      |                 | —    | —    | 7.6  |      |
|                                                            | All output pins*3        | High-speed interface high-drive |                 | —    | —    | 15   |      |
| Permissible output low current (total)                     | Total of all output pins |                                 | $\Sigma I_{OL}$ | —    | —    | 80   | mA   |
| Permissible output high current<br>(average value per pin) | All output pins*1        | Normal drive                    | $I_{OH}$        | —    | —    | -2.0 | mA   |
|                                                            | All output pins*2        | High drive                      |                 | —    | —    | -3.8 |      |
|                                                            | All output pins*3        | High-speed interface high-drive |                 | —    | —    | -7.5 |      |
| Permissible output high current<br>(max. value per pin)    | All output pins*1        | Normal drive                    | $I_{OH}$        | —    | —    | -4.0 | mA   |
|                                                            | All output pins*2        | High drive                      |                 | —    | —    | -7.6 |      |
|                                                            | All output pins*3        | High-speed interface high-drive |                 | —    | —    | -15  |      |
| Permissible output high current (total)                    | Total of all output pins |                                 | $\Sigma I_{OH}$ | —    | —    | -80  | mA   |

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

Note 3. This is the value when high-speed interface high-driving ability is set with a pin for which high-speed interface high-driving ability is selectable.

**Table 2.10 Thermal Resistance Value (Reference)**

| Item               | Package                      | Symbol        | Max. | Unit | Test Conditions                    |
|--------------------|------------------------------|---------------|------|------|------------------------------------|
| Thermal resistance | 176-pin LFQFP (PLQP0176KB-A) | $\theta_{ja}$ | 48.0 | °C/W | JESD51-2 and<br>JESD51-7 compliant |
|                    | 144-pin LFQFP (PLQP0144KA-B) |               | 50.9 |      |                                    |
|                    | 100-pin LFQFP (PLQP0100KB-B) |               | 52.5 |      |                                    |
|                    | 64-pin LFQFP (PLQP0064KB-C)  |               | 53.7 |      |                                    |
|                    | 177-pin TFLGA (PTLG0177KA-A) |               | 36.3 |      | JESD51-2 and<br>JESD51-9 compliant |
|                    | 176-pin LFBGA (PLBG0176GA-A) |               | 35.4 |      |                                    |
|                    | 145-pin TFLGA (PTLG0145KA-A) |               | 34.6 |      |                                    |
|                    | 100-pin TFLGA (PTLG0100JA-A) |               | 34.1 |      |                                    |
|                    | 64-pin TFBGA (PTBG0064KB-A)  |               | 35.3 |      |                                    |
|                    | 176-pin LFQFP (PLQP0176KB-A) | $\Psi_{jt}$   | 1.0  | °C/W | JESD51-2 and<br>JESD51-7 compliant |
|                    | 144-pin LFQFP (PLQP0144KA-B) |               | 1.5  |      |                                    |
|                    | 100-pin LFQFP (PLQP0100KB-B) |               | 1.5  |      |                                    |
|                    | 64-pin LFQFP (PLQP0064KB-C)  |               | 1.5  |      |                                    |
|                    | 177-pin TFLGA (PTLG0177KA-A) |               | 0.3  |      | JESD51-2 and<br>JESD51-9 compliant |
|                    | 176-pin LFBGA (PLBG0176GA-A) |               | 0.3  |      |                                    |
|                    | 145-pin TFLGA (PTLG0145KA-A) |               | 0.4  |      |                                    |
|                    | 100-pin TFLGA (PTLG0100JA-A) |               | 0.4  |      |                                    |
|                    | 64-pin TFBGA (PTBG0064KB-A)  |               | 0.5  |      |                                    |

Note: The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

## 2.4 AC Characteristics

**Table 2.11 Operating Frequency (High-Speed Operating Mode)**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $T_a = T_{opr}$

| Item                |                                 |                             | Symbol | Min. | Typ. | Max. | Unit |
|---------------------|---------------------------------|-----------------------------|--------|------|------|------|------|
| Operating frequency | System clock (ICLK)             |                             | f      | —    | —    | 120  | MHz  |
|                     | Peripheral module clock (PCLKA) |                             |        | —    | —    | 120  |      |
|                     | Peripheral module clock (PCLKB) |                             |        | —    | —    | 60   |      |
|                     | Peripheral module clock (PCLKC) |                             |        | —    | —    | 60   |      |
|                     | Peripheral module clock (PCLKD) |                             |        | —    | —    | 60   |      |
|                     | Flash-IF clock (FCLK)           |                             |        | —*1  | —    | 60   |      |
|                     | External bus clock (BCLK)       | Package of 144 pins or more |        | —    | —    | 120  |      |
|                     |                                 | 100-pin package             |        | —    | —    | 60   |      |
|                     | BCLK pin output                 | Package of 144 pins or more |        | —    | —    | 60   |      |
|                     |                                 | 100-pin package             |        | —    | —    | 30   |      |
|                     | SDRAM clock (SDCLK)             | Package of 144 pins or more |        | —    | —    | 60   |      |
|                     | SDCLK pin output                | Package of 144 pins or more |        | —    | —    | 60   |      |

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the flash memory contents.

**Table 2.12 Operating Frequency (Low-Speed Operating Mode 1)**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $T_a = T_{opr}$

| Item                |                                               |                             | Symbol | Min. | Typ. | Max. | Unit |
|---------------------|-----------------------------------------------|-----------------------------|--------|------|------|------|------|
| Operating frequency | System clock (ICLK)                           |                             | f      | —    | —    | 1    | MHz  |
|                     | Peripheral module clock (PCLKA)               |                             |        | —    | —    | 1    |      |
|                     | Peripheral module clock (PCLKB)               |                             |        | —    | —    | 1    |      |
|                     | Peripheral module clock (PCLKC)* <sup>1</sup> |                             |        | —    | —    | 1    |      |
|                     | Peripheral module clock (PCLKD)* <sup>1</sup> |                             |        | —    | —    | 1    |      |
|                     | Flash-IF clock (FCLK)                         |                             |        | —    | —    | 1    |      |
|                     | External bus clock (BCLK)                     | Package of 144 pins or more |        | —    | —    | 1    |      |
|                     |                                               | 100-pin package             |        | —    | —    | 1    |      |
|                     | BCLK pin output                               | Package of 144 pins or more |        | —    | —    | 1    |      |
|                     |                                               | 100-pin package             |        | —    | —    | 1    |      |
|                     | SDRAM clock (SDCLK)                           |                             |        | —    | —    | 1    |      |
|                     | SDCLK pin output                              |                             |        | —    | —    | 1    |      |

Note 1. When the 12-bit A/D converter is used, the frequency must be set to at least 1 MHz.

**Table 2.13 Operating Frequency (Low-Speed Operating Mode 2)**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $T_a = T_{opr}$

| Item                |                                   |                             | Symbol | Min. | Typ. | Max. | Unit |
|---------------------|-----------------------------------|-----------------------------|--------|------|------|------|------|
| Operating frequency | System clock (ICLK)               |                             | f      | 32   | —    | 264  | kHz  |
|                     | Peripheral module clock (PCLKA)   |                             |        | —    | —    | 264  |      |
|                     | Peripheral module clock (PCLKB)   |                             |        | —    | —    | 264  |      |
|                     | Peripheral module clock (PCLKC)*1 |                             |        | —    | —    | 264  |      |
|                     | Peripheral module clock (PCLKD)*1 |                             |        | —    | —    | 264  |      |
|                     | Flash-IF clock (FCLK)             |                             |        | 32   | —    | 264  |      |
|                     | External bus clock (BCLK)         | Package of 144 pins or more |        | —    | —    | 264  |      |
|                     |                                   | 100-pin package             |        | —    | —    | 264  |      |
|                     | BCLK pin output                   | Package of 144 pins or more |        | —    | —    | 264  |      |
|                     |                                   | 100-pin package             |        | —    | —    | 264  |      |
|                     | SDRAM clock (SDCLK)               | Package of 144 pins or more |        | —    | —    | 264  |      |
|                     | SDCLK pin output                  | Package of 144 pins or more |        | —    | —    | 264  |      |

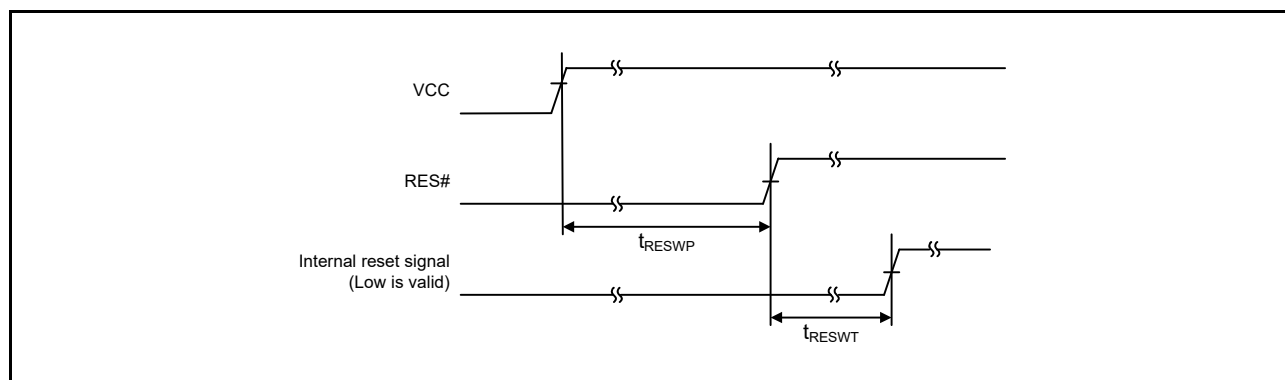
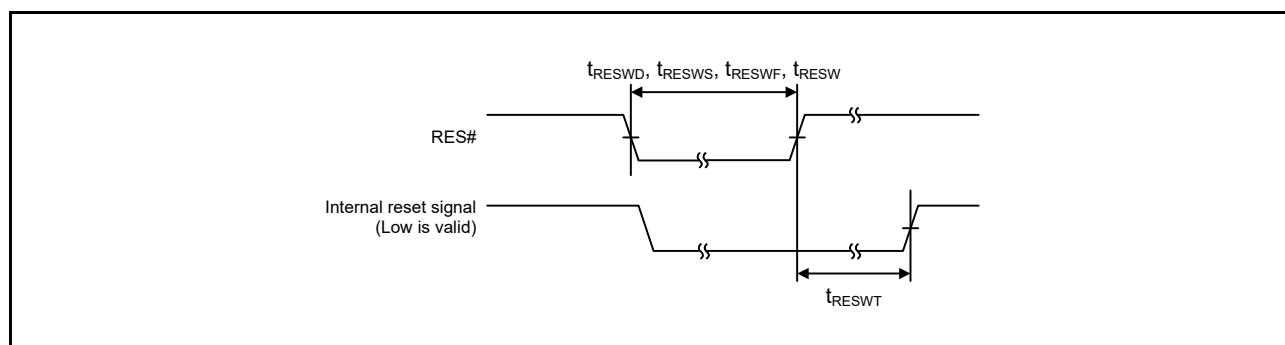
Note 1. The 12-bit A/D converter cannot be used.

## 2.4.1 Reset Timing

**Table 2.14 Reset Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $T_a = T_{opr}$

| Item                                                                                            |                                                                                                                     | Symbol      | Min. | Typ. | Max. | Unit       | Test Conditions |
|-------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|-------------|------|------|------|------------|-----------------|
| RES# pulse width                                                                                | Power-on                                                                                                            | $t_{RESWP}$ | 1    | —    | —    | ms         | Figure 2.1      |
|                                                                                                 | Deep software standby mode                                                                                          | $t_{RESWD}$ | 0.6  | —    | —    | ms         | Figure 2.2      |
|                                                                                                 | Software standby mode, low-speed operating mode 2                                                                   | $t_{RESWS}$ | 0.3  | —    | —    | ms         |                 |
|                                                                                                 | Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory | $t_{RESWF}$ | 200  | —    | —    | $\mu$ s    |                 |
|                                                                                                 | Other than above                                                                                                    | $t_{RESW}$  | 200  | —    | —    | $\mu$ s    |                 |
| Waiting time after release from the RES# pin reset                                              |                                                                                                                     | $t_{RESWT}$ | 54   | —    | 55   | $t_{Lcyc}$ | Figure 2.1      |
| Internal reset time<br>(independent watchdog timer reset, watchdog timer reset, software reset) |                                                                                                                     | $t_{RESW2}$ | 100  | —    | 108  | $t_{Lcyc}$ |                 |

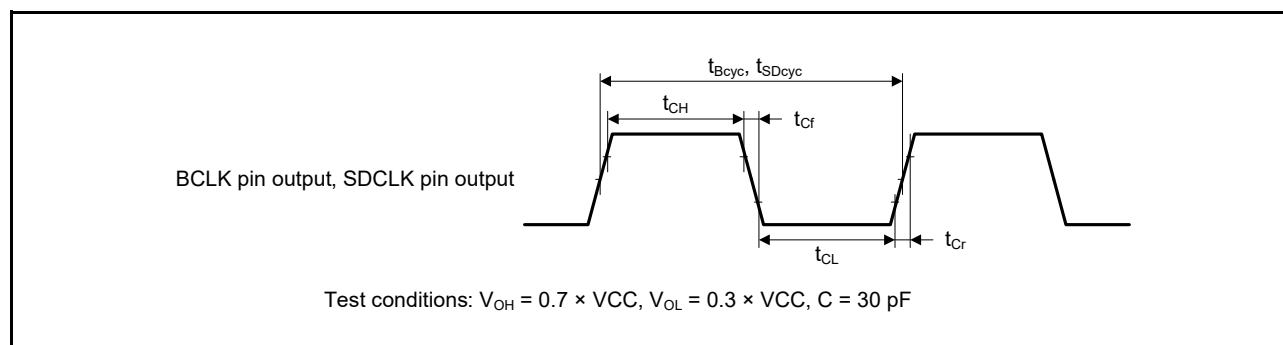
**Figure 2.1 Reset Input Timing at Power-On****Figure 2.2 Reset Input Timing**

## 2.4.2 Clock Timing

**Table 2.15 BCLK Pin Output, SDCLK Pin Output Clock Timing**

Conditions:  $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AV_{CC0}$ ,  
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $T_a = T_{opr}$

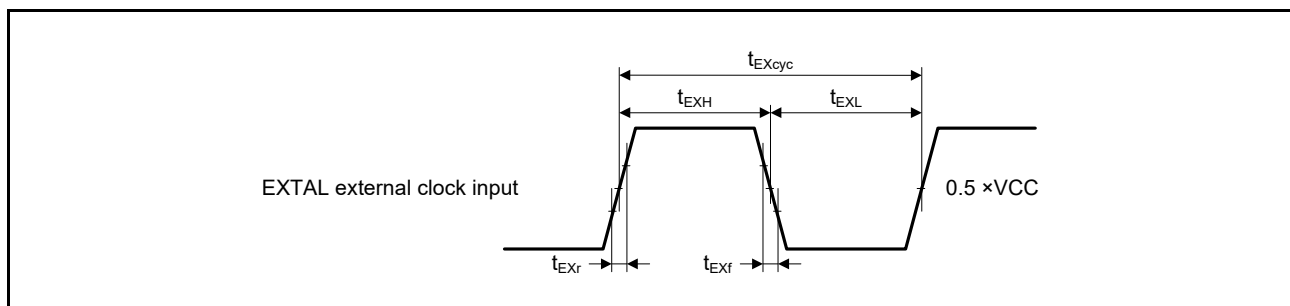
| Item                              |                             | Symbol     | Min. | Typ. | Max. | Unit | Test Conditions |
|-----------------------------------|-----------------------------|------------|------|------|------|------|-----------------|
| BCLK pin output cycle time        | Package of 144 pins or more | $t_{Bcyc}$ | 16.6 | —    | —    | ns   | Figure 2.3      |
|                                   | 100-pin package             |            | 33.2 | —    | —    |      |                 |
| BCLK pin output high pulse width  |                             | $t_{CH}$   | 3.3  | —    | —    | ns   |                 |
| BCLK pin output low pulse width   |                             | $t_{CL}$   | 3.3  | —    | —    | ns   |                 |
| BCLK pin output rising time       |                             | $t_{Cr}$   | —    | —    | 5    | ns   |                 |
| BCLK pin output falling time      |                             | $t_{Cf}$   | —    | —    | 5    | ns   |                 |
| SDCLK pin output cycle time       | Package of 144 pins or more | $t_{Bcyc}$ | 16.6 | —    | —    | ns   |                 |
| SDCLK pin output high pulse width |                             | $t_{CH}$   | 3.3  | —    | —    | ns   |                 |
| SDCLK pin output low pulse width  |                             | $t_{CL}$   | 3.3  | —    | —    | ns   |                 |
| SDCLK pin output rising time      |                             | $t_{Cr}$   | —    | —    | 5    | ns   |                 |
| SDCLK pin output falling time     |                             | $t_{Cf}$   | —    | —    | 5    | ns   |                 |

**Figure 2.3 BCLK Pin and SDCLK Pin Output Timing**

**Table 2.16 EXTAL Clock Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = VCC\_USB = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq VREFH0 \leq AVCC0$ ,  
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS\_USB = 0$  V,  
 $T_a = T_{opr}$

| Item                                        | Symbol       | Min.  | Typ. | Max. | Unit | Test Conditions |
|---------------------------------------------|--------------|-------|------|------|------|-----------------|
| EXTAL external clock input cycle time       | $t_{EXcyc}$  | 41.66 | —    | —    | ns   | Figure 2.4      |
| EXTAL external clock input frequency        | $f_{EXMAIN}$ | —     | —    | 24   | MHz  |                 |
| EXTAL external clock input high pulse width | $t_{EXH}$    | 15.83 | —    | —    | ns   |                 |
| EXTAL external clock input low pulse width  | $t_{EXL}$    | 15.83 | —    | —    | ns   |                 |
| EXTAL external clock rising time            | $t_{EXr}$    | —     | —    | 5    | ns   |                 |
| EXTAL external clock falling time           | $t_{EXf}$    | —     | —    | 5    | ns   |                 |

**Figure 2.4 EXTAL External Clock Input Timing****Table 2.17 Main Clock Timing**

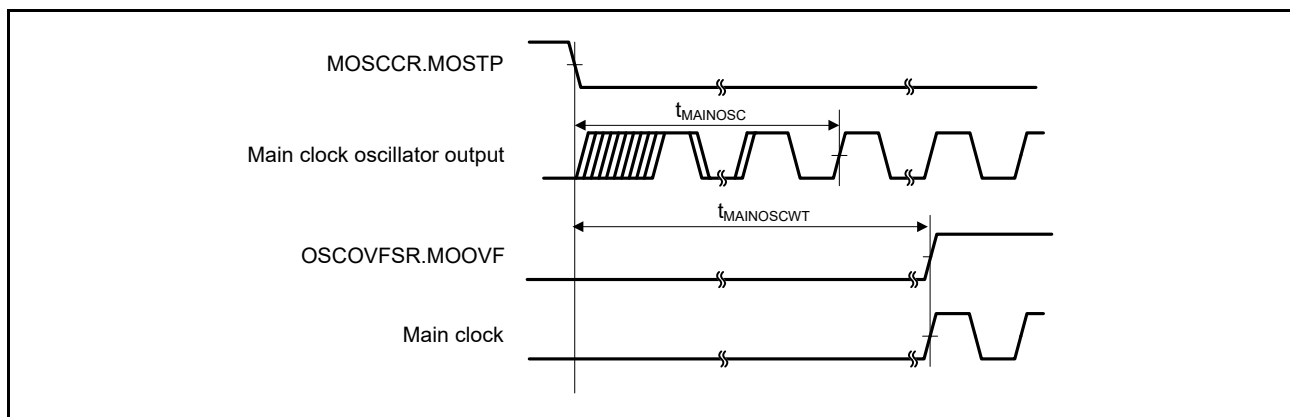
Conditions:  $V_{CC} = AVCC0 = AVCC1 = VCC\_USB = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq VREFH0 \leq AVCC0$ ,  
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS\_USB = 0$  V,  
 $T_a = T_{opr}$

| Item                                                     | Symbol         | Min. | Typ. | Max. | Unit | Test Conditions |
|----------------------------------------------------------|----------------|------|------|------|------|-----------------|
| Main clock oscillation frequency                         | $f_{MAIN}$     | 8    | —    | 24   | MHz  | Figure 2.5      |
| Main clock oscillator stabilization time (crystal)       | $t_{MAINOSC}$  | —    | —    | —*1  | ms   |                 |
| Main clock oscillation stabilization wait time (crystal) | $t_{MAINOSCW}$ | —    | —    | —*2  | ms   |                 |

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.

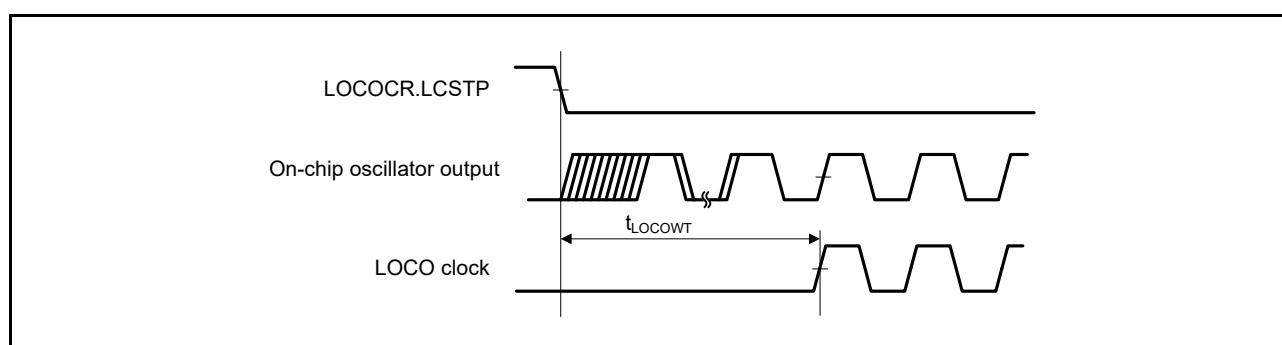
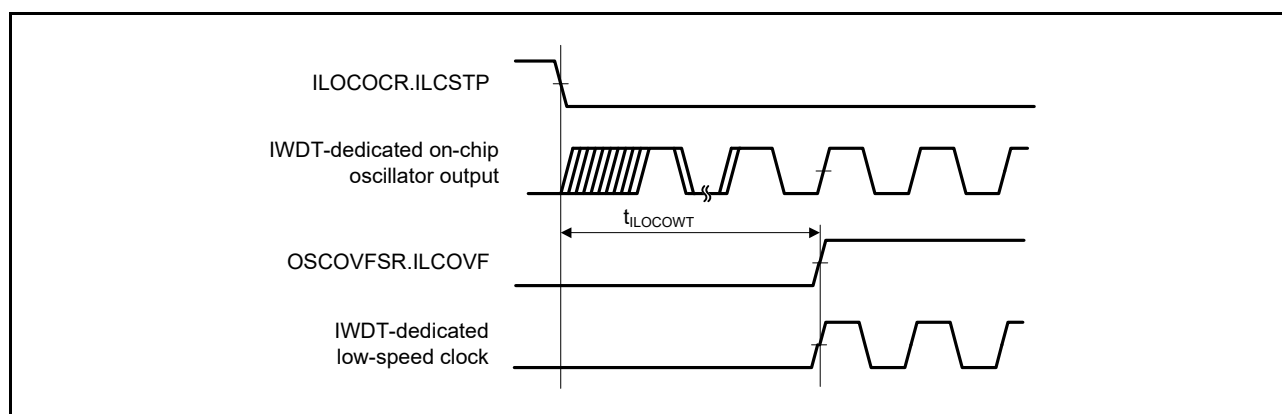
$$t_{MAINOSCW} = [(MSTS[7:0] \text{ bits} \times 32) + 10] / f_{LOCO}$$

**Figure 2.5 Main Clock Oscillation Start Timing**

**Table 2.18 LOCO and IWDT-Dedicated Low-Speed Clock Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $T_a = T_{opr}$

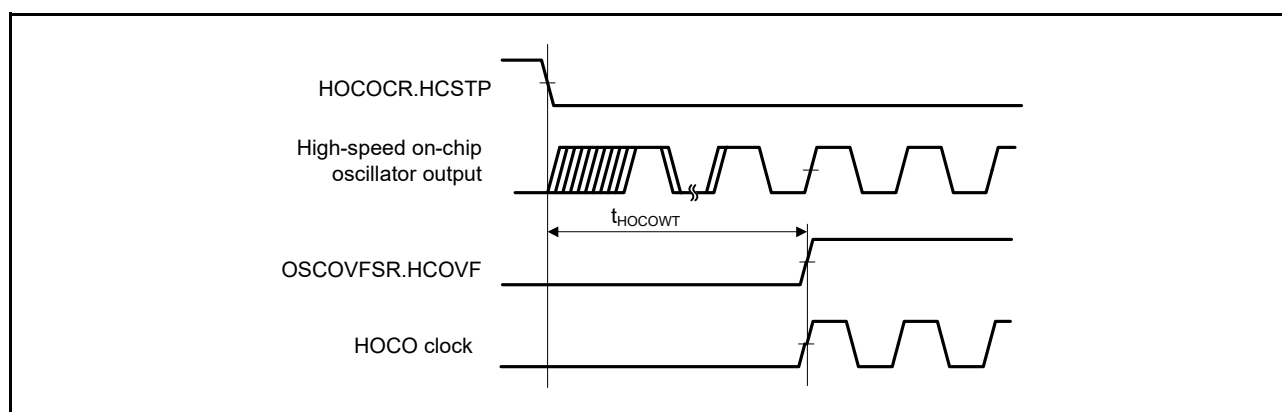
| Item                                                               | Symbol        | Min. | Typ. | Max. | Unit    | Test Conditions |
|--------------------------------------------------------------------|---------------|------|------|------|---------|-----------------|
| LOCO clock cycle time                                              | $t_{Lcyc}$    | 3.78 | 4.16 | 4.63 | $\mu$ s |                 |
| LOCO clock oscillation frequency                                   | $f_{LOCO}$    | 216  | 240  | 264  | kHz     |                 |
| LOCO clock oscillation stabilization wait time                     | $t_{LOCOWT}$  | —    | —    | 44   | $\mu$ s | Figure 2.6      |
| IWDT-dedicated low-speed clock cycle time                          | $t_{iLcyc}$   | 7.57 | 8.33 | 9.26 | $\mu$ s |                 |
| IWDT-dedicated low-speed clock oscillation frequency               | $f_{iLOCO}$   | 108  | 120  | 132  | kHz     |                 |
| IWDT-dedicated low-speed clock oscillation stabilization wait time | $t_{iLOCOWT}$ | —    | 142  | 190  | $\mu$ s | Figure 2.7      |

**Figure 2.6 LOCO Clock Oscillation Start Timing****Figure 2.7 IWDT-dedicated Low-Speed Clock Oscillation Start Timing**

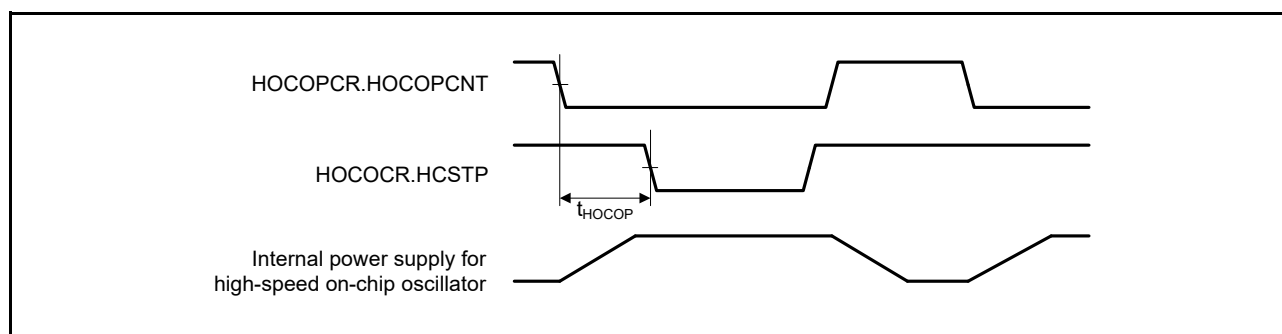
**Table 2.19 HOCO Clock Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $T_a = T_{opr}$

| Item                                           | Symbol       | Min.  | Typ. | Max.  | Unit          | Test Conditions                                      |
|------------------------------------------------|--------------|-------|------|-------|---------------|------------------------------------------------------|
| HOCO clock oscillation frequency               | $f_{HOCO}$   | 15.61 | 16   | 16.39 | MHz           | $-20^{\circ}\text{C} \leq T_a$                       |
|                                                |              | 17.56 | 18   | 18.44 |               |                                                      |
|                                                |              | 19.52 | 20   | 20.48 |               |                                                      |
|                                                |              | 15.52 | 16   | 16.48 |               | $-40^{\circ}\text{C} \leq T_a < -20^{\circ}\text{C}$ |
|                                                |              | 17.46 | 18   | 18.54 |               |                                                      |
|                                                |              | 19.4  | 20   | 20.6  |               |                                                      |
| HOCO clock oscillation stabilization wait time | $t_{HOCOWT}$ | —     | 105  | 149   | $\mu\text{s}$ | Figure 2.8                                           |
| HOCO clock power supply stabilization time     | $t_{HOCOP}$  | —     | —    | 150   | $\mu\text{s}$ | Figure 2.9                                           |



**Figure 2.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)**

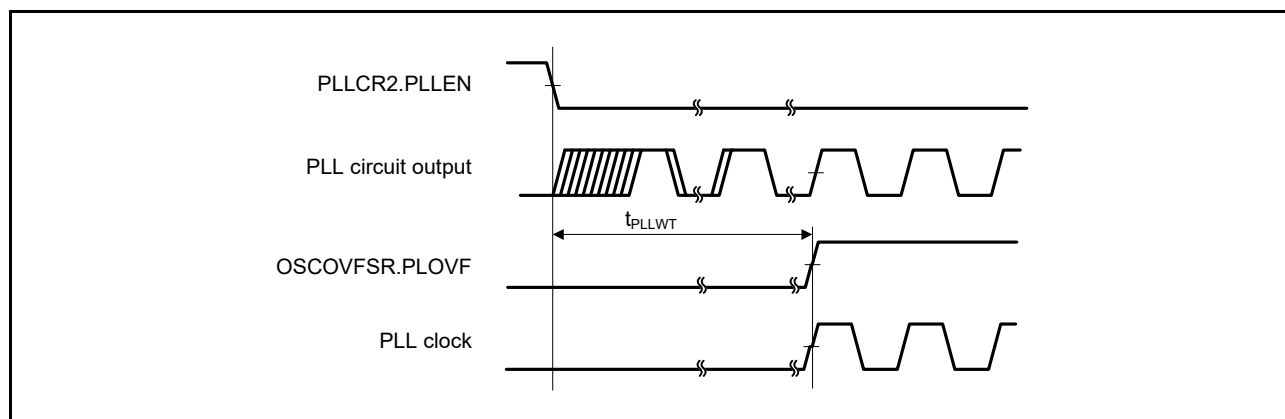


**Figure 2.9 High-Speed On-Chip Oscillator Power Supply Control Timing**

**Table 2.20 PLL Clock Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $T_a = T_{opr}$

| Item                                          | Symbol      | Min. | Typ. | Max. | Unit    | Test Conditions |
|-----------------------------------------------|-------------|------|------|------|---------|-----------------|
| PLL clock oscillation frequency               | $f_{PLL}$   | 120  | —    | 240  | MHz     |                 |
| PLL clock oscillation stabilization wait time | $t_{PLLWT}$ | —    | 259  | 320  | $\mu$ s | Figure 2.10     |

**Figure 2.10 PLL Clock Oscillation Start Timing****Table 2.21 Sub-Clock Timing**

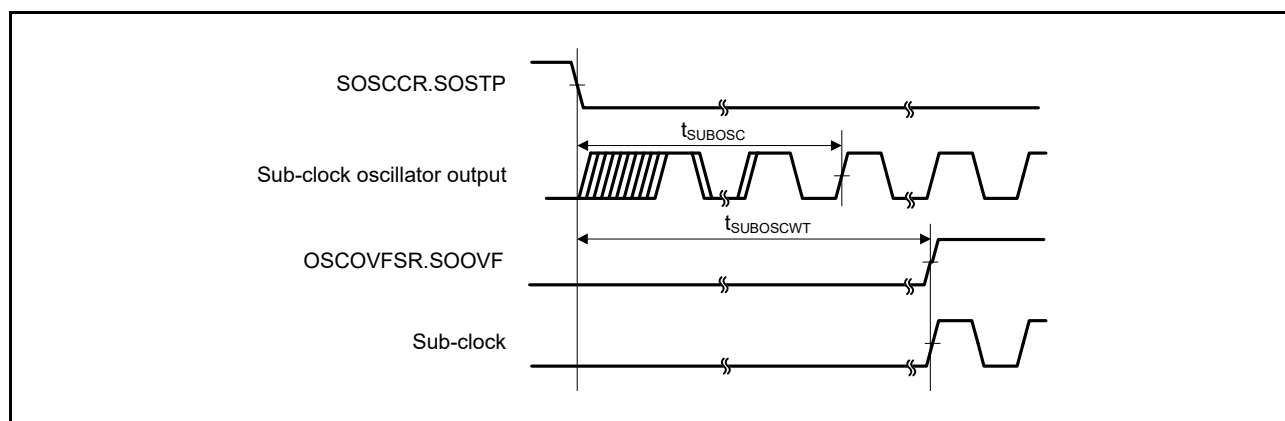
Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $V_{BATT} = 1.62$  to  $3.6$  V,  $T_a = T_{opr}$

| Item                                          | Symbol         | Min. | Typ.   | Max. | Unit | Test Conditions |
|-----------------------------------------------|----------------|------|--------|------|------|-----------------|
| Sub-clock oscillation frequency               | $f_{SUB}$      | —    | 32.768 | —    | kHz  |                 |
| Sub-clock oscillation stabilization time      | $t_{SUBOSC}$   | —    | —      | *1   | s    | Figure 2.11     |
| Sub-clock oscillation stabilization wait time | $t_{SUBOSCWT}$ | —    | —      | *2   | s    |                 |

Note 1. When using a sub-clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the  $SOSCWTCCR.SSTS[7:0]$  bits determines the sub-clock oscillation stabilization wait time in accord with the formula below.

$$t_{SUBOSCWT} = [(SSTS[7:0] \text{ bits} \times 16384) + 10] / f_{LOCO}$$

**Figure 2.11 Sub-Clock Oscillation Start Timing**

## 2.4.3 Timing of Recovery from Low Power Consumption Modes

**Table 2.22 Timing of Recovery from Low Power Consumption Modes (1)**

Conditions:  $VCC = AVCC0 = AVCC1 = VCC\_USB = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq VREFH0 \leq AVCC0$ ,  
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS\_USB = 0$  V,  
 $T_a = T_{opr}$

| Item                                        |                                                      |                                                                   | Symbol      | Min. | Typ. | Max.                                                                    |                                        | Unit    | Test Conditions |
|---------------------------------------------|------------------------------------------------------|-------------------------------------------------------------------|-------------|------|------|-------------------------------------------------------------------------|----------------------------------------|---------|-----------------|
|                                             |                                                      |                                                                   |             |      |      | $t_{SBYOSCWT}^{*2}$                                                     | $t_{SBYSEQ}^{*3}$                      |         |                 |
| Recovery time from software standby mode *1 | Crystal resonator connected to main clock oscillator | Main clock oscillator operating                                   | $t_{SBYMC}$ | —    | —    | $\{(MSTS[7:0] \text{ bit} \times 32) + 76\} / 0.216$                    | $100 + 7 / f_{ICLK} + 2n / f_{MAIN}$   | $\mu s$ | Figure 2.12     |
|                                             |                                                      | Main clock oscillator and PLL circuit operating                   | $t_{SBYPC}$ |      |      | $\{(MSTS[7:0] \text{ bit} \times 32) + 138\} / 0.216$                   | $100 + 7 / f_{ICLK} + 2n / f_{PLL}$    |         |                 |
|                                             | External clock input to main clock oscillator        | Main clock oscillator operating                                   | $t_{SBYEX}$ |      |      | 352                                                                     | $100 + 7 / f_{ICLK} + 2n / f_{EXMAIN}$ |         |                 |
|                                             |                                                      | Main clock oscillator and PLL circuit operating                   | $t_{SBYPE}$ |      |      | 639                                                                     | $100 + 7 / f_{ICLK} + 2n / f_{PLL}$    |         |                 |
|                                             | Sub-clock oscillator operating                       |                                                                   | $t_{SBYSC}$ |      |      | $\{(SSTS[7:0] \text{ bit} \times 16384) + 13\} / 0.216 + 10 / f_{FCLK}$ | $100 + 4 / f_{ICLK} + 2n / f_{SUE}$    |         |                 |
|                                             | High-speed on-chip oscillator operating              | High-speed on-chip oscillator operating                           | $t_{SBYHO}$ |      |      | 454                                                                     | $100 + 7 / f_{ICLK} + 2n / f_{HOCO}$   |         |                 |
|                                             |                                                      | High-speed on-chip oscillator operating and PLL circuit operating | $t_{SBYPH}$ |      |      | 741                                                                     | $100 + 7 / f_{ICLK} + 2n / f_{PLL}$    |         |                 |
|                                             | Low-speed on-chip oscillator operating*4             |                                                                   | $t_{SBYLO}$ |      |      | 338                                                                     | $100 + 7 / f_{ICLK} + 2n / f_{LOCO}$   |         |                 |

Note 1. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization waiting time ( $t_{SBYOSCWT}$ ) and the time required for operations by the software standby release sequencer ( $t_{SBYSEQ}$ ).

Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time  $t_{SBYOSCWT}$  is selected.

Note 3. For n, the greatest value is selected from among the internal clock division settings.

Note 4. This condition applies when  $f_{ICLK}:f_{FCLK} = 1:1, 2:1$ , or  $4:1$ .

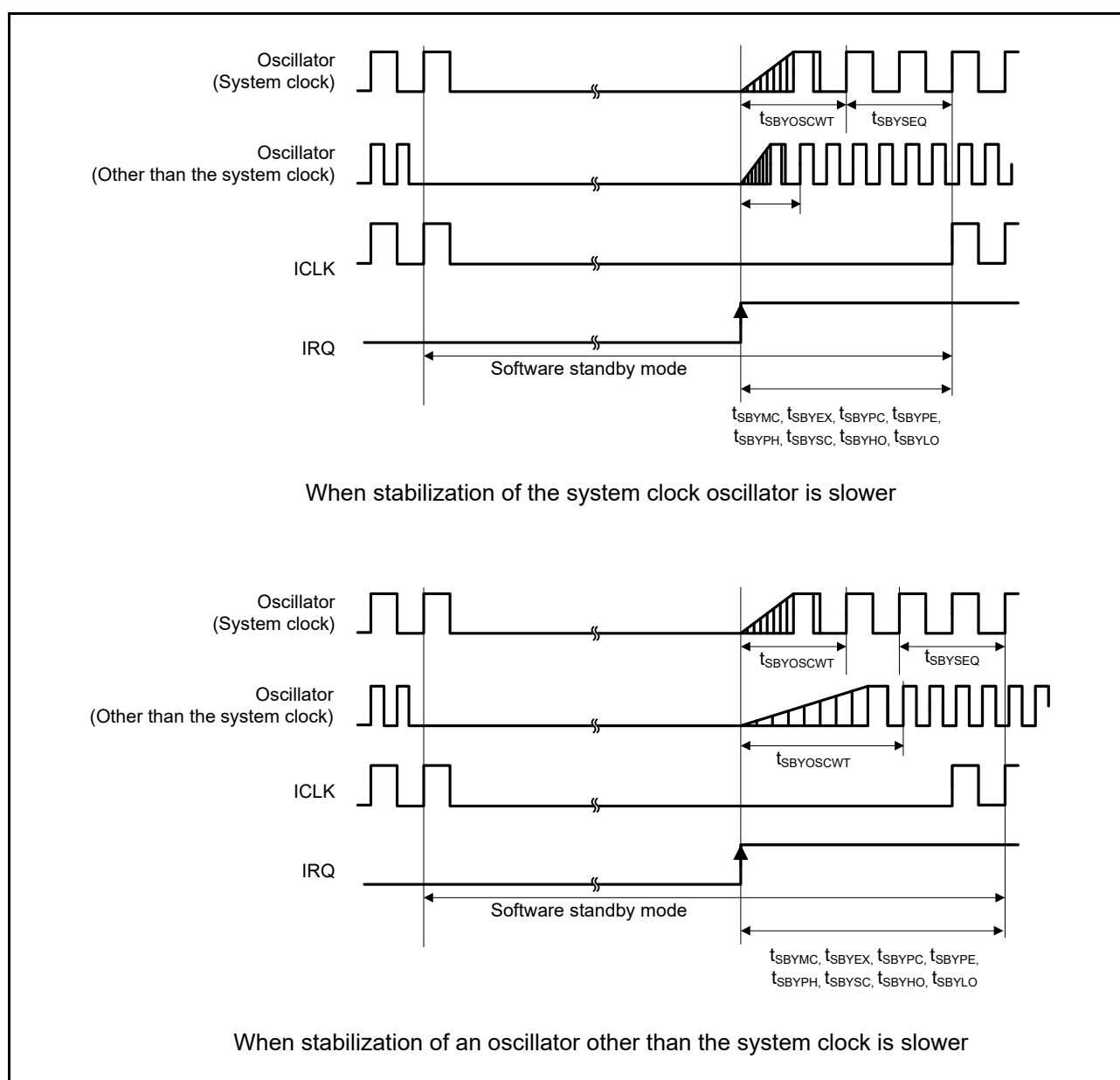
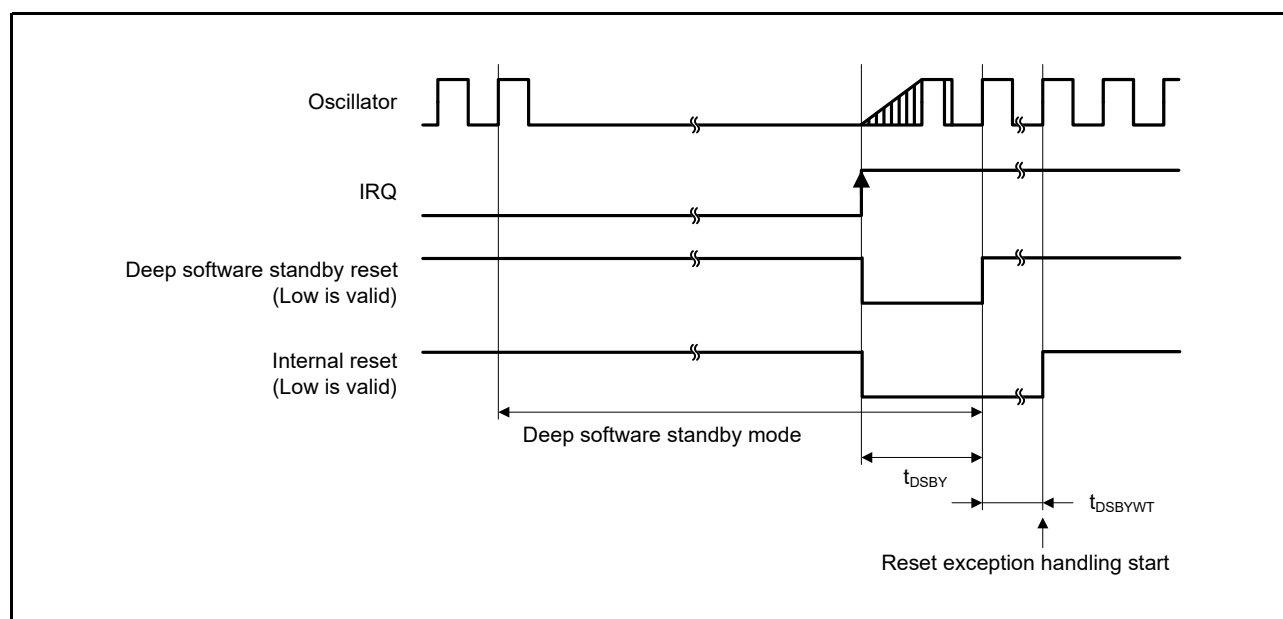


Figure 2.12 Software Standby Mode Recovery Timing

**Table 2.23 Timing of Recovery from Low Power Consumption Modes (2)**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = VCC\_USB = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq VREFH0 \leq AVCC0$ ,  
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS\_USB = 0$  V,  
 $T_a = T_{opr}$

| Item                                                     | Symbol       | Min. | Typ. | Max. | Unit       | Test Conditions |
|----------------------------------------------------------|--------------|------|------|------|------------|-----------------|
| Recovery time from deep software standby mode            | $t_{DSBY}$   | —    | —    | 0.9  | ms         | Figure 2.13     |
| Wait time after recovery from deep software standby mode | $t_{DSBYWT}$ | 23   | —    | 24   | $t_{Lcyc}$ |                 |

**Figure 2.13 Deep Software Standby Mode Recovery Timing**

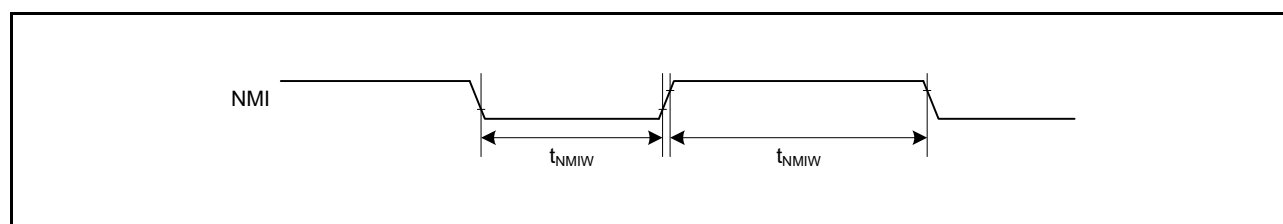
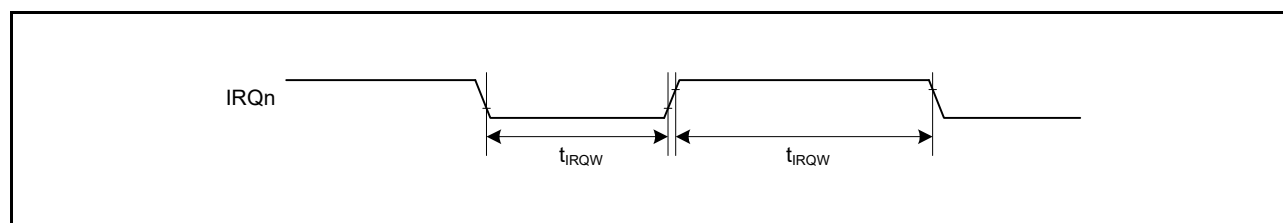
## 2.4.4 Control Signal Timing

**Table 2.24 Control Signal Timing**

Conditions:  $VCC = AVCC0 = AVCC1 = VCC\_USB = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq VREFH0 \leq AVCC0$ ,  
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS\_USB = 0$  V,  
 $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$

| Item            | Symbol     | Min.*1               | Typ. | Max. | Unit | Test Conditions*1                             |
|-----------------|------------|----------------------|------|------|------|-----------------------------------------------|
| NMI pulse width | $t_{NMIW}$ | 200                  | —    | —    | ns   | $2 \times t_{PBcyc} \leq 200$ ns, Figure 2.14 |
|                 |            | $2 \times t_{PBcyc}$ | —    | —    |      | $2 \times t_{PBcyc} > 200$ ns, Figure 2.14    |
| IRQ pulse width | $t_{IRQW}$ | 200                  | —    | —    | ns   | $2 \times t_{PBcyc} \leq 200$ ns, Figure 2.15 |
|                 |            | $2 \times t_{PBcyc}$ | —    | —    |      | $2 \times t_{PBcyc} > 200$ ns, Figure 2.15    |

Note 1.  $t_{PBcyc}$ : PCLKB cycle

**Figure 2.14 NMI Interrupt Input Timing****Figure 2.15 IRQ Interrupt Input Timing**

## 2.4.5 Bus Timing

**Table 2.25 Bus Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $ICLK = PCLKA = 8$  to  $120$  MHz,  $PCLKB = BCLK = SDCLK = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the driving ability control register.

| Item                            | Symbol     | Min. | Max. | Unit | Test Conditions               |
|---------------------------------|------------|------|------|------|-------------------------------|
| Address delay time              | $t_{AD}$   | —    | 12.5 | ns   | Figure 2.16 to<br>Figure 2.21 |
| Byte control delay time         | $t_{BCD}$  | —    | 12.5 | ns   |                               |
| CS# delay time                  | $t_{CSD}$  | —    | 12.5 | ns   |                               |
| ALE delay time                  | $t_{ALED}$ | —    | 12.5 | ns   |                               |
| RD# delay time                  | $t_{RSD}$  | —    | 12.5 | ns   |                               |
| Read data setup time            | $t_{RDS}$  | 12.5 | —    | ns   |                               |
| Read data hold time             | $t_{RDH}$  | 0    | —    | ns   |                               |
| WR# delay time                  | $t_{WRD}$  | —    | 12.5 | ns   |                               |
| Write data delay time           | $t_{WDD}$  | —    | 12.5 | ns   |                               |
| Write data hold time            | $t_{WDH}$  | 0    | —    | ns   |                               |
| WAIT# setup time                | $t_{WTS}$  | 12.5 | —    | ns   | Figure 2.22                   |
| WAIT# hold time                 | $t_{WTH}$  | 0    | —    | ns   |                               |
| Address delay time 2 (SDRAM)    | $t_{AD2}$  | 1    | 12.5 | ns   | Figure 2.23 to<br>Figure 2.29 |
| CS# delay time 2 (SDRAM)        | $t_{CSD2}$ | 1    | 12.5 | ns   |                               |
| DQM delay time (SDRAM)          | $t_{DQMD}$ | 1    | 12.5 | ns   |                               |
| CKE delay time (SDRAM)          | $t_{CKED}$ | 1    | 12.5 | ns   |                               |
| Read data setup time 2 (SDRAM)  | $t_{RDS2}$ | 10   | —    | ns   |                               |
| Read data hold time 2 (SDRAM)   | $t_{RDH2}$ | 0    | —    | ns   |                               |
| Write data delay time 2 (SDRAM) | $t_{WDD2}$ | —    | 12.5 | ns   |                               |
| Write data hold time 2 (SDRAM)  | $t_{WDH2}$ | 1    | —    | ns   |                               |
| WE# delay time (SDRAM)          | $t_{WED}$  | 1    | 12.5 | ns   |                               |
| RAS# delay time (SDRAM)         | $t_{RASD}$ | 1    | 12.5 | ns   |                               |
| CAS# delay time (SDRAM)         | $t_{CASD}$ | 1    | 12.5 | ns   |                               |

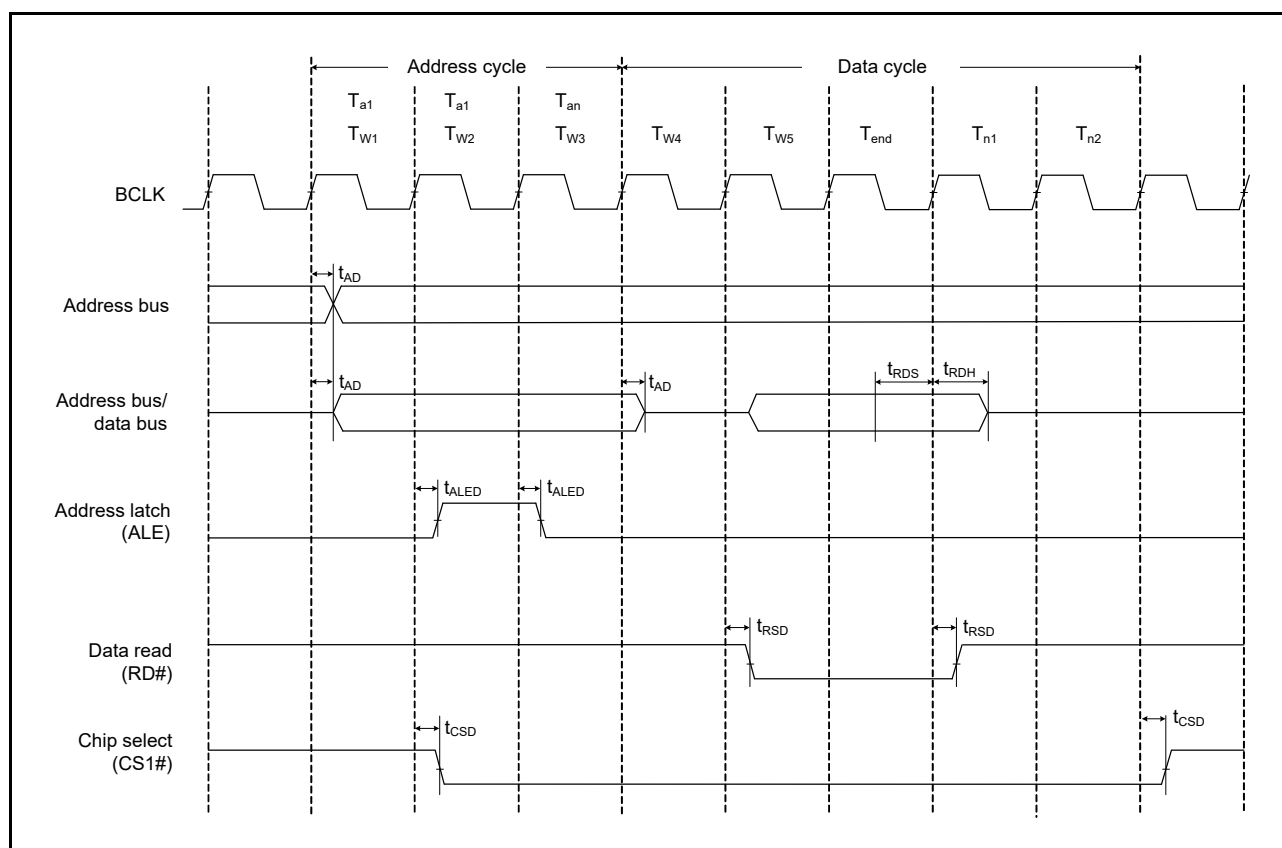


Figure 2.16 Address/Data Multiplexed Bus Read Access Timing

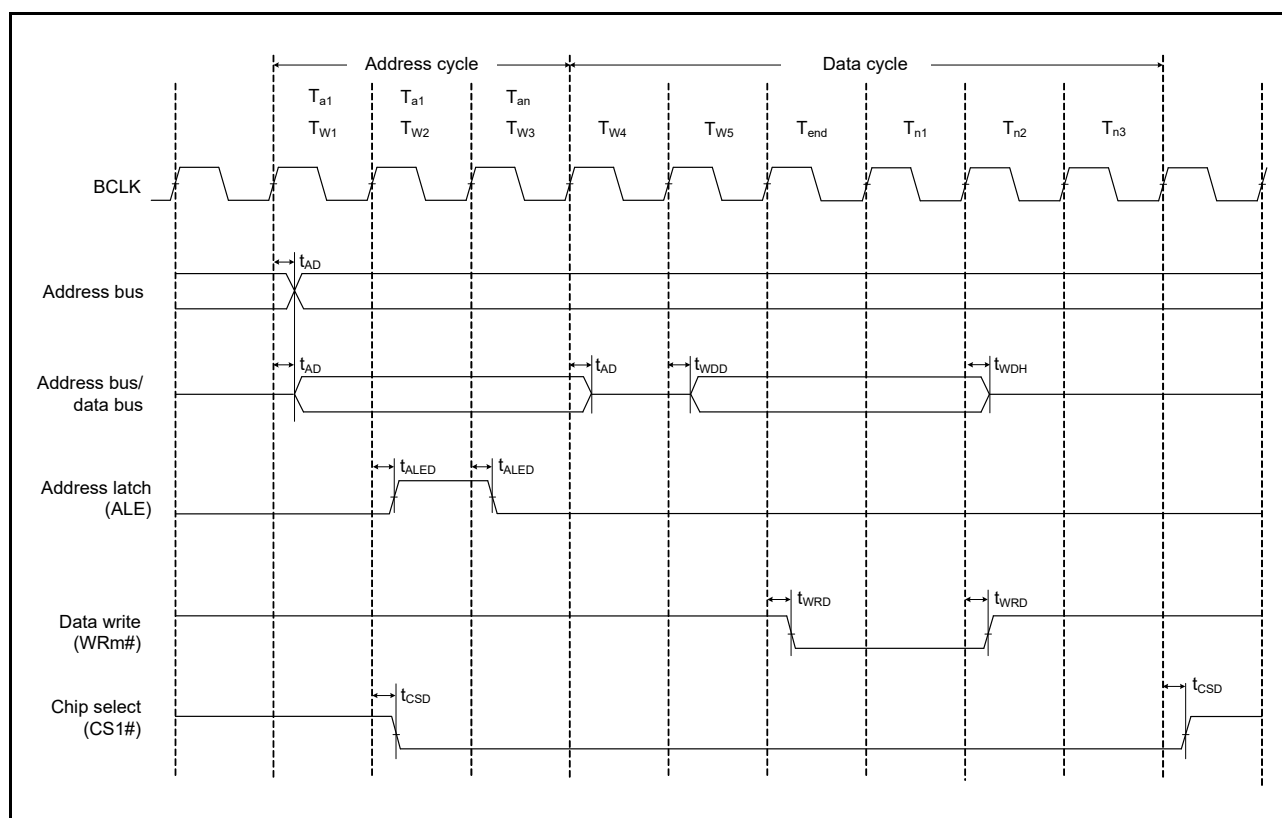
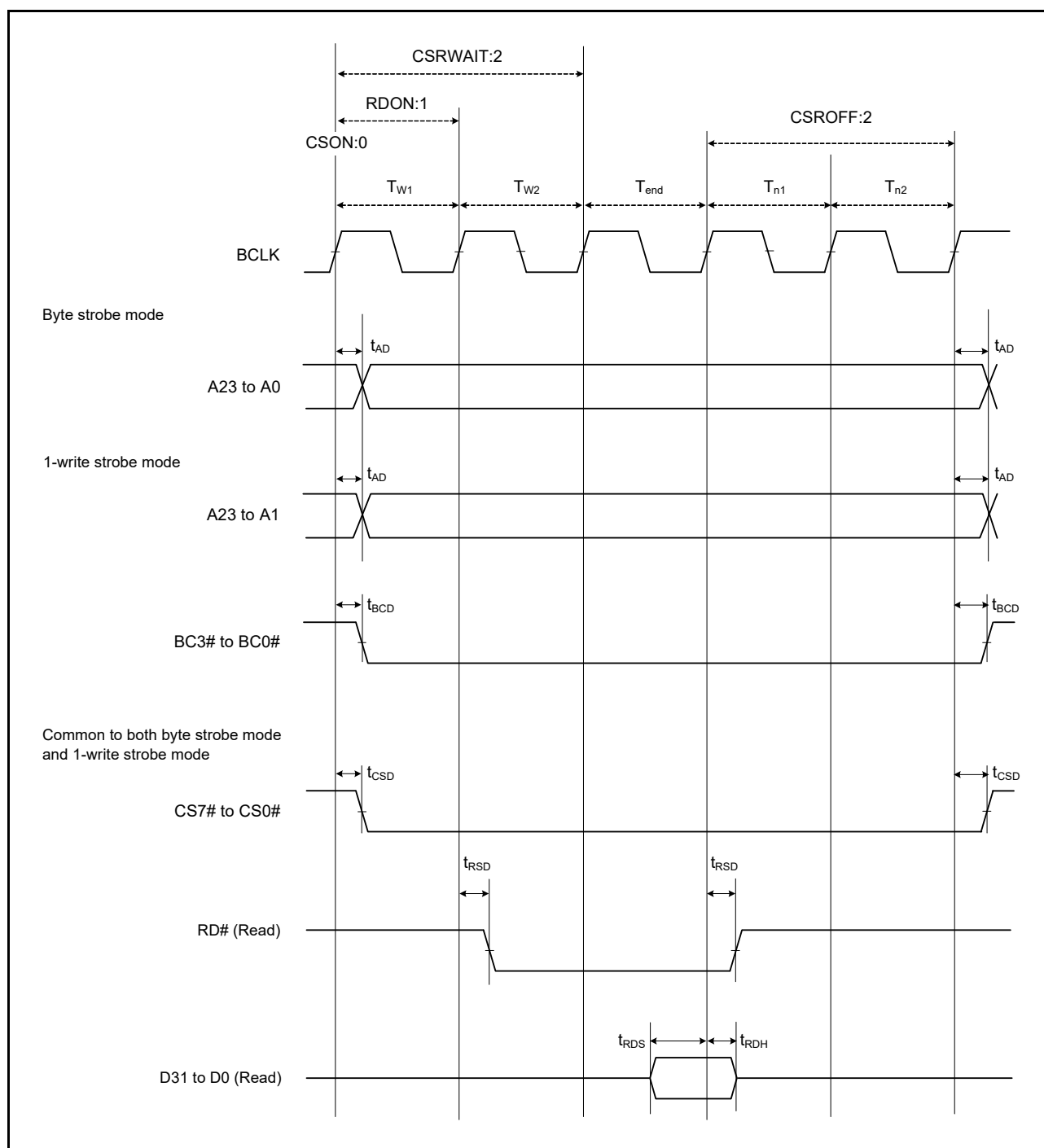
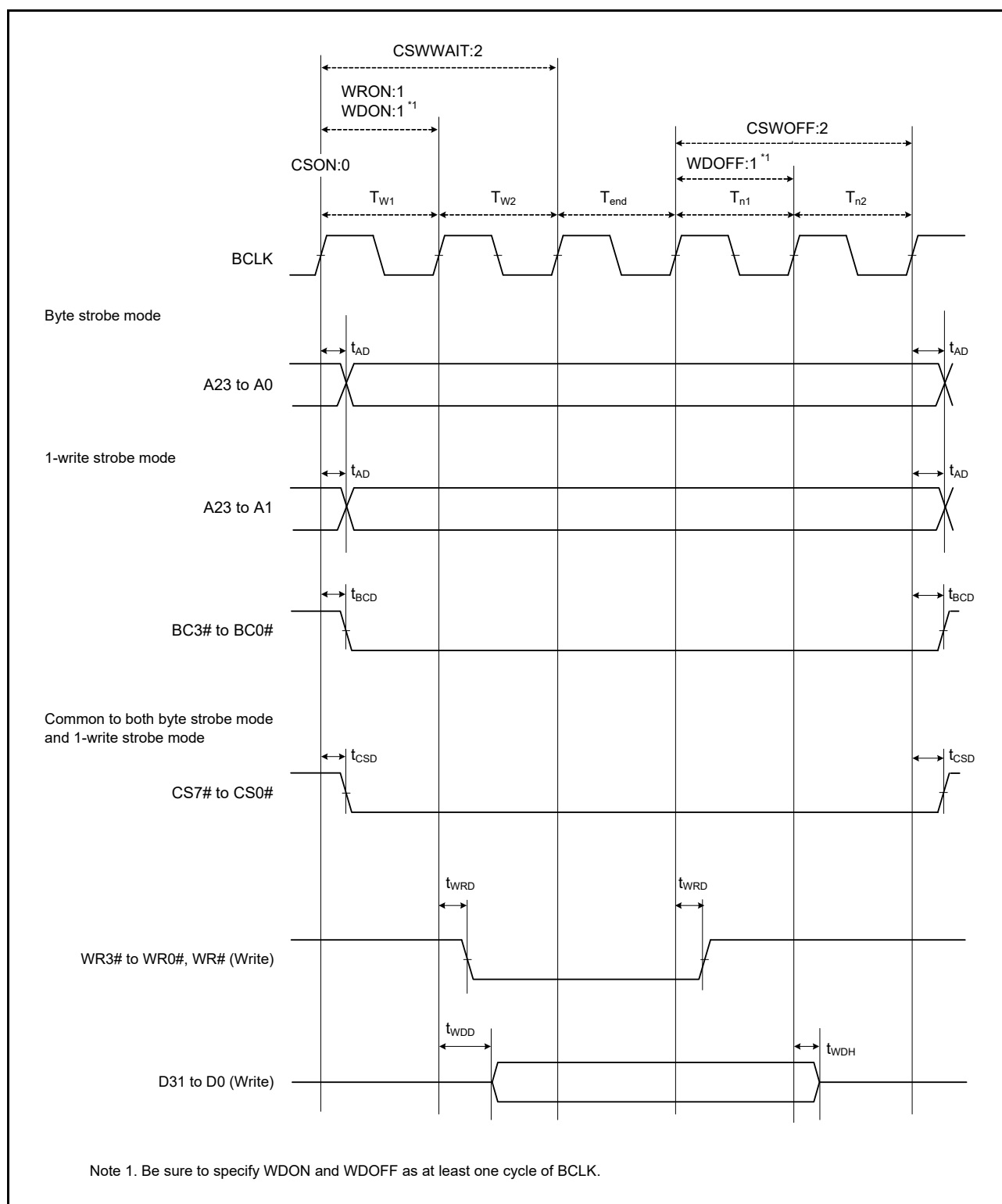


Figure 2.17 Address/Data Multiplexed Bus Write Access Timing



**Figure 2.18 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)**



**Figure 2.19 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)**

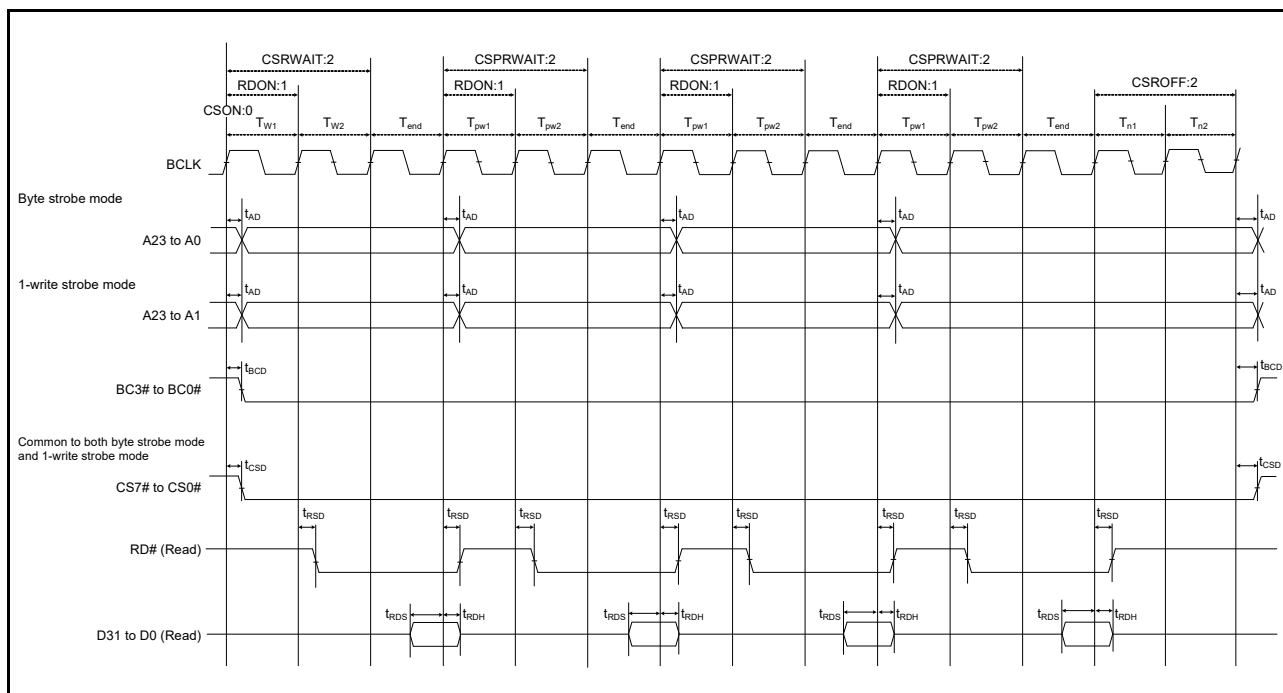


Figure 2.20 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

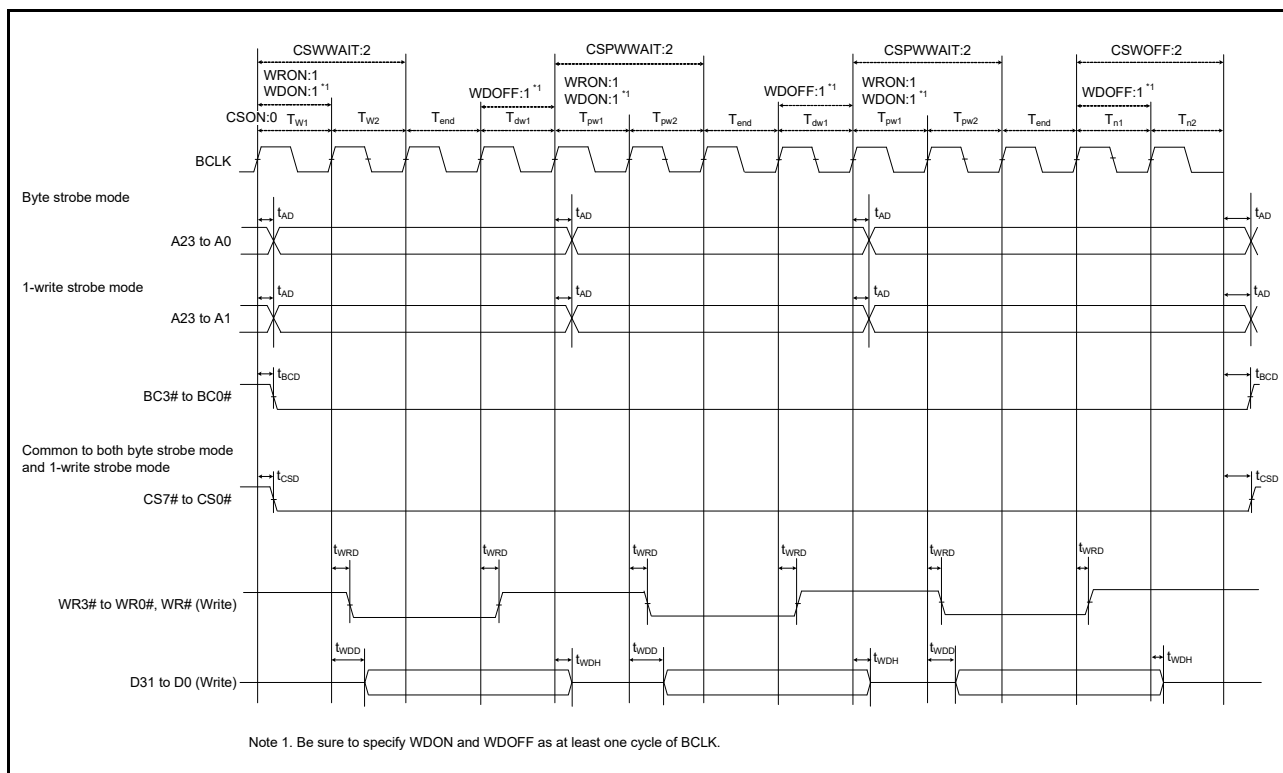
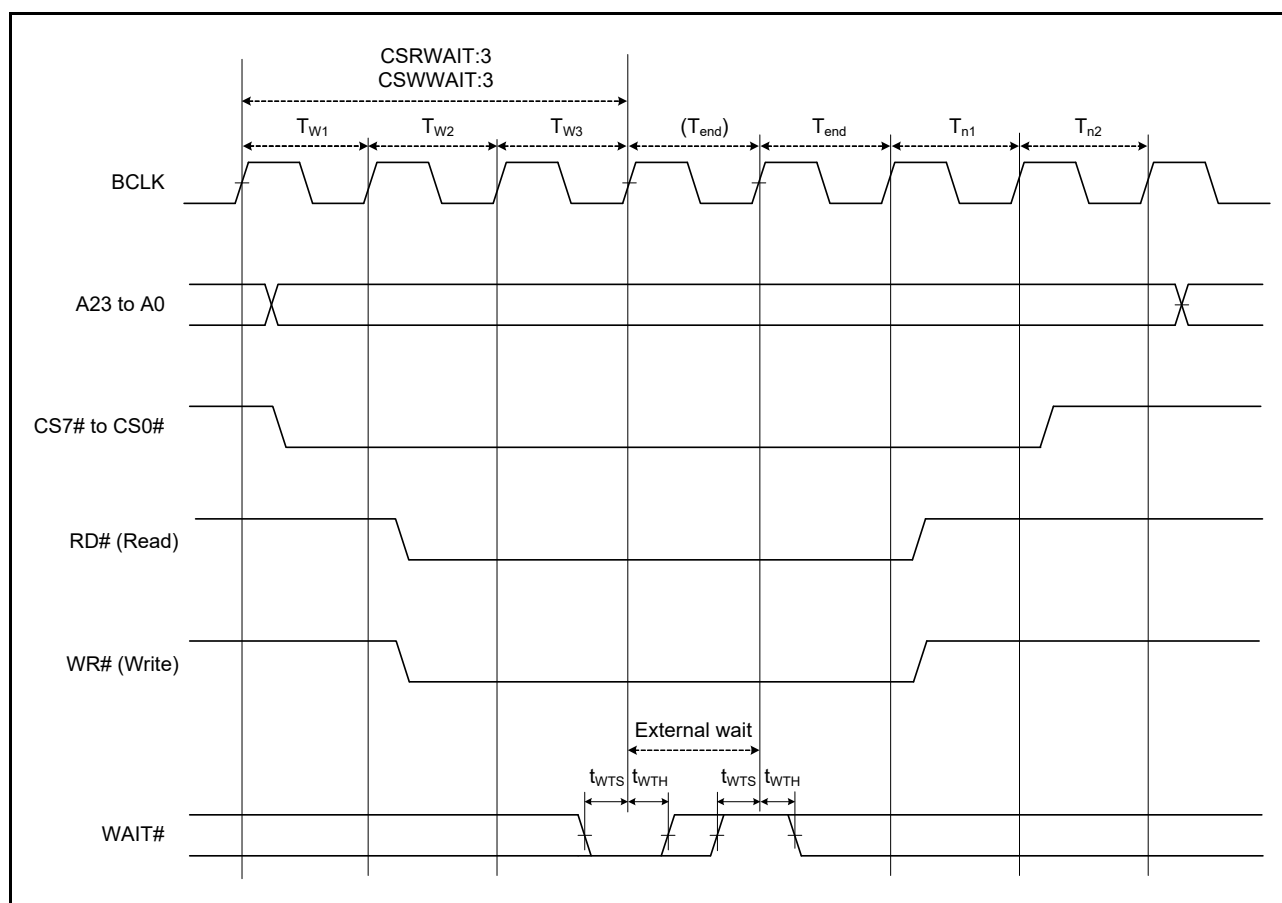


Figure 2.21 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)



**Figure 2.22 External Bus Timing/External Wait Control**

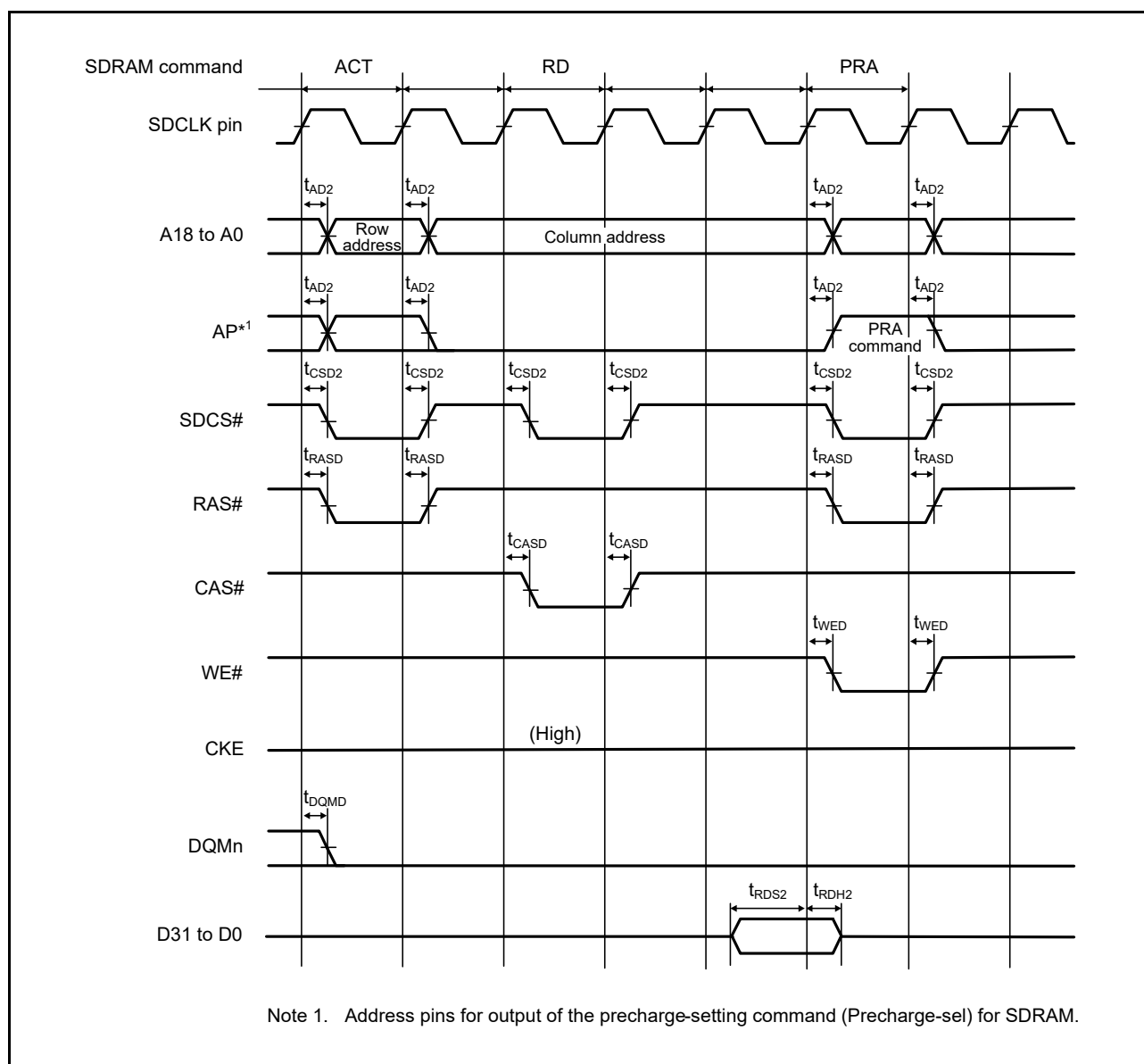


Figure 2.23 SDRAM Space Single Read Bus Timing

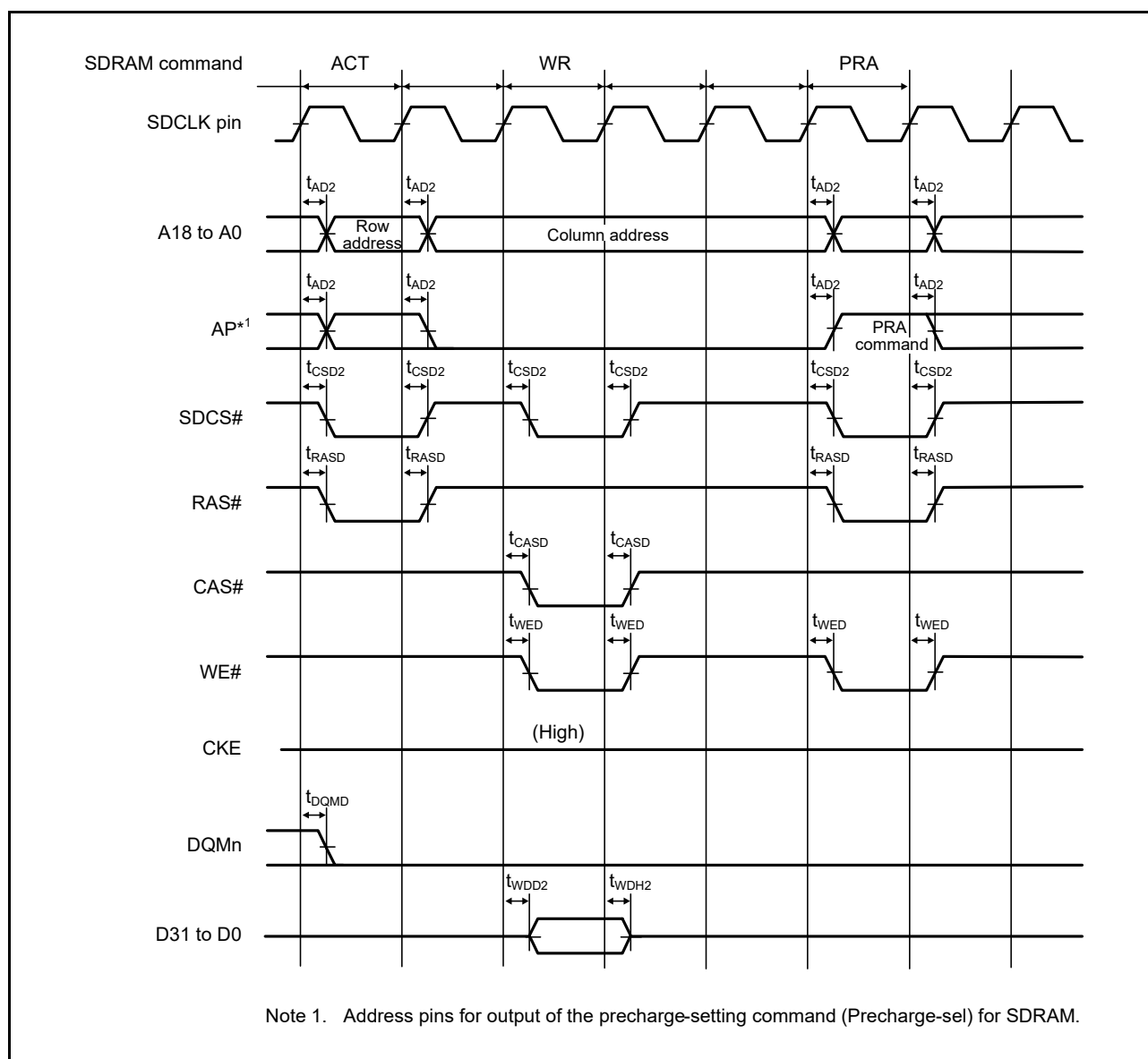
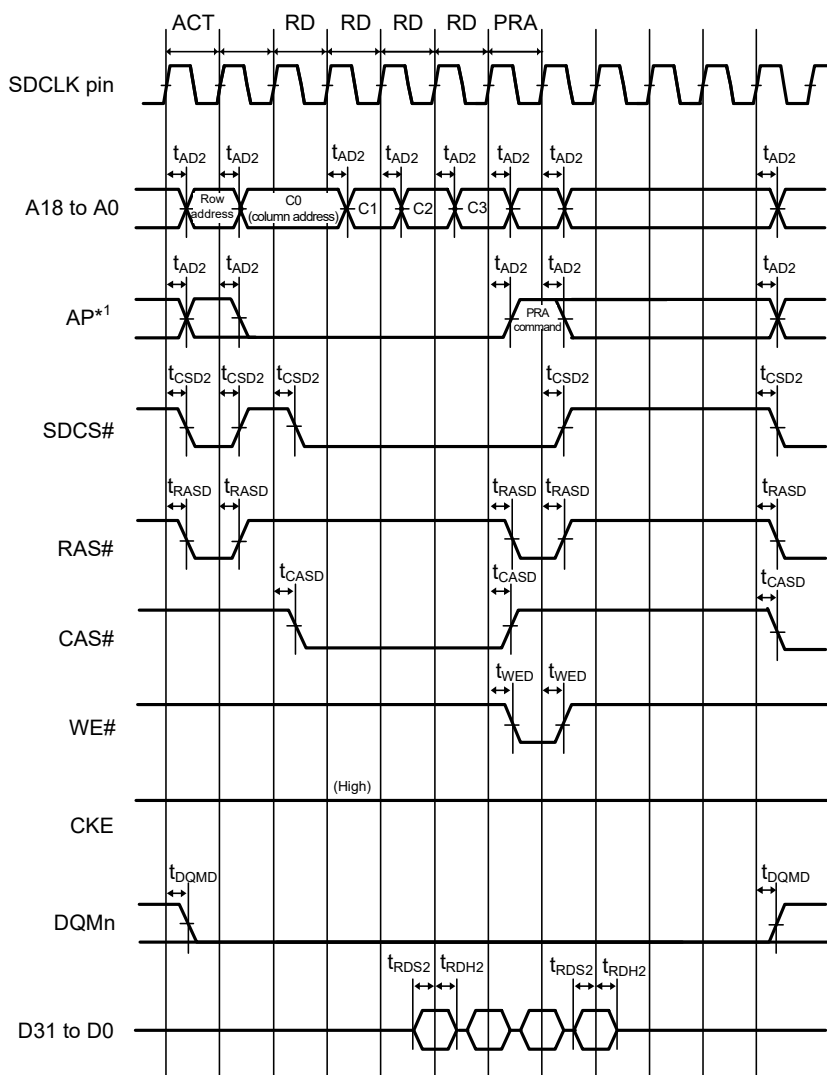
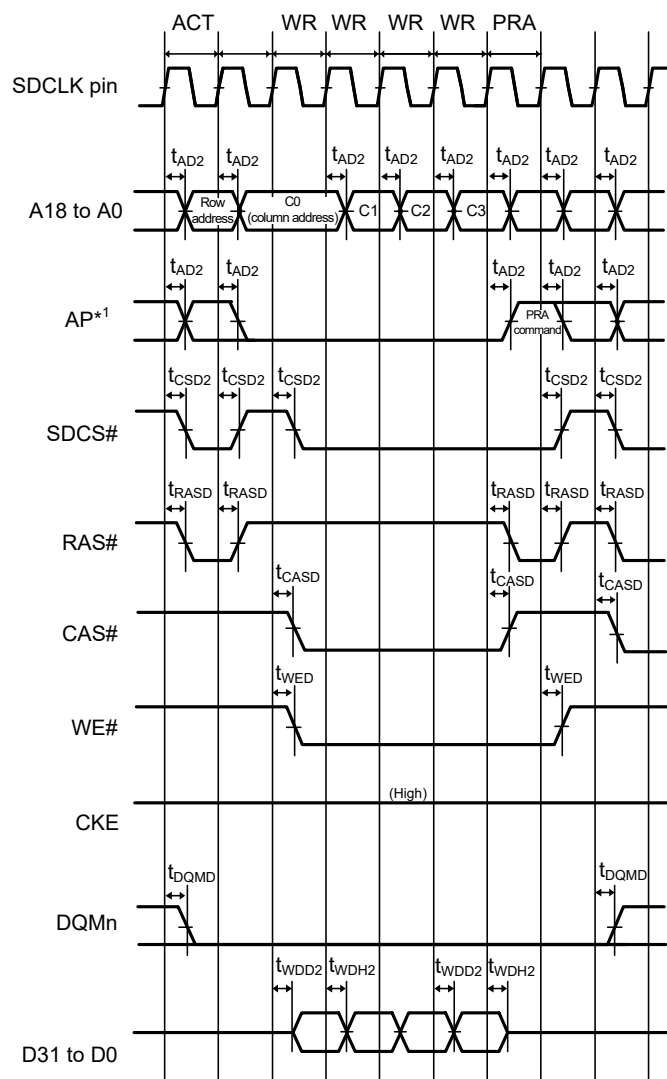


Figure 2.24 SDRAM Space Single Write Bus Timing



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 2.25 SDRAM Space Multiple Read Bus Timing**



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.26 SDRAM Space Multiple Write Bus Timing

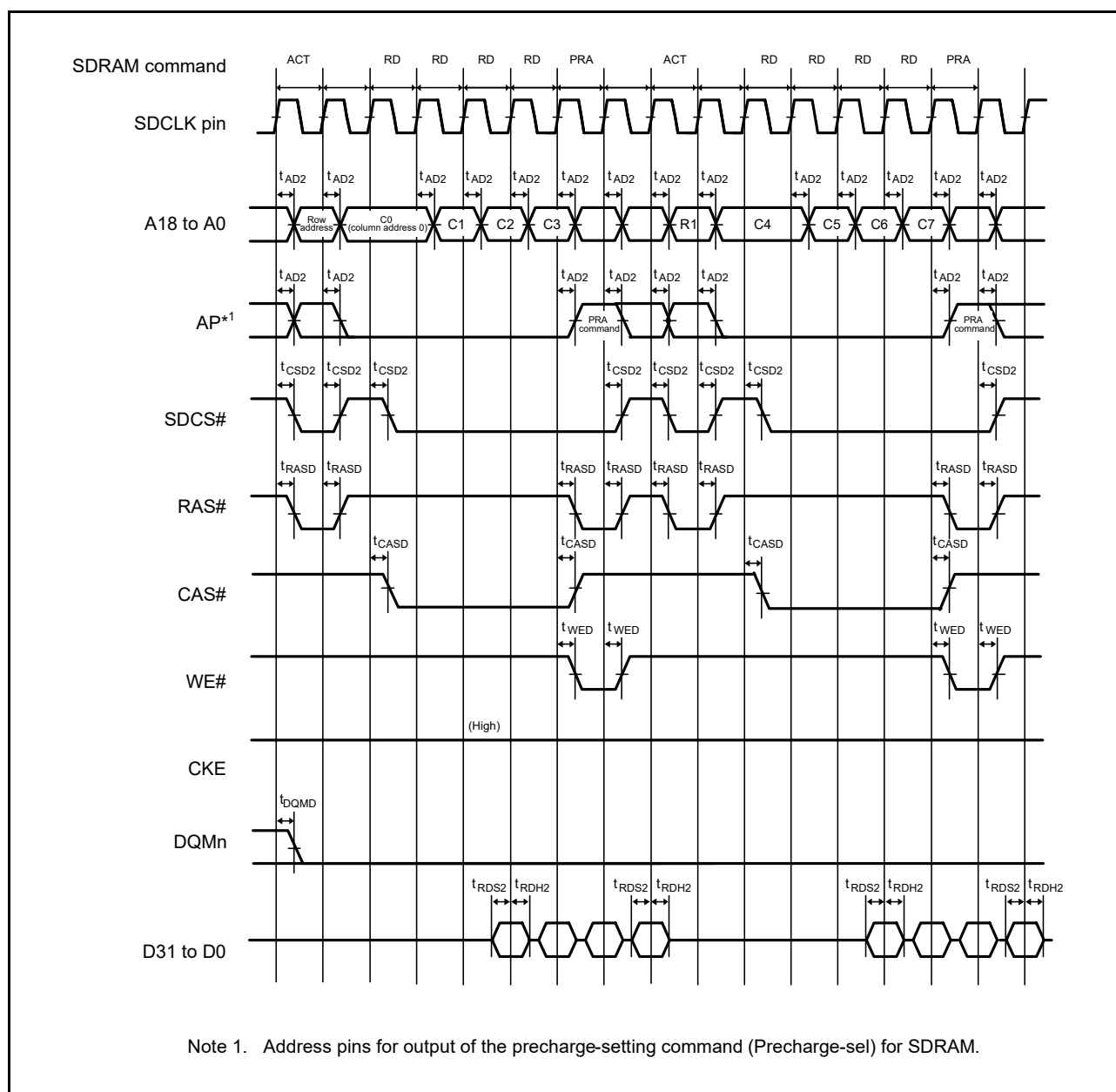
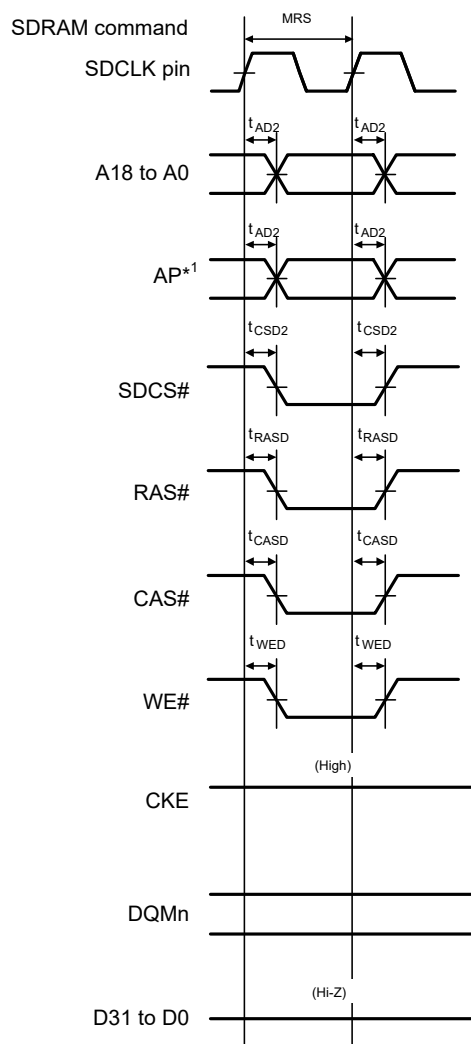
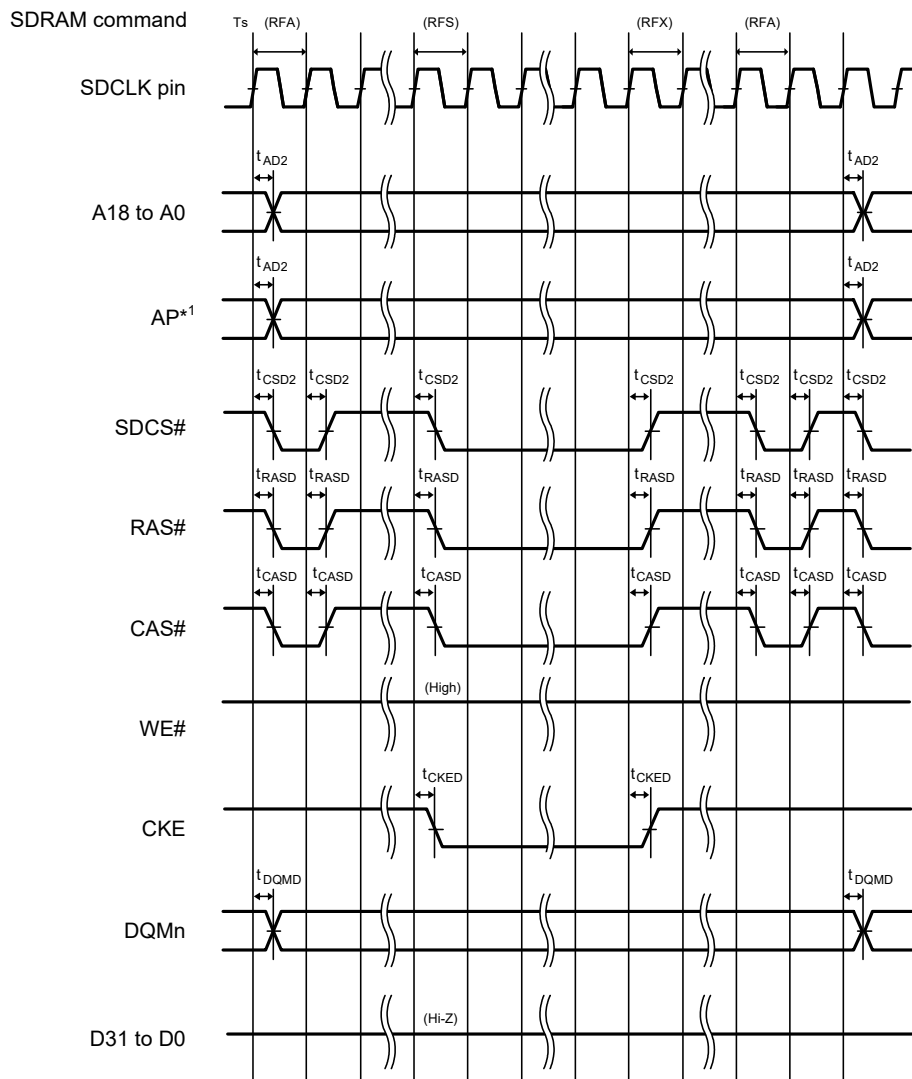


Figure 2.27 SDRAM Space Multiple Read Line Stride Bus Timing



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.28 SDRAM Space Mode Register Set Bus Timing



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

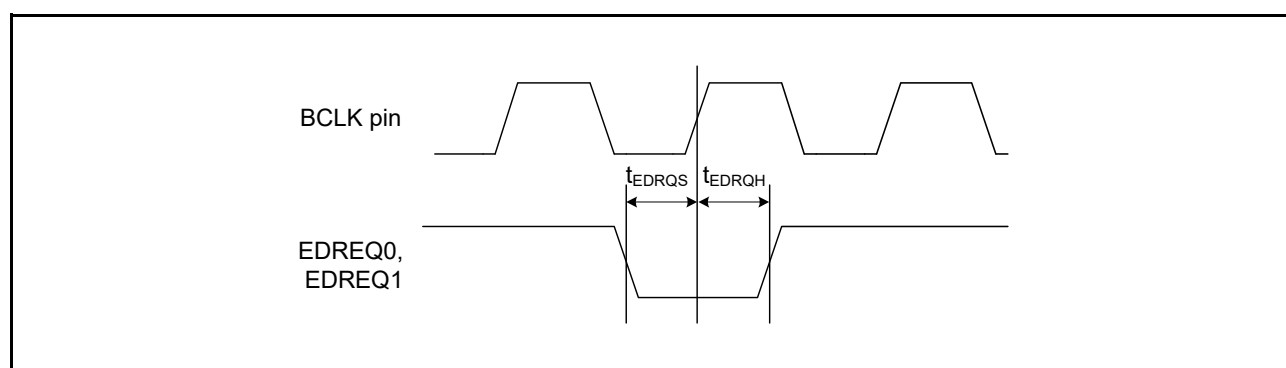
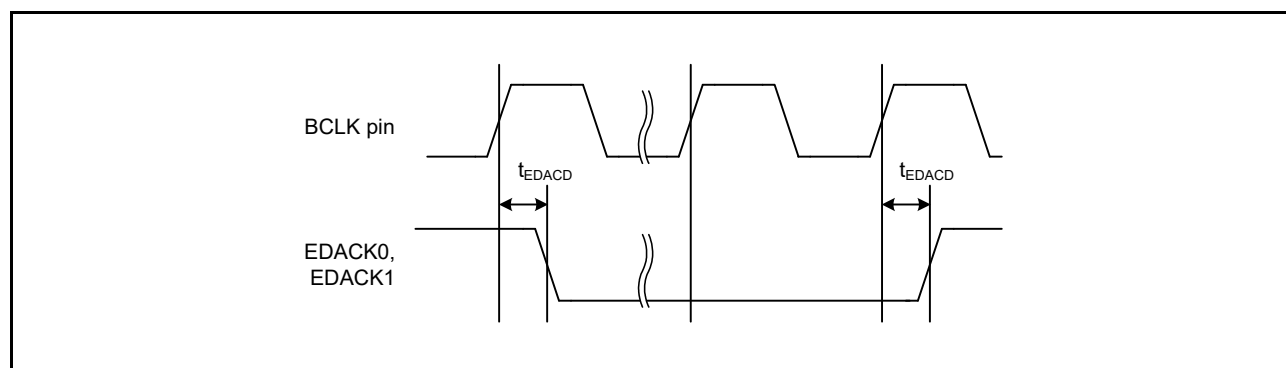
**Figure 2.29 SDRAM Space Self-Refresh Bus Timing**

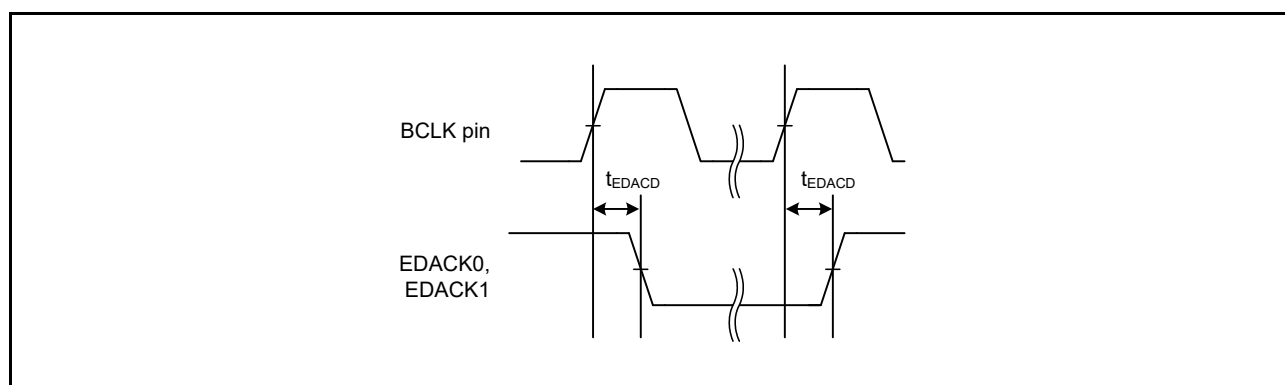
## 2.4.6 EXDMAC Timing

**Table 2.26 EXDMAC Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $ICLK = PCLKA = 8$  to  $120$  MHz,  $PCLKB = BCLK = SDCLK = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the driving ability control register.

|        | Item             | Symbol      | Min. | Max. | Unit | Test Conditions             |
|--------|------------------|-------------|------|------|------|-----------------------------|
| EXDMAC | EDREQ setup time | $t_{EDRQS}$ | 13   | —    | ns   | Figure 2.30                 |
|        | EDREQ hold time  | $t_{EDRQH}$ | 2    | —    | ns   |                             |
|        | EDACK delay time | $t_{EDACD}$ | —    | 13   | ns   | Figure 2.31,<br>Figure 2.32 |

**Figure 2.30 EDREQ0 and EDREQ1 Input Timing****Figure 2.31 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area)**



**Figure 2.32 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)**

## 2.4.7 Timing of On-Chip Peripheral Modules

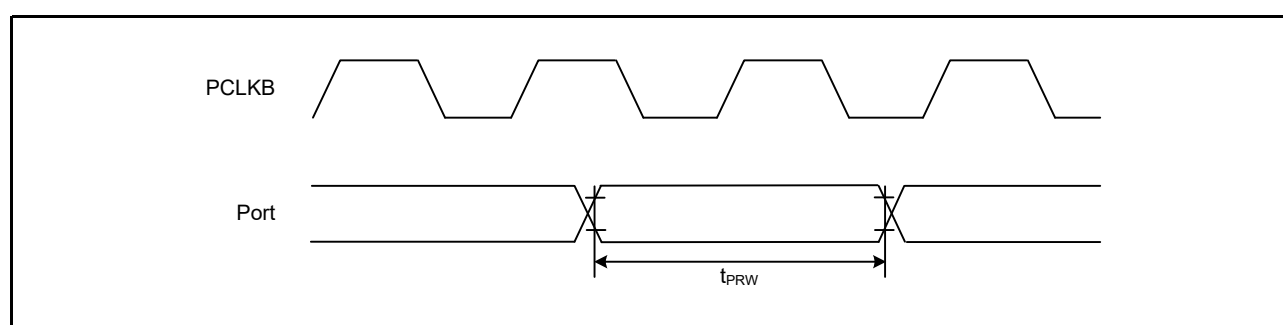
### 2.4.7.1 I/O Port

**Table 2.27 I/O Port Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the driving ability control register.

| Item      |                        | Symbol    | Min. | Max. | Unit*1      | Test Conditions |
|-----------|------------------------|-----------|------|------|-------------|-----------------|
| I/O ports | Input data pulse width | $t_{PRW}$ | 1.5  | —    | $t_{PBcyc}$ | Figure 2.33     |

Note 1.  $t_{PBcyc}$ : PCLKB cycle



**Figure 2.33 I/O Port Input Timing**

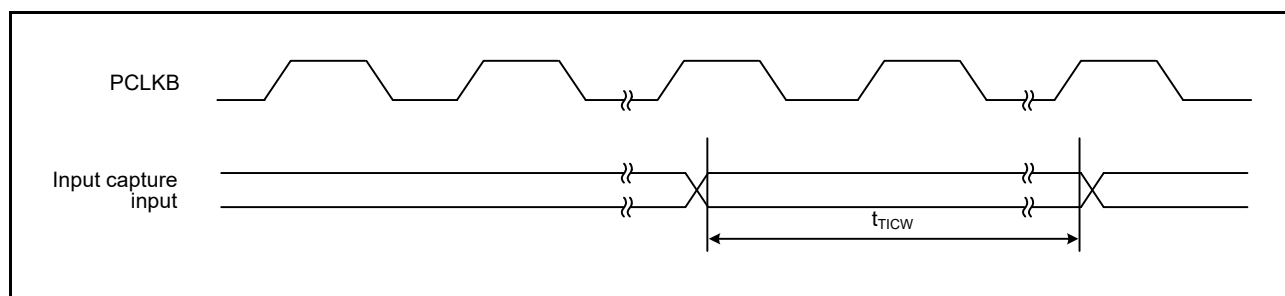
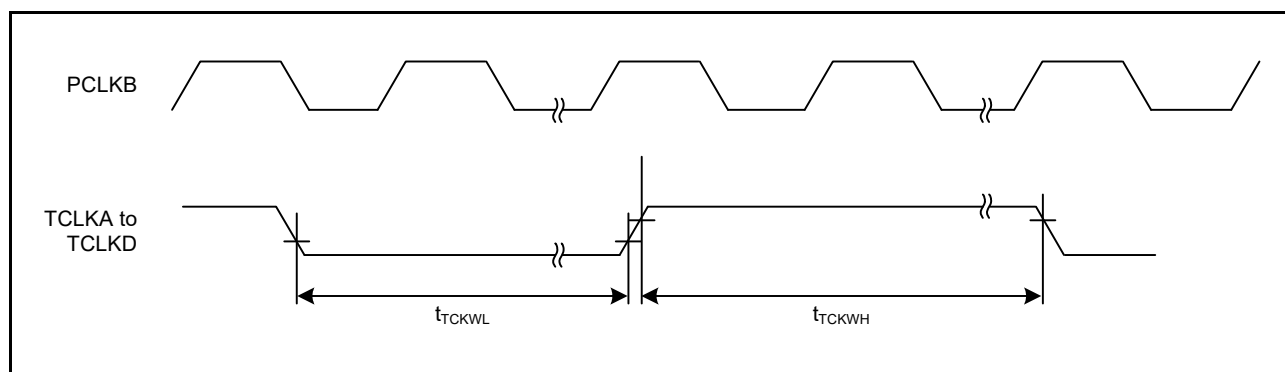
## 2.4.7.2 TPU

**Table 2.28 TPU Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the driving ability control register.

| Item |                                 |                     | Symbol                       | Min. | Max. | Unit*1      | Test Conditions |
|------|---------------------------------|---------------------|------------------------------|------|------|-------------|-----------------|
| TPU  | Input capture input pulse width | Single-edge setting | $t_{TICW}$                   | 1.5  | —    | $t_{PBcyc}$ | Figure 2.34     |
|      |                                 | Both-edge setting   |                              | 2.5  | —    |             |                 |
|      | Timer clock pulse width         | Single-edge setting | $t_{TCKWH}$ ,<br>$t_{TCKWL}$ | 1.5  | —    | $t_{PBcyc}$ | Figure 2.35     |
|      |                                 | Both-edge setting   |                              | 2.5  | —    |             |                 |
|      |                                 | Phase counting mode |                              | 2.5  | —    |             |                 |

Note 1.  $t_{PBcyc}$ : PCLKB cycle

**Figure 2.34 TPU Input Capture Input Timing****Figure 2.35 TPU Clock Input Timing**

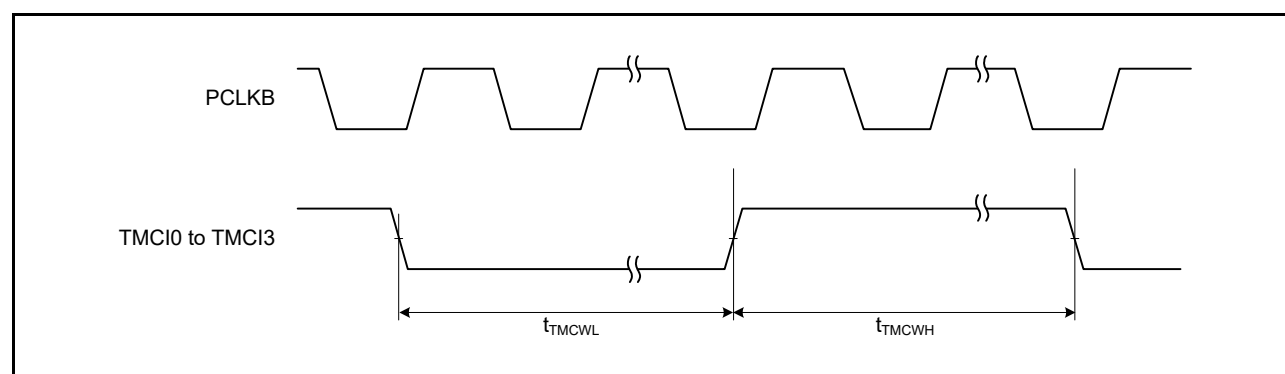
## 2.4.7.3 TMR

**Table 2.29 TMR Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the driving ability control register.

| Item |                         |                     | Symbol                       | Min. | Max. | Unit*1      | Test Conditions |
|------|-------------------------|---------------------|------------------------------|------|------|-------------|-----------------|
| TMR  | Timer clock pulse width | Single-edge setting | $t_{TMCWH}$ ,<br>$t_{TMCWL}$ | 1.5  | —    | $t_{PBcyc}$ | Figure 2.36     |
|      |                         | Both-edge setting   |                              | 2.5  | —    |             |                 |

Note 1.  $t_{PBcyc}$ : PCLKB cycle

**Figure 2.36 TMR Clock Input Timing**

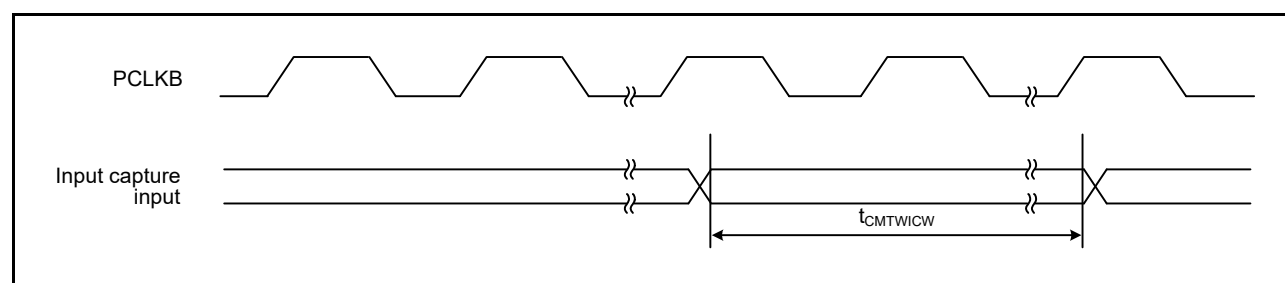
## 2.4.7.4 CMTW

**Table 2.30 CMTW Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the driving ability control register.

| Item |                                 |                     | Symbol         | Min. | Max. | Unit*1      | Test Conditions |
|------|---------------------------------|---------------------|----------------|------|------|-------------|-----------------|
| CMTW | Input capture input pulse width | Single-edge setting | $t_{CMTWTICW}$ | 1.5  | —    | $t_{PBcyc}$ | Figure 2.37     |
|      |                                 | Both-edge setting   |                | 2.5  | —    |             |                 |

Note 1.  $t_{PBcyc}$ : PCLKB cycle

**Figure 2.37 CMTW Input Capture Input Timing**

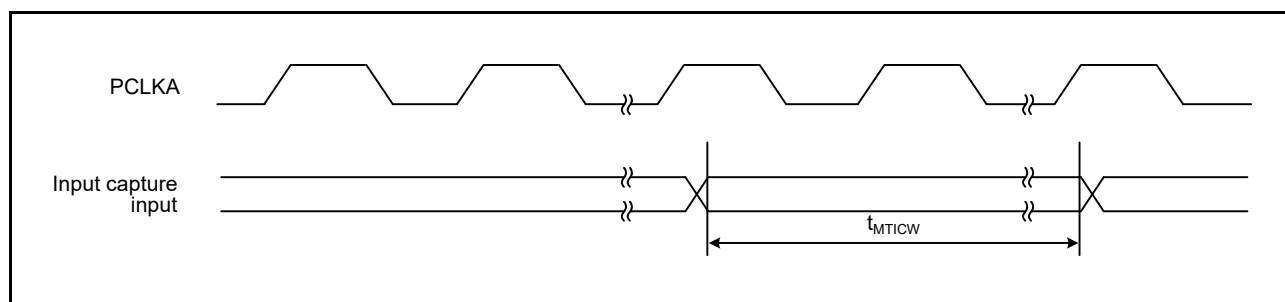
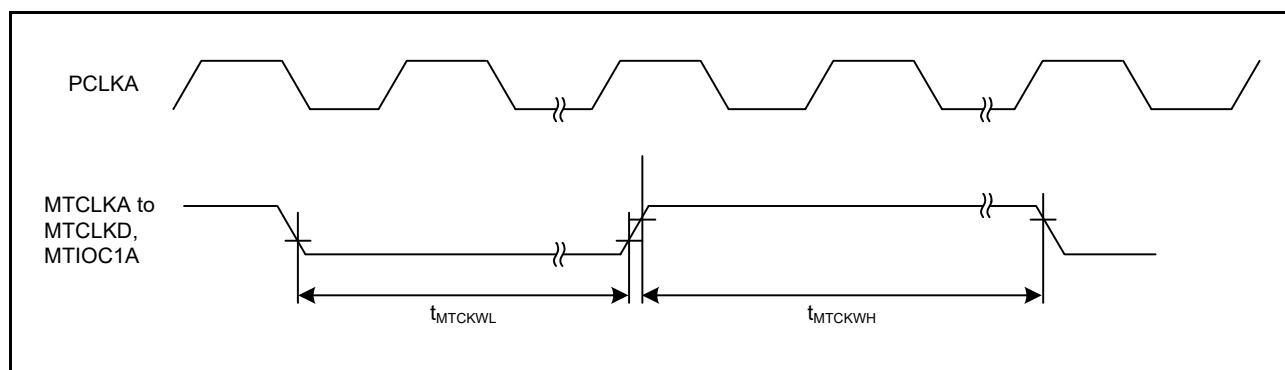
## 2.4.7.5 MTU3

**Table 2.31 MTU3 Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the driving ability control register.

| Item |                                 |                     | Symbol                         | Min. | Max. | Unit*1      | Test Conditions |
|------|---------------------------------|---------------------|--------------------------------|------|------|-------------|-----------------|
| MTU3 | Input capture input pulse width | Single-edge setting | $t_{MTICW}$                    | 1.5  | —    | $t_{PAcyc}$ | Figure 2.38     |
|      |                                 | Both-edge setting   |                                | 2.5  | —    |             |                 |
|      | Timer clock pulse width         | Single-edge setting | $t_{MTCKWH}$ ,<br>$t_{MTCKWL}$ | 1.5  | —    | $t_{PAcyc}$ | Figure 2.39     |
|      |                                 | Both-edge setting   |                                | 2.5  | —    |             |                 |
|      |                                 | Phase counting mode |                                | 2.5  | —    |             |                 |

Note 1.  $t_{PAcyc}$ : PCLKA cycle

**Figure 2.38 MTU3 Input Capture Input Timing****Figure 2.39 MTU3 Clock Input Timing**

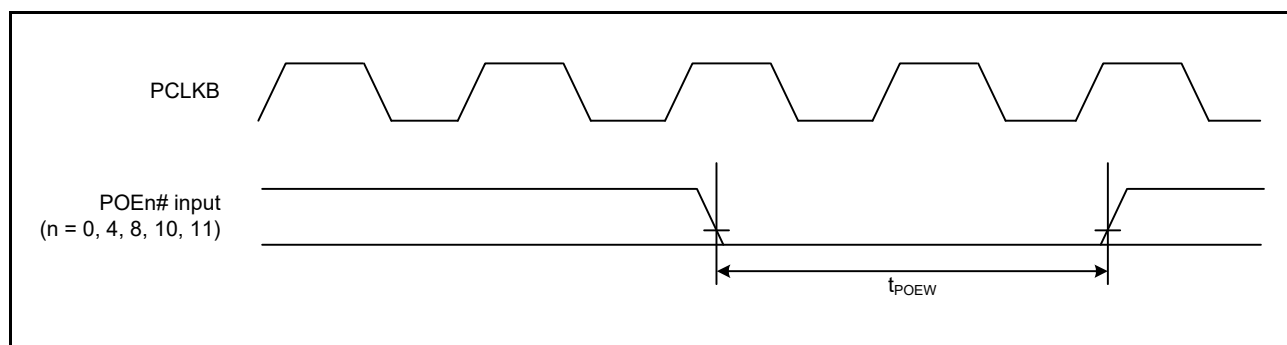
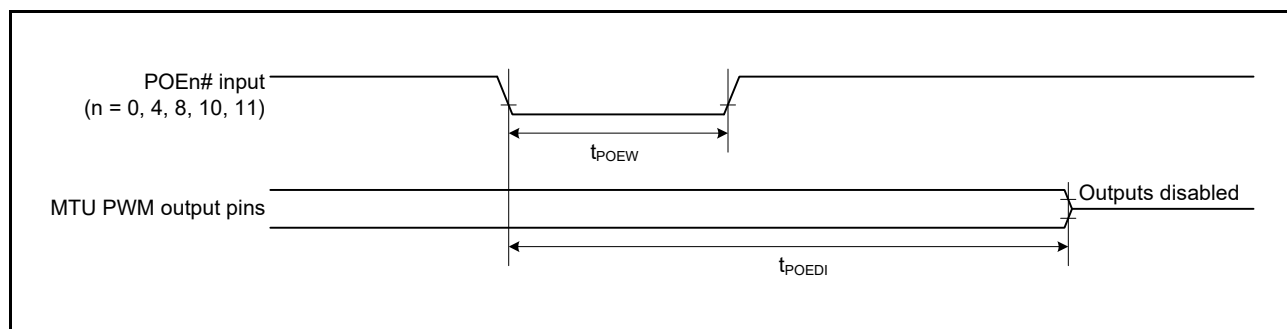
## 2.4.7.6 POE3

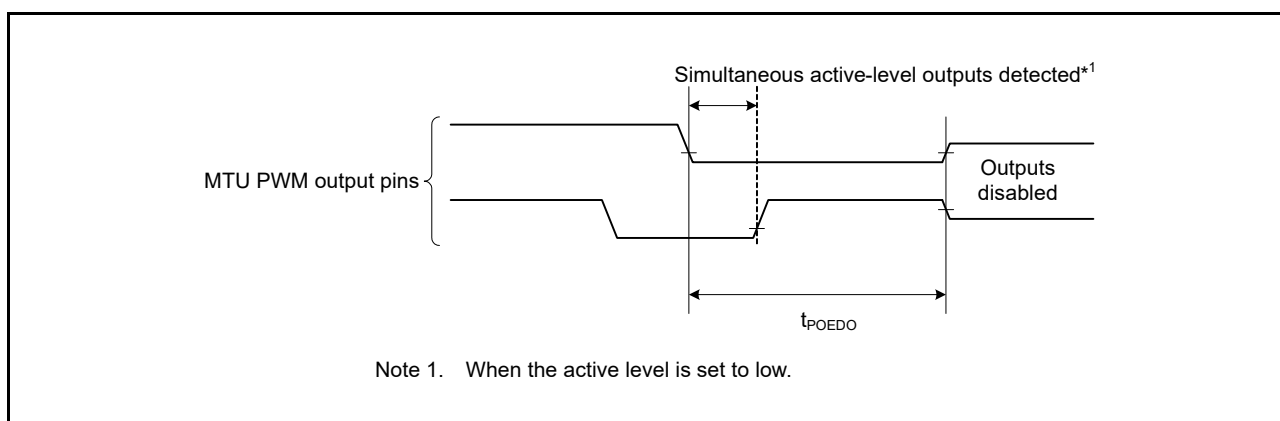
**Table 2.32 POE3 Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the drive capacity control register.

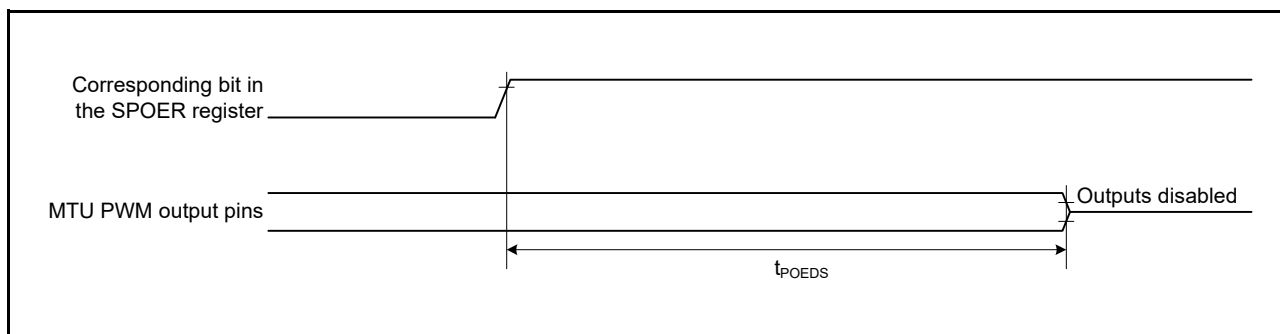
| Item                | Symbol                                           | Min.                | Typ. | Max. | Unit*1         | Test Conditions                                                                                                   |
|---------------------|--------------------------------------------------|---------------------|------|------|----------------|-------------------------------------------------------------------------------------------------------------------|
| POE                 | POEn# input pulse width<br>(n = 0, 4, 8, 10, 11) | t <sub>POEW</sub>   | 1.5  | —    | —              | t <sub>PBcyc</sub> Figure 2.40                                                                                    |
| Output disable time | Transition of the POEn# signal level             | t <sub>POEDI</sub>  | —    | —    | 5 PCLKB + 0.24 | μs Figure 2.41<br>When detecting falling edges<br>(ICSRm.POEnM[3:0] = 0000b<br>(m = 1 to 5; n = 0, 4, 8, 10, 11)) |
|                     | Simultaneous conduction of output pins           | t <sub>POEDO</sub>  | —    | —    | 3 PCLKB + 0.2  | μs Figure 2.42                                                                                                    |
|                     | Register setting                                 | t <sub>POEDS</sub>  | —    | —    | 1 PCLKB + 0.2  | μs Figure 2.43<br>Time for access to the register is not included.                                                |
|                     | Oscillation stop detection                       | t <sub>POEDOS</sub> | —    | —    | 21             | μs Figure 2.44                                                                                                    |

Note 1. t<sub>PBcyc</sub>: PCLKB cycle

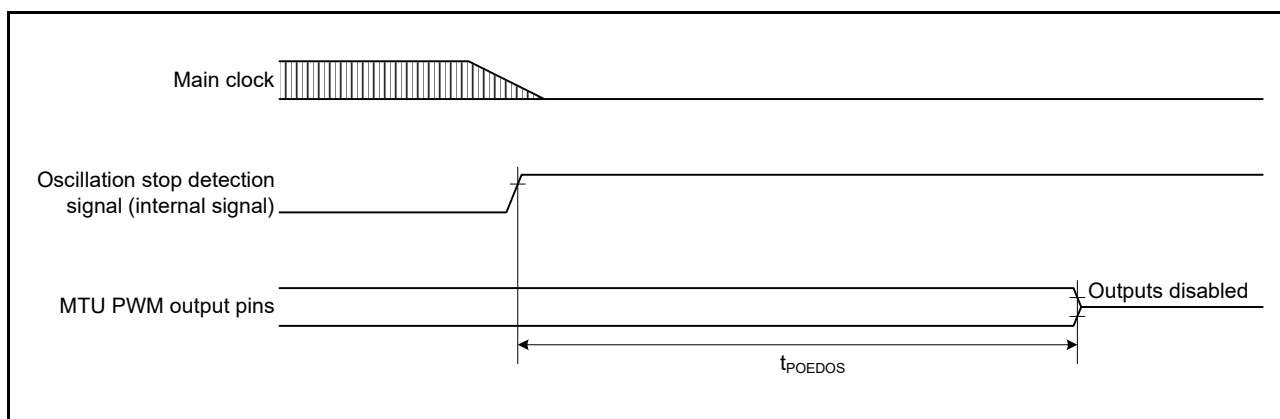
**Figure 2.40 POE# Pin Input Timing****Figure 2.41 Output Disable Time for POE in Response to Transition of the POEn# Signal Level**



**Figure 2.42 Output Disable Time for POE in Response to the Simultaneous Conduction of Output Pins**



**Figure 2.43 Output Disable Time for POE in Response to the Register Setting**



**Figure 2.44 Output Disable Time for POE in Response to the Oscillation Stop Detection**

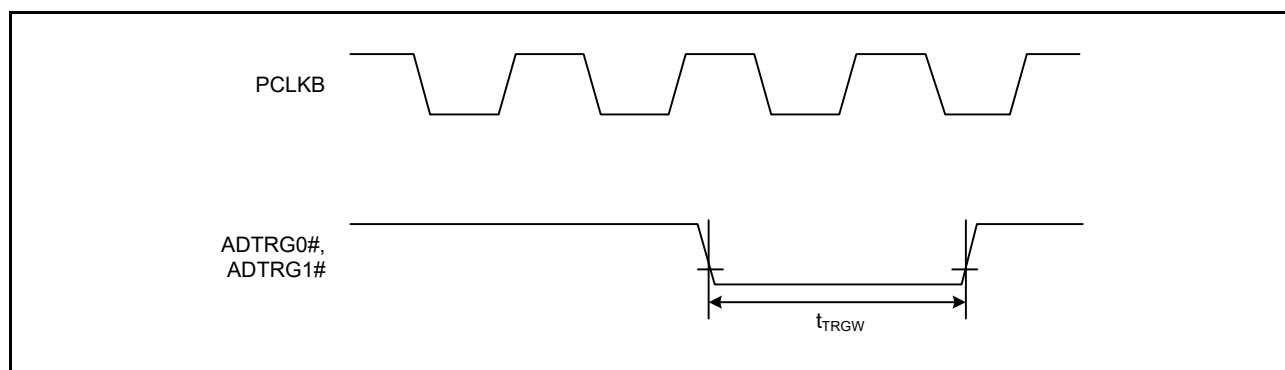
## 2.4.7.7 A/D Converter Trigger

**Table 2.33 A/D Converter Trigger Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the driving ability control register.

| Item          |                                         | Symbol     | Min. | Max. | Unit*1      | Test Conditions |
|---------------|-----------------------------------------|------------|------|------|-------------|-----------------|
| A/D converter | A/D converter trigger input pulse width | $t_{TRGW}$ | 1.5  | —    | $t_{PBcyc}$ | Figure 2.45     |

Note 1.  $t_{PBcyc}$ : PCLKB cycle

**Figure 2.45 A/D Converter Trigger Input Timing**

## 2.4.7.8 CAC

**Table 2.34 CAC Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the driving ability control register.

| Item*1, *2 |                          |                          | Symbol       | Min.*1, *2                  | Max. | Unit | Test Conditions |
|------------|--------------------------|--------------------------|--------------|-----------------------------|------|------|-----------------|
| CAC        | CACREF input pulse width | $t_{PBcyc} \leq t_{cac}$ | $t_{CACREF}$ | $4.5 t_{cac} + 3 t_{PBcyc}$ | —    | ns   |                 |
|            |                          | $t_{PBcyc} > t_{cac}$    |              | $5 t_{cac} + 6.5 t_{PBcyc}$ | —    |      |                 |

Note 1.  $t_{PBcyc}$ : PCLKB cycle

Note 2.  $t_{cac}$ : CAC count clock source cycle

## 2.4.7.9 SCI

**Table 2.35 SCIg, SCIH, and SCII Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the driving ability control register.

| Item                   |                          |                   | Symbol     | Min. | Max. | Unit*1      | Test Conditions |
|------------------------|--------------------------|-------------------|------------|------|------|-------------|-----------------|
| SCIg, SCIH             | Input clock cycle        | Asynchronous      | $t_{Scyc}$ | 4    | —    | $t_{PBcyc}$ | Figure 2.46     |
|                        |                          | Clock synchronous |            | 6    | —    |             |                 |
|                        | Input clock pulse width  |                   | $t_{SCKW}$ | 0.4  | 0.6  | $t_{Scyc}$  |                 |
|                        | Input clock rise time    |                   | $t_{SCKr}$ | —    | 5    | ns          |                 |
|                        | Input clock fall time    |                   | $t_{SCKf}$ | —    | 5    | ns          |                 |
|                        | Output clock cycle       | Asynchronous*2    | $t_{Scyc}$ | 8    | —    | $t_{PBcyc}$ |                 |
|                        |                          | Clock synchronous |            | 4    | —    |             |                 |
|                        | Output clock pulse width |                   | $t_{SCKW}$ | 0.4  | 0.6  | $t_{Scyc}$  |                 |
|                        | Output clock rise time   |                   | $t_{SCKr}$ | —    | 5    | ns          |                 |
|                        | Output clock fall time   |                   | $t_{SCKf}$ | —    | 5    | ns          |                 |
|                        | Transmit data delay time | Clock synchronous | $t_{TXD}$  | —    | 28   | ns          | Figure 2.47     |
|                        | Receive data setup time  | Clock synchronous | $t_{RXS}$  | 15   | —    | ns          |                 |
|                        | Receive data hold time   | Clock synchronous | $t_{RXH}$  | 5    | —    | ns          |                 |
| SCII                   | Input clock cycle        | Asynchronous      | $t_{Scyc}$ | 4    | —    | $t_{PAcyc}$ | Figure 2.46     |
|                        |                          | Clock synchronous |            | 12   | —    |             |                 |
|                        | Input clock pulse width  |                   | $t_{SCKW}$ | 0.4  | 0.6  | $t_{Scyc}$  |                 |
|                        | Input clock rise time    |                   | $t_{SCKr}$ | —    | 5    | ns          |                 |
|                        | Input clock fall time    |                   | $t_{SCKf}$ | —    | 5    | ns          |                 |
|                        | Output clock cycle       | Asynchronous*2    | $t_{Scyc}$ | 8    | —    | $t_{PAcyc}$ |                 |
|                        |                          | Clock synchronous |            | 8    | —    |             |                 |
|                        | Output clock pulse width |                   | $t_{SCKW}$ | 0.4  | 0.6  | $t_{Scyc}$  |                 |
|                        | Output clock rise time   |                   | $t_{SCKr}$ | —    | 5    | ns          |                 |
|                        | Output clock fall time   |                   | $t_{SCKf}$ | —    | 5    | ns          |                 |
|                        | Transmit data delay time | Master            | $t_{TXD}$  | —    | 15   | ns          | Figure 2.47     |
|                        |                          | Slave             |            | —    | 28   |             |                 |
|                        | Receive data setup time  | Clock synchronous | $t_{RXS}$  | 20   | —    | ns          |                 |
| Receive data hold time | Clock synchronous        | $t_{RXH}$         | 5          | —    |      |             |                 |

Note 1.  $t_{PBcyc}$ : PCLKB cycle;  $t_{PAcyc}$ : PCLKA cycle

Note 2. When the SEMR.ABCS and SEMR.BGDM bits are set to 1

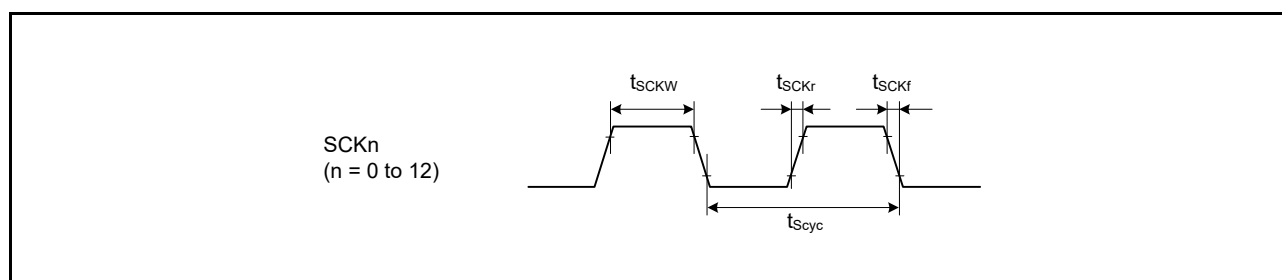


Figure 2.46 SCK Clock Input Timing

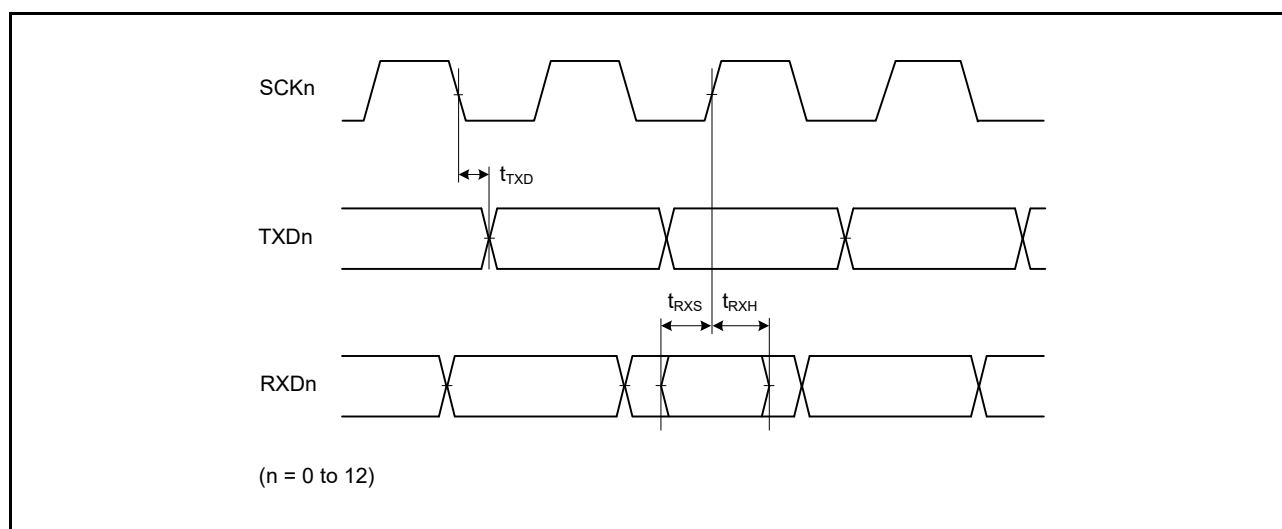


Figure 2.47 SCI Input/Output Timing: Clock Synchronous Mode

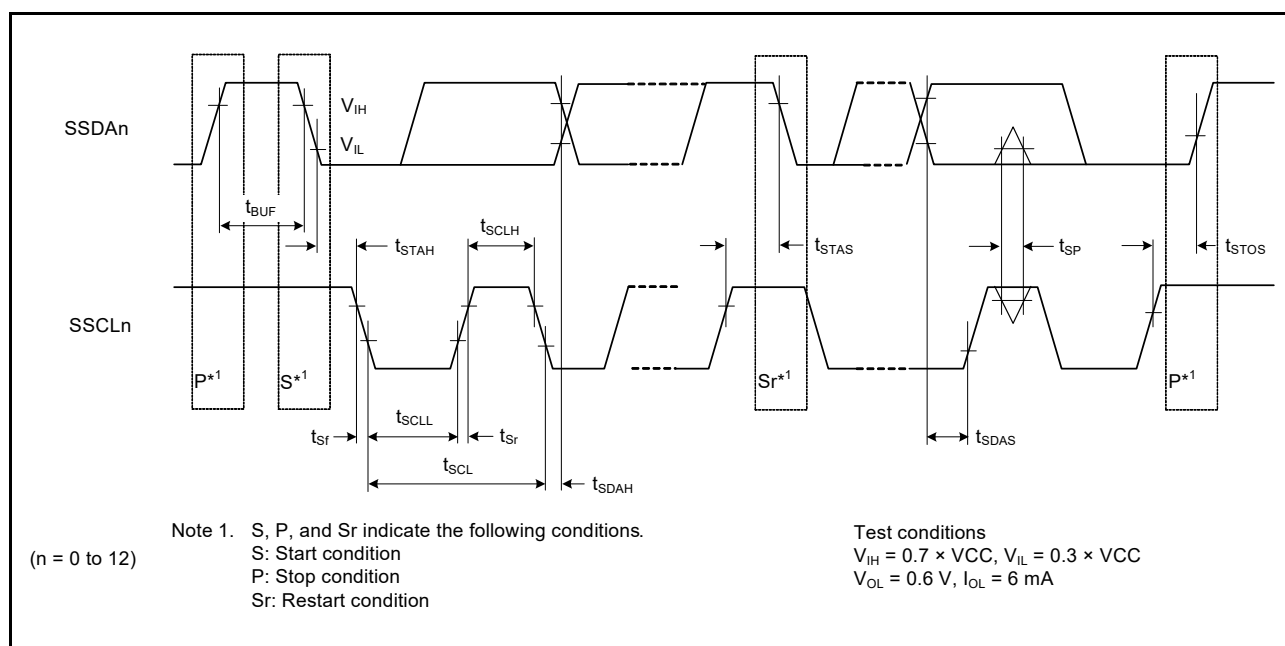
**Table 2.36 Simple IIC Timing**

Conditions:  $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AV_{CC0}$ ,  
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 High-drive output is selected by the driving ability control register.

| Item                          |                                           | Symbol     | Min. | Max.                | Unit | Test Conditions |
|-------------------------------|-------------------------------------------|------------|------|---------------------|------|-----------------|
| Simple IIC<br>(Standard-mode) | SSCL, SSDA input rise time                | $t_{Sr}$   | —    | 1000                | ns   | Figure 2.48     |
|                               | SSCL, SSDA input fall time                | $t_{Sf}$   | —    | 300                 | ns   |                 |
|                               | SSCL, SSDA input spike pulse removal time | $t_{SP}$   | 0    | $4 \times t_{Pcyc}$ | ns   |                 |
|                               | Data input setup time                     | $t_{SDAS}$ | 250  | —                   | ns   |                 |
|                               | Data input hold time                      | $t_{SDAH}$ | 0    | —                   | ns   |                 |
|                               | SSCL, SSDA capacitive load                | $C_b^{*1}$ | —    | 400                 | pF   |                 |
| Simple IIC<br>(Fast-mode)     | SSCL, SSDA input rise time                | $t_{Sr}$   | —    | 300                 | ns   |                 |
|                               | SSCL, SSDA input fall time                | $t_{Sf}$   | —    | 300                 | ns   |                 |
|                               | SSCL, SSDA input spike pulse removal time | $t_{SP}$   | 0    | $4 \times t_{Pcyc}$ | ns   |                 |
|                               | Data input setup time                     | $t_{SDAS}$ | 100  | —                   | ns   |                 |
|                               | Data input hold time                      | $t_{SDAH}$ | 0    | —                   | ns   |                 |
|                               | SSCL, SSDA capacitive load                | $C_b^{*1}$ | —    | 400                 | pF   |                 |

Note:  $t_{Pcyc}$  refers to the period of PCLKA in SCI10 and SCI11, and of PCLKB in SCI0 to SCI9, and SCI12.

Note 1.  $C_b$  is the total capacitance of the bus lines.

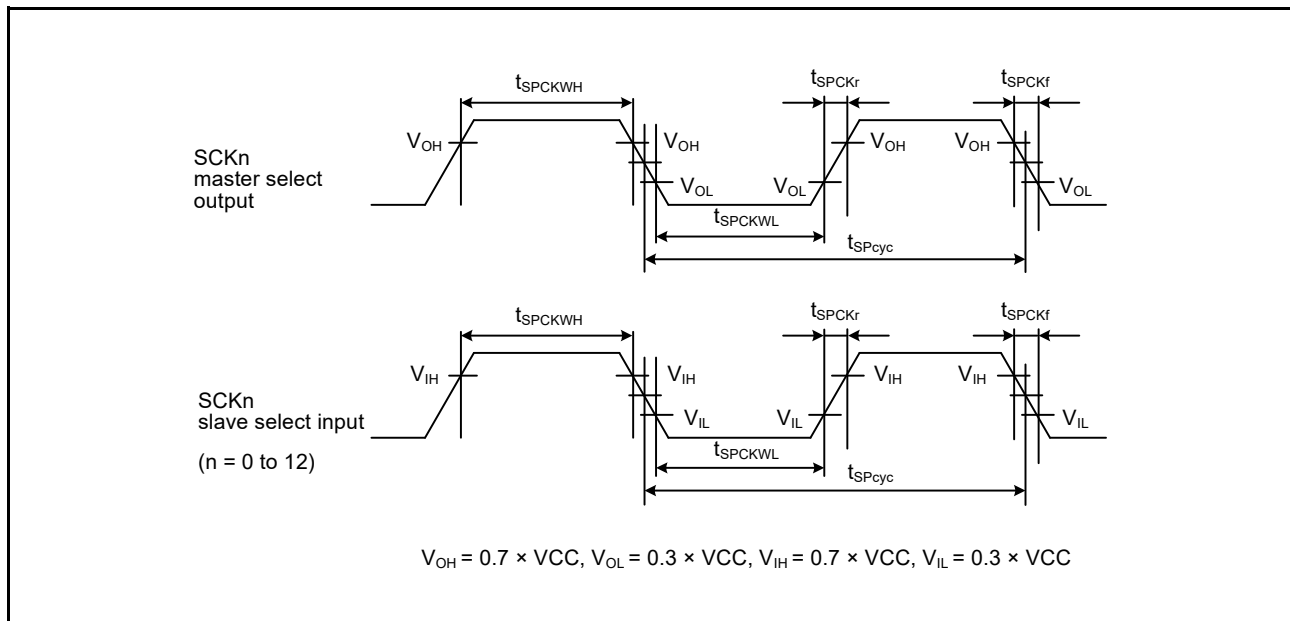
**Figure 2.48 Simple IIC Bus Interface Input/Output Timing**

**Table 2.37 Simple SPI Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
High-drive output is selected by the driving ability control register.

| Item       |                                 | Symbol                    | Min. | Max.  | Unit*1      | Test Conditions            |
|------------|---------------------------------|---------------------------|------|-------|-------------|----------------------------|
| Simple SPI | SCK clock cycle output (master) | $t_{SPcyc}$               | 4    | 65536 | $t_{Pcyc}$  | Figure 2.49                |
|            | SCK clock cycle input (slave)   |                           | 6    | 65536 |             |                            |
|            | SCK clock high pulse width      | $t_{SPCKWH}$              | 0.4  | 0.6   | $t_{SPcyc}$ |                            |
|            | SCK clock low pulse width       | $t_{SPCKWL}$              | 0.4  | 0.6   | $t_{SPcyc}$ |                            |
|            | SCK clock rise/fall time        | $t_{SPCKr}$ , $t_{SPCKf}$ | —    | 20    | ns          |                            |
|            | Data input setup time           | $t_{SU}$                  | 33.3 | —     | ns          | Figure 2.50 to Figure 2.53 |
|            | Data input hold time            | $t_H$                     | 33.3 | —     | ns          |                            |
|            | SS input setup time             | $t_{LEAD}$                | 1    | —     | $t_{SPcyc}$ |                            |
|            | SS input hold time              | $t_{LAG}$                 | 1    | —     | $t_{SPcyc}$ |                            |
|            | Data output delay time          | $t_{OD}$                  | —    | 33.3  | ns          |                            |
|            | Data output hold time           | $t_{OH}$                  | −10  | —     | ns          |                            |
|            | Data rise/fall time             | $t_{Dr}$ , $t_{Df}$       | —    | 16.6  | ns          |                            |
|            | SS input rise/fall time         | $t_{SSLr}$ , $t_{SSLf}$   | —    | 16.6  | ns          |                            |
|            | Slave access time               | $t_{SA}$                  | —    | 5     | $t_{Pcyc}$  | Figure 2.52, Figure 2.53   |
|            | Slave output release time       | $t_{REL}$                 | —    | 5     | $t_{Pcyc}$  |                            |

Note 1.  $t_{Pcyc}$  refers to the period of PCLKA in SCI10 and SCI11, and of PCLKB in SCI0 to SCI9, and SCI12.

**Figure 2.49 Simple SPI Clock Timing**

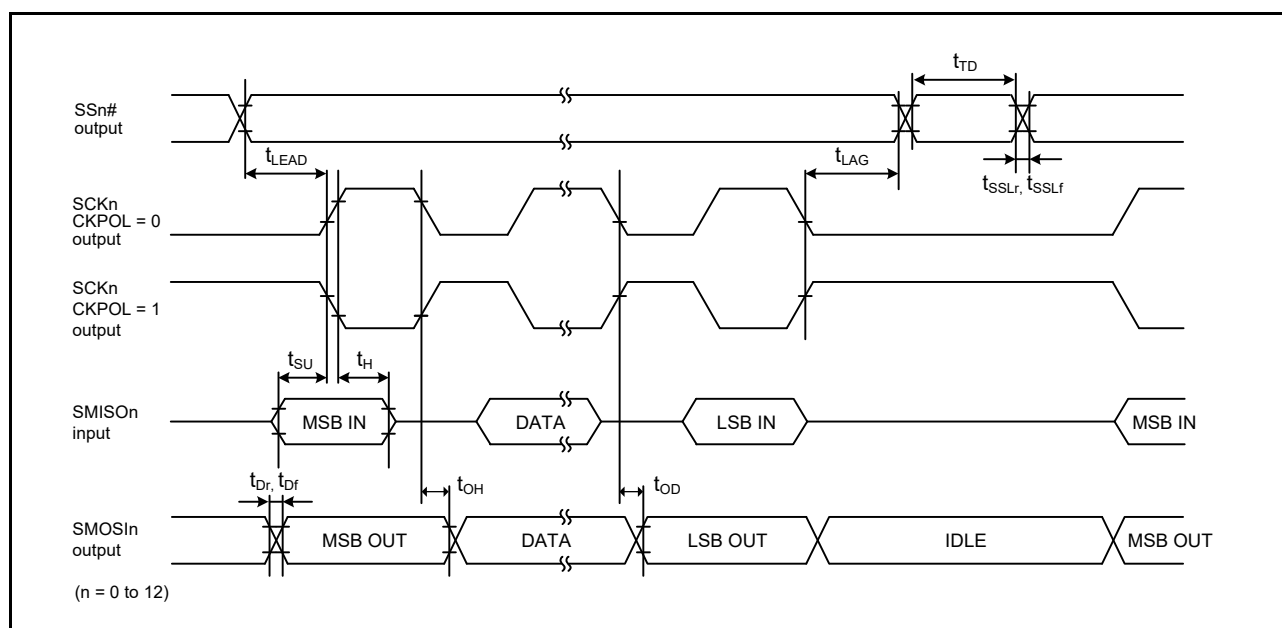


Figure 2.50 Simple SPI Timing (Master, CKPH = 1)

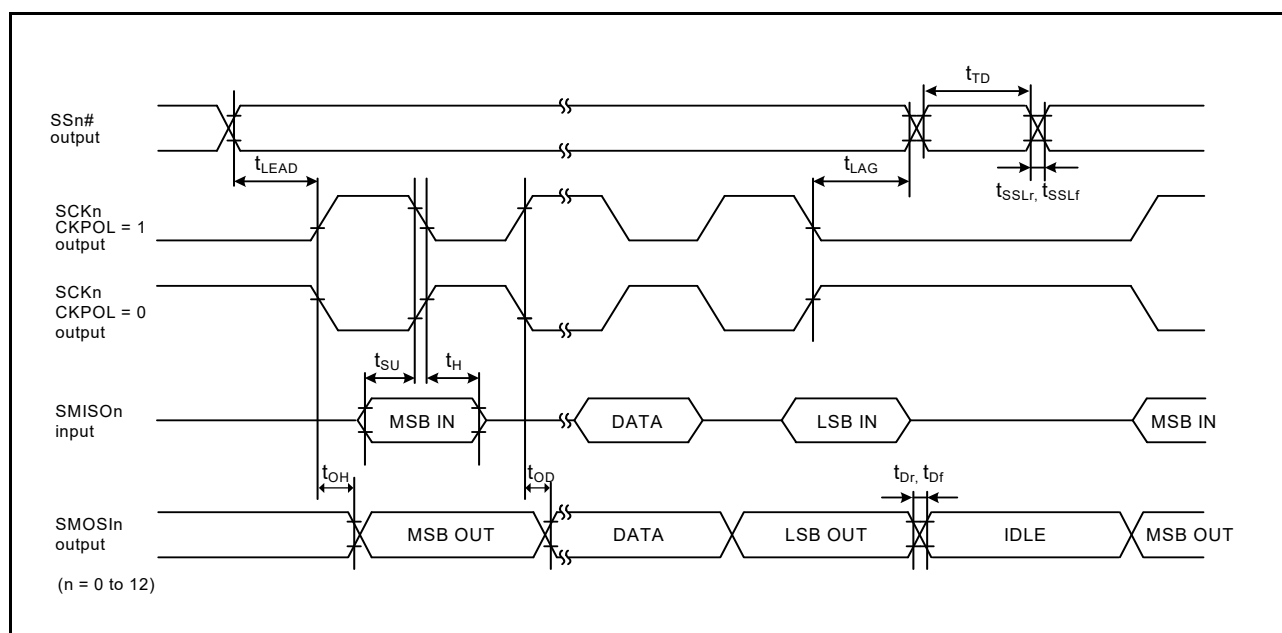
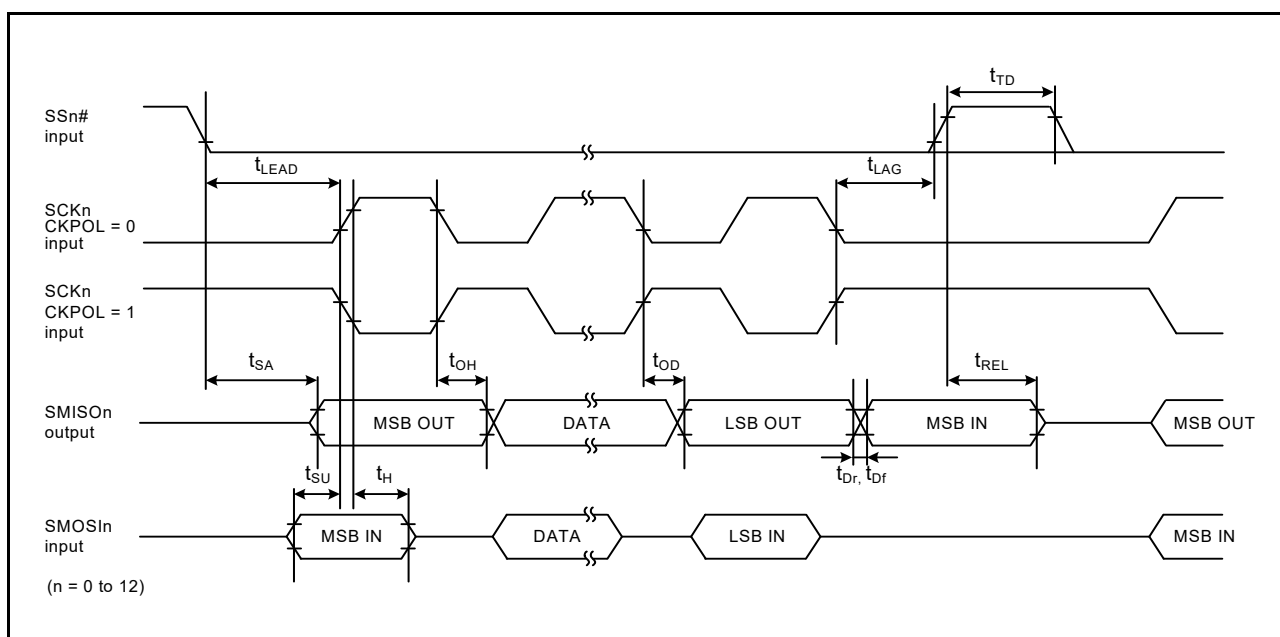
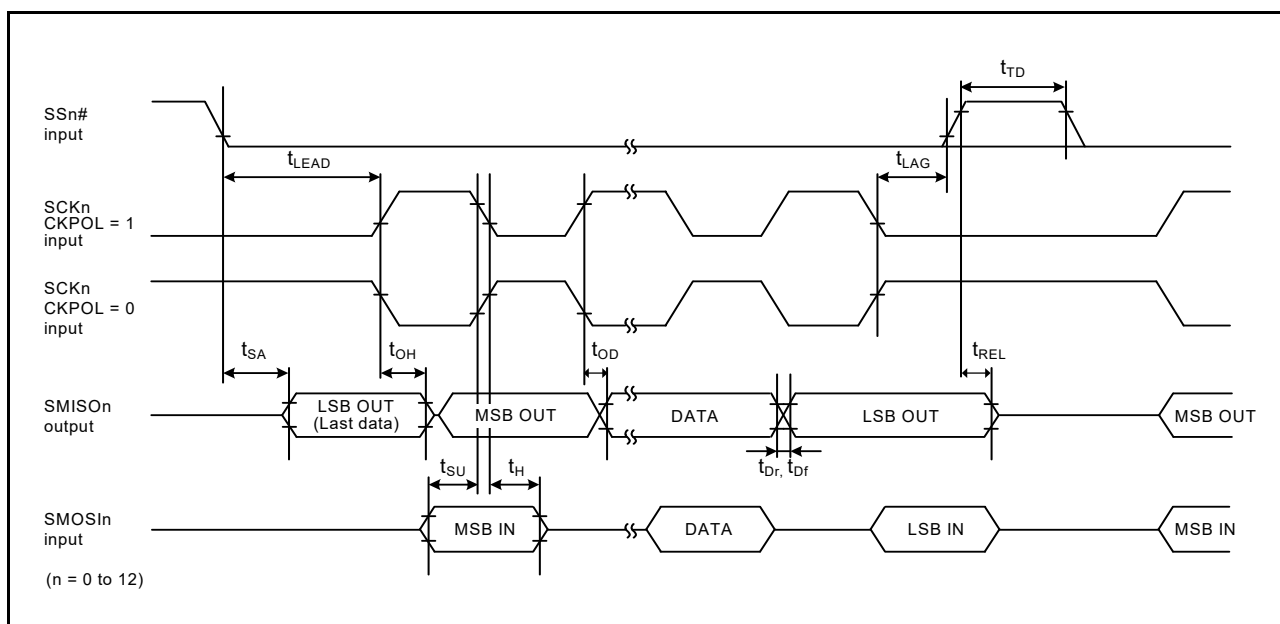


Figure 2.51 Simple SPI Timing (Master, CKPH = 0)



**Figure 2.52 Simple SPI Timing (Slave, CKPH = 1)**



**Figure 2.53 Simple SPI Timing (Slave, CKPH = 0)**

## 2.4.7.10 RSPI

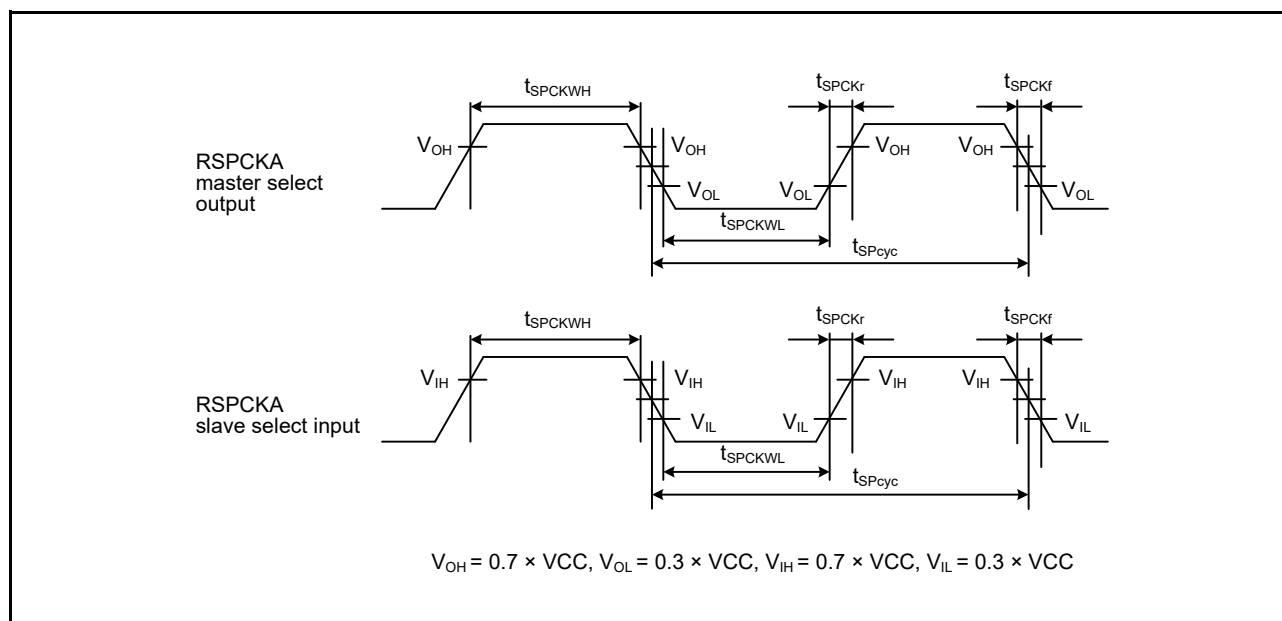
**Table 2.38 RSPI Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the driving ability control register.

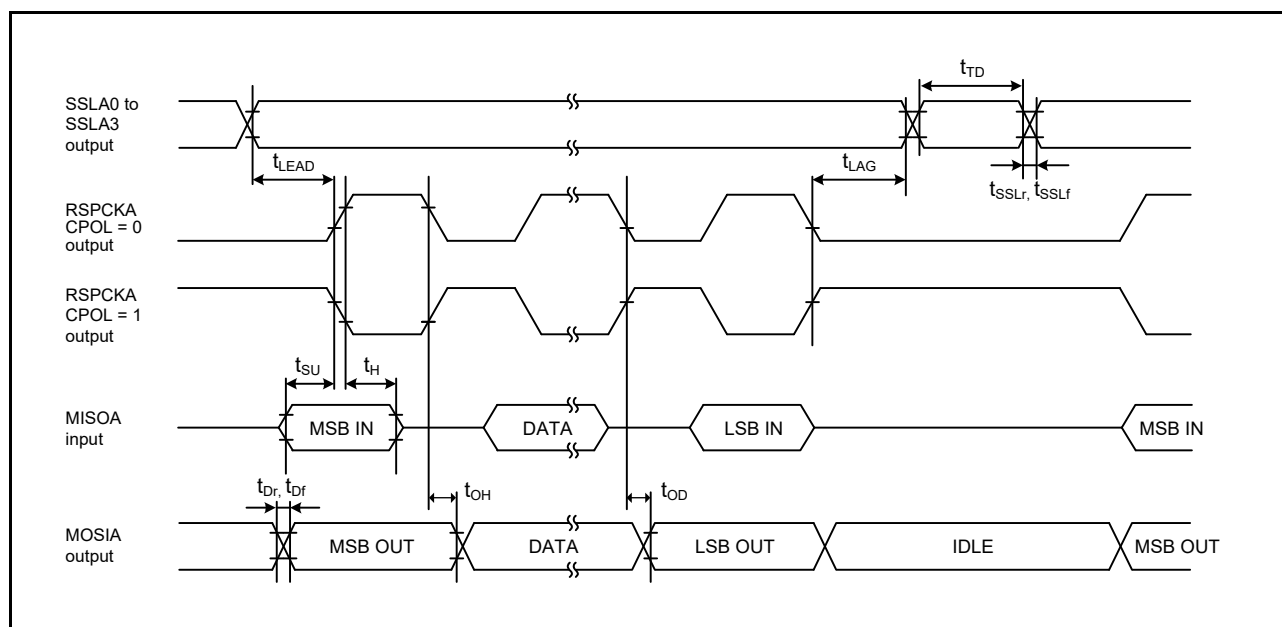
| Item |                                    |        | Symbol           | Min.*1                                        | Max.*1                                    | Unit*1      | Test Conditions*2          |
|------|------------------------------------|--------|------------------|-----------------------------------------------|-------------------------------------------|-------------|----------------------------|
| RSPI | RSPCK clock cycle                  | Master | $t_{SPCyc}$      | 2                                             | 4096                                      | $t_{PAcyc}$ | Figure 2.54                |
|      |                                    | Slave  |                  | 4                                             | —                                         | —           |                            |
|      | RSPCK clock high pulse width       | Master | $t_{SPCKWH}$     | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | —                                         | ns          |                            |
|      |                                    | Slave  |                  | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2$     | —                                         | —           |                            |
|      | RSPCK clock low pulse width        | Master | $t_{SPCKWL}$     | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | —                                         | ns          |                            |
|      |                                    | Slave  |                  | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2$     | —                                         | —           |                            |
|      | RSPCK clock rise/fall time         | Output | $t_{SPCKr}$      | —                                             | 5                                         | ns          | Figure 2.55 to Figure 2.60 |
|      |                                    | Input  | $t_{SPCKf}$      | —                                             | 1                                         | $\mu s$     |                            |
|      | Data input setup time              | Master | $t_{SU}$         | 6                                             | —                                         | ns          |                            |
|      |                                    | Slave  |                  | 8.3                                           | —                                         | —           |                            |
|      | Data input hold time               | Master | $t_{HF}$         | 0                                             | —                                         | ns          |                            |
|      |                                    |        | $t_H$            | $t_{PAcyc}$                                   | —                                         | —           |                            |
|      |                                    | Slave  |                  | 8.3                                           | —                                         | —           |                            |
|      | SSL setup time                     | Master | $t_{LEAD}$       | 1                                             | 8                                         | $t_{SPCyc}$ |                            |
|      |                                    | Slave  |                  | 6                                             | —                                         | $t_{PAcyc}$ |                            |
|      | SSL hold time                      | Master | $t_{LAG}$        | 1                                             | 8                                         | $t_{SPCyc}$ |                            |
|      |                                    | Slave  |                  | 6                                             | —                                         | $t_{PAcyc}$ |                            |
|      | Data output delay time             | Master | $t_{OD}$         | —                                             | 6.3                                       | ns          |                            |
|      |                                    | Slave  |                  | —                                             | 28                                        | —           |                            |
|      | Data output hold time              | Master | $t_{OH}$         | 0                                             | —                                         | ns          |                            |
|      |                                    | Slave  |                  | 0                                             | —                                         | —           |                            |
|      | Successive transmission delay time | Master | $t_{TD}$         | $t_{SPCyc} + 2 \times t_{PAcyc}$              | $8 \times t_{SPCyc} + 2 \times t_{PAcyc}$ | ns          | Figure 2.59, Figure 2.60   |
|      |                                    | Slave  |                  | $6 \times t_{PAcyc}$                          | —                                         | —           |                            |
|      | MOSI and MISO rise/fall time       | Output | $t_{Dr}, t_{Df}$ | —                                             | 5                                         | ns          |                            |
|      |                                    | Input  |                  | —                                             | 1                                         | $\mu s$     |                            |
|      | SSL rise/fall time                 | Output | $t_{SSLr}$       | —                                             | 5                                         | ns          |                            |
|      |                                    | Input  | $t_{SSLf}$       | —                                             | 1                                         | $\mu s$     |                            |
|      | Slave access time                  |        | $t_{SA}$         | —                                             | $2 \times t_{PAcyc} + 28$                 | ns          | Figure 2.59, Figure 2.60   |
|      | Slave output release time          |        | $t_{REL}$        | —                                             | $2 \times t_{PAcyc} + 28$                 | ns          |                            |

Note 1.  $t_{PACyc}$ : PCLKA cycle

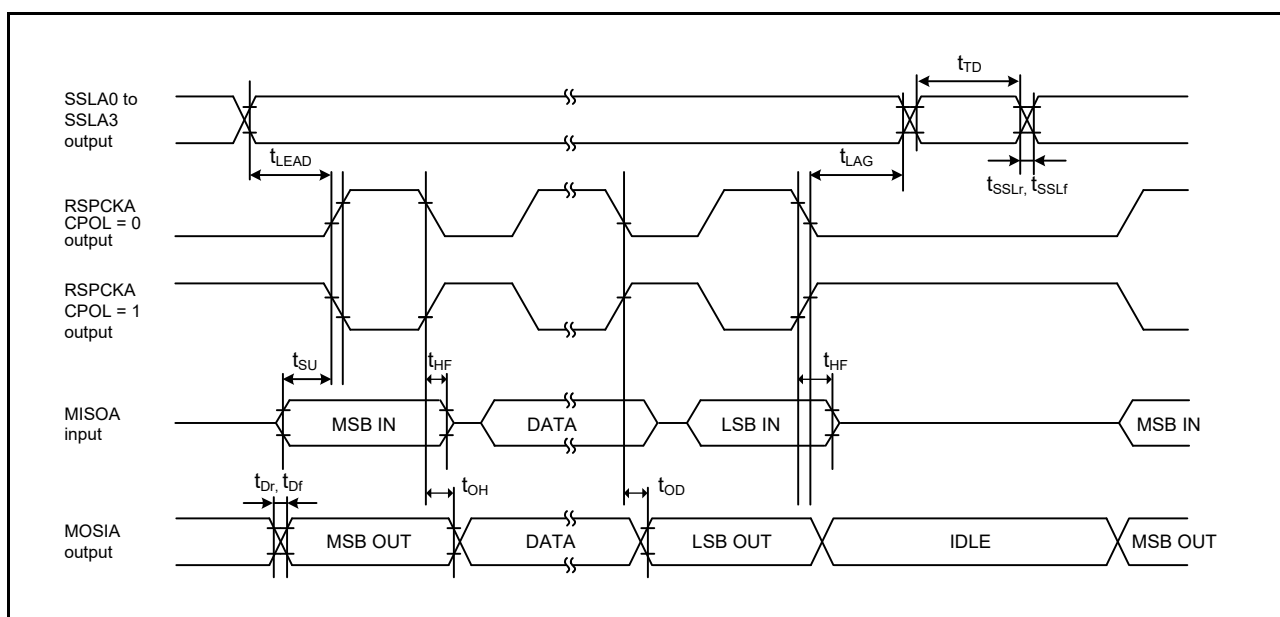
Note 2. When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All RSPI AC timings are measured in combination with the pins in the same group.



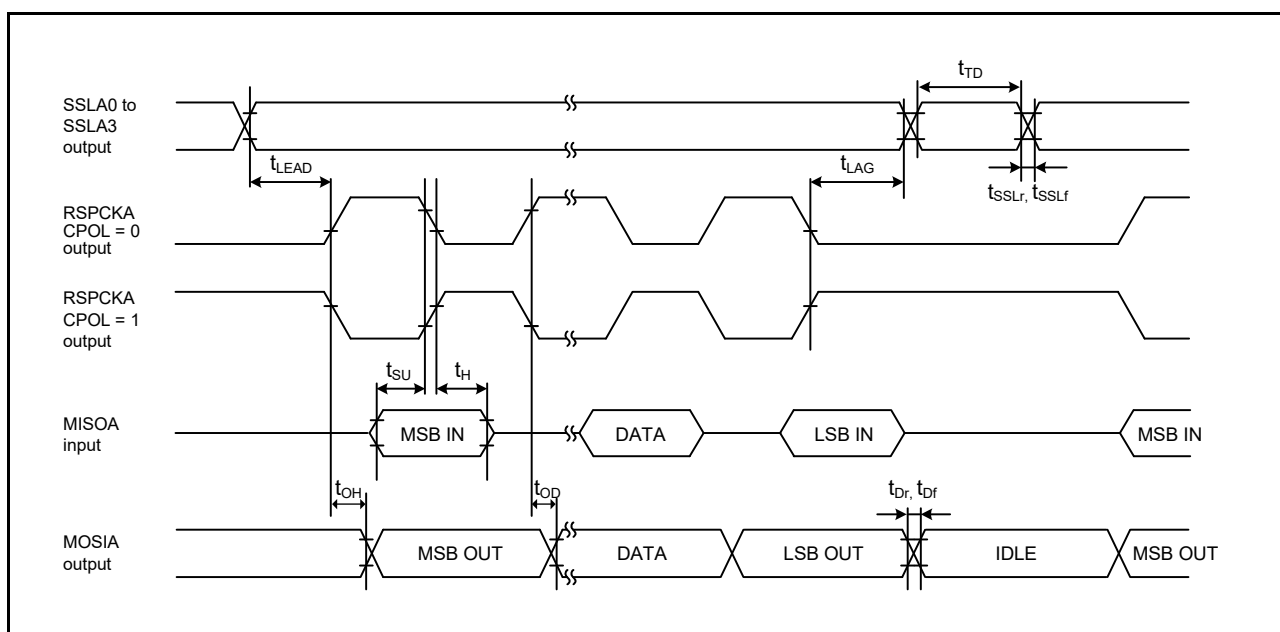
**Figure 2.54 RSPI Clock Timing**



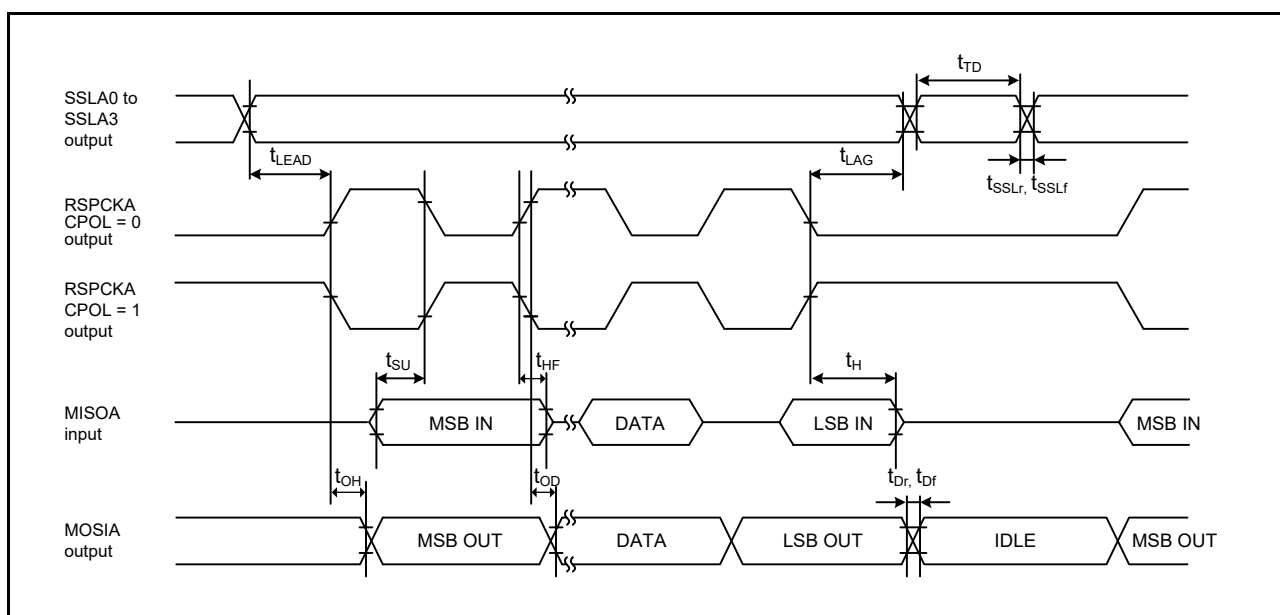
**Figure 2.55 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)**



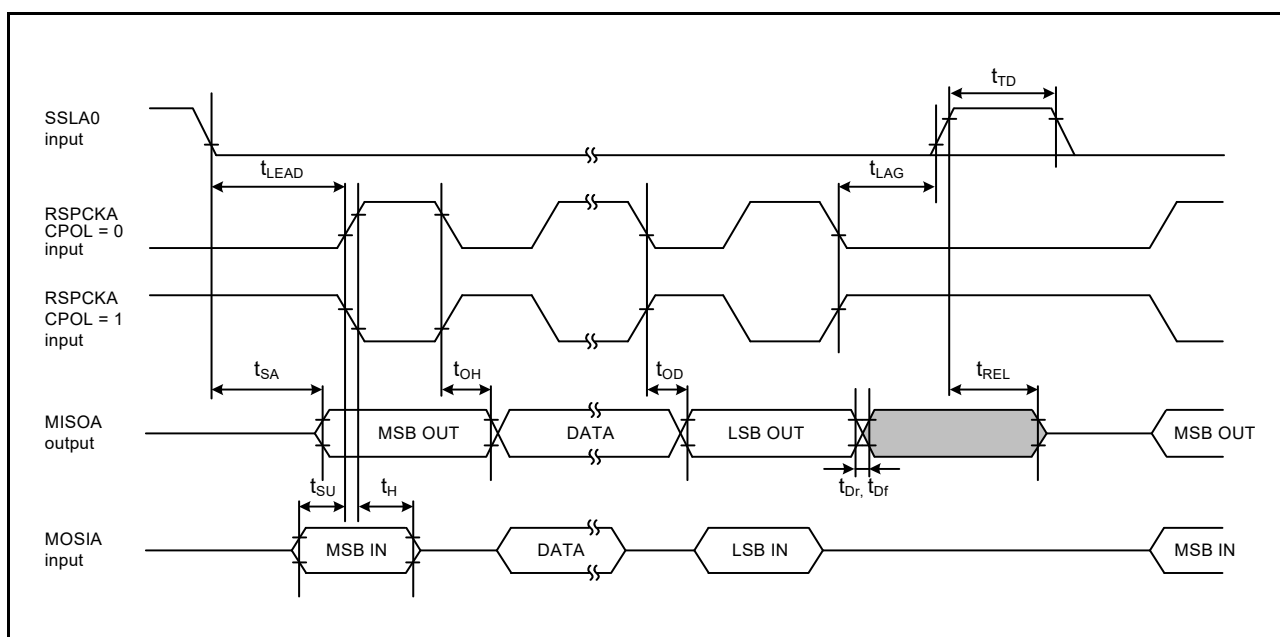
**Figure 2.56 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to 1/2)**



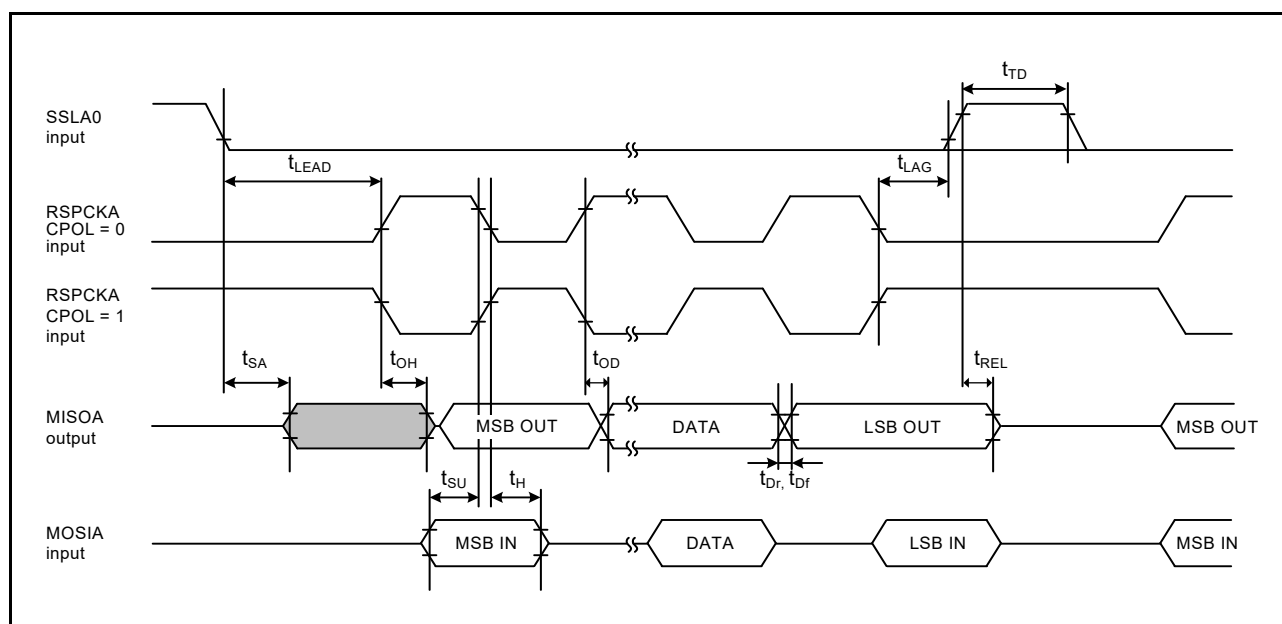
**Figure 2.57 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)**



**Figure 2.58 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to 1/2)**



**Figure 2.59 RSPI Timing (Slave, CPHA = 0)**



**Figure 2.60 RSPI Timing (Slave, CPHA = 1)**

## 2.4.7.11 QSPI

**Table 2.39 QSPI Timing**

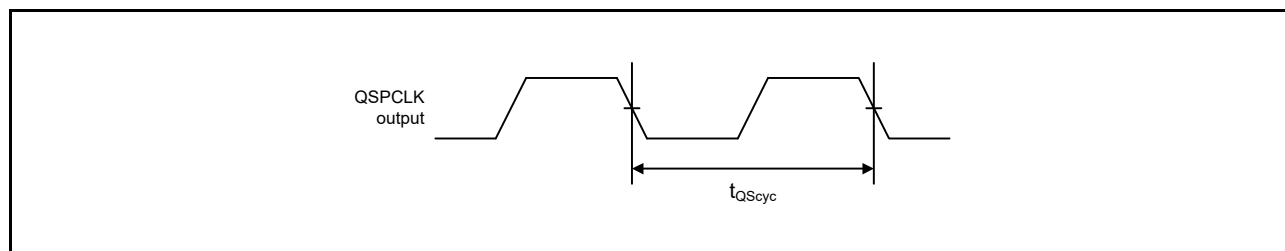
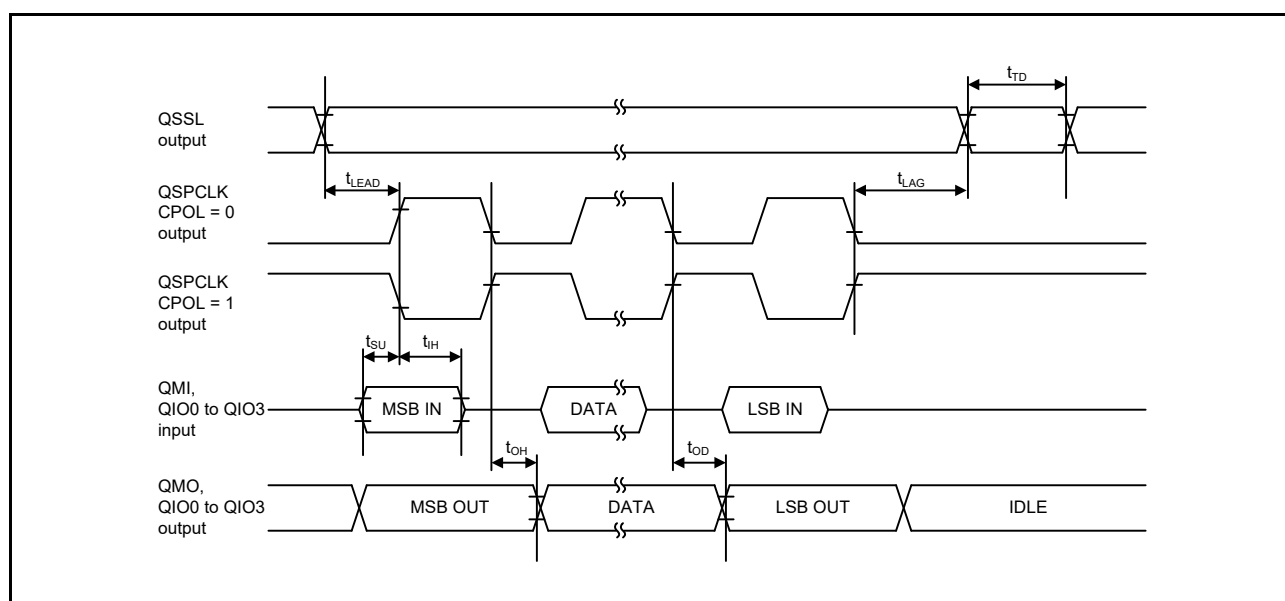
Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the driving ability control register.\*3

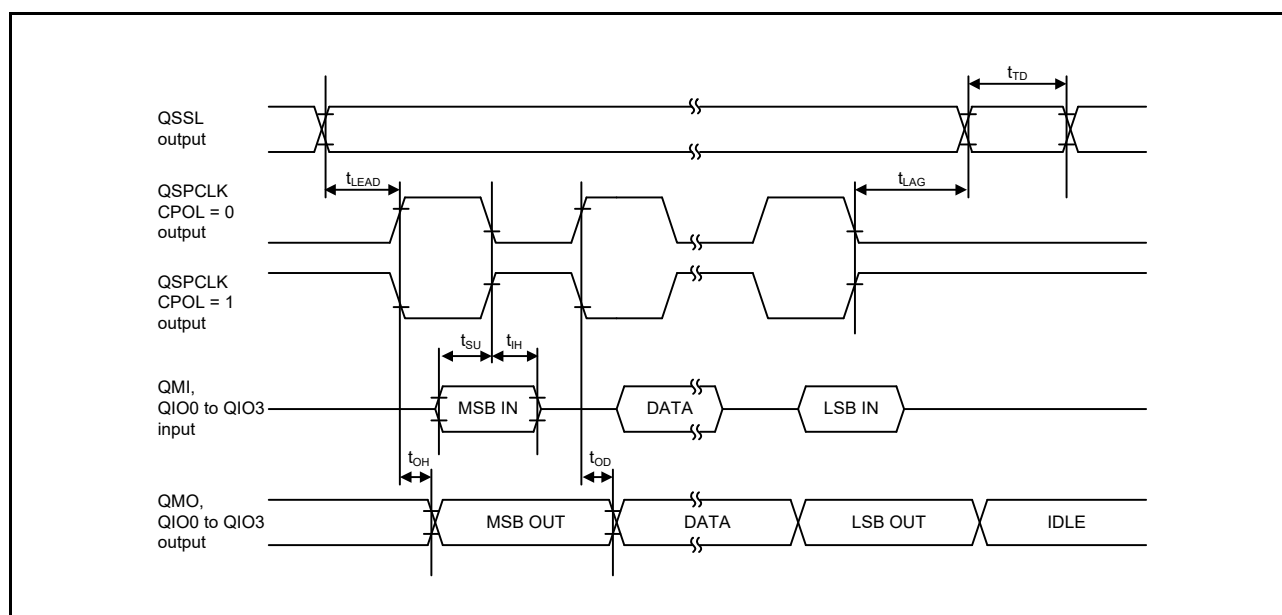
| Item | Symbol                             | Min.        | Max. | Unit*1 | Test Conditions*2           |
|------|------------------------------------|-------------|------|--------|-----------------------------|
| QSPI | QSPCLK clock cycle                 | $t_{QScyc}$ | 2    | 4080   | $t_{PBcyc}$ Figure 2.61     |
|      | Data input setup time              | $t_{su}$    | 6.5  | —      | ns Figure 2.62, Figure 2.63 |
|      | Data input hold time               | $t_{IH}$    | 5    | —      | ns                          |
|      | SS setup time                      | $t_{LEAD}$  | 1.5  | 8.5    | $t_{QScyc}$                 |
|      | SS hold time                       | $t_{LAG}$   | 1    | 8      | $t_{QScyc}$                 |
|      | Data output delay time             | $t_{OD}$    | —    | 10.0   | ns                          |
|      | Data output hold time              | $t_{OH}$    | —5   | —      | ns                          |
|      | Successive transmission delay time | $t_{TD}$    | 1    | 8      | $t_{QScyc}$                 |

Note 1.  $t_{PBcyc}$ : PCLKB cycle

Note 2. When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All QSPI AC timings are measured in combination with the pins in the same group.

Note 3. In the G-version products, the AC characteristics are measured by setting the drive capacity control register 2 corresponding the QSPCLK pin as a high-speed interface high-drive output.

**Figure 2.61 QSPI Clock Timing****Figure 2.62 Transmit/Receive Timing (CPHA = 0)**



**Figure 2.63** Transmit/Receive Timing (CPHA = 1)

## 2.4.7.12 RIIC

**Table 2.40 RIIC Timing (1/2)**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 High-drive output is selected by the driving ability control register.

| Item                                                |                                         | Symbol     | Min.*1                                             | Max.                     | Unit | Test Conditions |
|-----------------------------------------------------|-----------------------------------------|------------|----------------------------------------------------|--------------------------|------|-----------------|
| RIIC<br>(Standard-mode,<br>SMBus)<br>ICFER.FMPE = 0 | SCL input cycle time                    | $t_{SCL}$  | $6(12) \times t_{IICcyc} + 1300$                   | —                        | ns   | Figure 2.64     |
|                                                     | SCL input high pulse width              | $t_{SCLH}$ | $3(6) \times t_{IICcyc} + 300$                     | —                        | ns   |                 |
|                                                     | SCL input low pulse width               | $t_{SCLL}$ | $3(6) \times t_{IICcyc} + 300$                     | —                        | ns   |                 |
|                                                     | SCL, SDA input rise time                | $t_{Sr}$   | —                                                  | 1000                     | ns   |                 |
|                                                     | SCL, SDA input fall time                | $t_{Sf}$   | —                                                  | 300                      | ns   |                 |
|                                                     | SCL, SDA input spike pulse removal time | $t_{SP}$   | 0                                                  | $1(4) \times t_{IICcyc}$ | ns   |                 |
|                                                     | SDA input bus free time                 | $t_{BUF}$  | $3(6) \times t_{IICcyc} + 300$                     | —                        | ns   |                 |
|                                                     | Start condition input hold time         | $t_{STAH}$ | $t_{IICcyc} + 300$                                 | —                        | ns   |                 |
|                                                     | Restart condition input setup time      | $t_{STAS}$ | 1000                                               | —                        | ns   |                 |
|                                                     | Stop condition input setup time         | $t_{STOS}$ | 1000                                               | —                        | ns   |                 |
|                                                     | Data input setup time                   | $t_{SDAS}$ | $t_{IICcyc} + 50$                                  | —                        | ns   |                 |
|                                                     | Data input hold time                    | $t_{SDAH}$ | 0                                                  | —                        | ns   |                 |
|                                                     | SCL, SDA capacitive load                | $C_b^{*2}$ | —                                                  | 400                      | pF   |                 |
| RIIC<br>(Fast-mode)<br>ICFER.FMPE = 0               | SCL input cycle time                    | $t_{SCL}$  | $6(12) \times t_{IICcyc} + 600$                    | —                        | ns   |                 |
|                                                     | SCL input high pulse width              | $t_{SCLH}$ | $3(6) \times t_{IICcyc} + 300$                     | —                        | ns   |                 |
|                                                     | SCL input low pulse width               | $t_{SCLL}$ | $3(6) \times t_{IICcyc} + 300$                     | —                        | ns   |                 |
|                                                     | SCL, SDA input rise time                | $t_{Sr}$   | $20 \times (\text{External pull-up voltage}/5.5V)$ | 300                      | ns   |                 |
|                                                     | SCL, SDA input fall time                | $t_{Sf}$   | $20 \times (\text{External pull-up voltage}/5.5V)$ | 300                      | ns   |                 |
|                                                     | SCL, SDA input spike pulse removal time | $t_{SP}$   | 0                                                  | $1(4) \times t_{IICcyc}$ | ns   |                 |
|                                                     | SDA input bus free time                 | $t_{BUF}$  | $3(6) \times t_{IICcyc} + 300$                     | —                        | ns   |                 |
|                                                     | Start condition input hold time         | $t_{STAH}$ | $t_{IICcyc} + 300$                                 | —                        | ns   |                 |
|                                                     | Restart condition input setup time      | $t_{STAS}$ | 300                                                | —                        | ns   |                 |
|                                                     | Stop condition input setup time         | $t_{STOS}$ | 300                                                | —                        | ns   |                 |
|                                                     | Data input setup time                   | $t_{SDAS}$ | $t_{IICcyc} + 50$                                  | —                        | ns   |                 |
|                                                     | Data input hold time                    | $t_{SDAH}$ | 0                                                  | —                        | ns   |                 |
|                                                     | SCL, SDA capacitive load                | $C_b^{*2}$ | —                                                  | 400                      | pF   |                 |

**Table 2.40 RIIC Timing (2/2)**

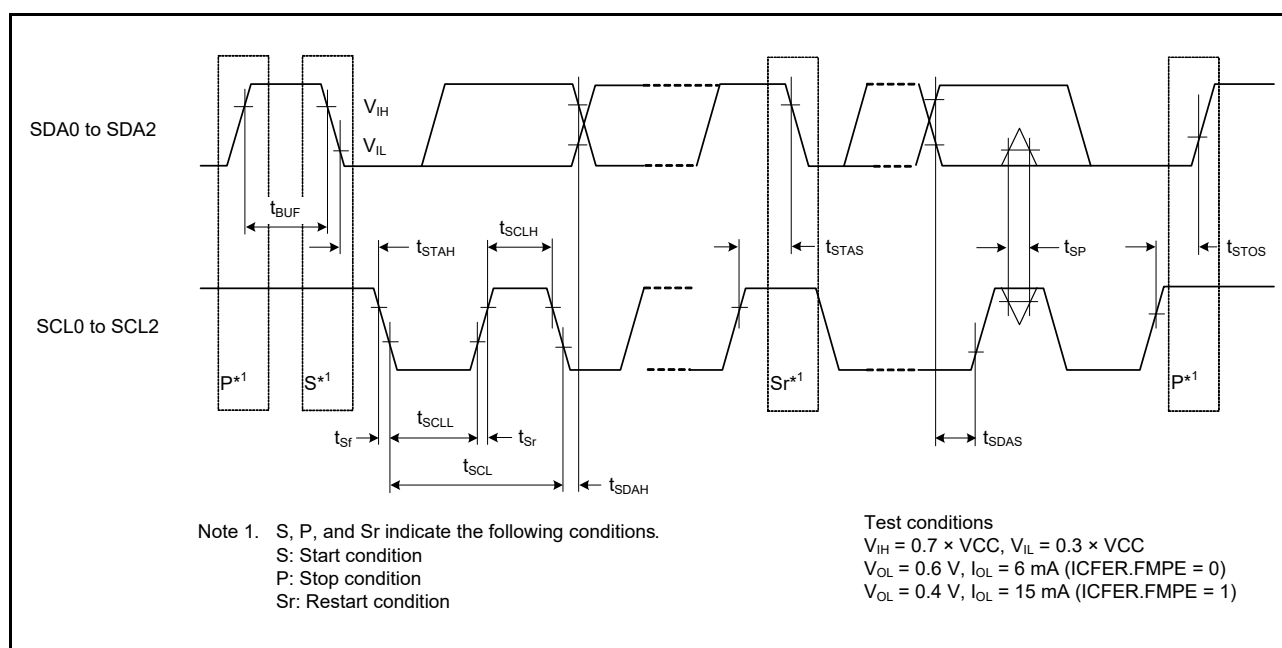
Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 High-drive output is selected by the driving ability control register.

|                                        | Item                                    | Symbol     | Min.*1                          | Max.                     | Unit | Test Conditions |
|----------------------------------------|-----------------------------------------|------------|---------------------------------|--------------------------|------|-----------------|
| RIIC<br>(Fast-mode+)<br>ICFER.FMPE = 1 | SCL input cycle time                    | $t_{SCL}$  | $6(12) \times t_{IICcyc} + 240$ | —                        | ns   | Figure 2.64     |
|                                        | SCL input high pulse width              | $t_{SCLH}$ | $3(6) \times t_{IICcyc} + 120$  | —                        | ns   |                 |
|                                        | SCL input low pulse width               | $t_{SCLL}$ | $3(6) \times t_{IICcyc} + 120$  | —                        | ns   |                 |
|                                        | SCL, SDA input rise time                | $t_{Sr}$   | —                               | 120                      | ns   |                 |
|                                        | SCL, SDA input fall time                | $t_{Sf}$   | —                               | 120                      | ns   |                 |
|                                        | SCL, SDA input spike pulse removal time | $t_{SP}$   | 0                               | $1(4) \times t_{IICcyc}$ | ns   |                 |
|                                        | SDA input bus free time                 | $t_{BUF}$  | $3(6) \times t_{IICcyc} + 120$  | —                        | ns   |                 |
|                                        | Start condition input hold time         | $t_{STAH}$ | $t_{IICcyc} + 120$              | —                        | ns   |                 |
|                                        | Restart condition input setup time      | $t_{STAS}$ | 120                             | —                        | ns   |                 |
|                                        | Stop condition input setup time         | $t_{STOS}$ | 120                             | —                        | ns   |                 |
|                                        | Data input setup time                   | $t_{SDAS}$ | $t_{IICcyc} + 20$               | —                        | ns   |                 |
|                                        | Data input hold time                    | $t_{SDAH}$ | 0                               | —                        | ns   |                 |
|                                        | SCL, SDA capacitive load                | $C_b^{*2}$ | —                               | 550                      | pF   |                 |

Note:  $t_{IICcyc}$ : RIIC internal reference clock (IIC $\phi$ ) cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2.  $C_b$  is the total capacitance of the bus lines.

**Figure 2.64 RIIC Bus Interface Input/Output Timing**

## 2.4.7.13 MMC

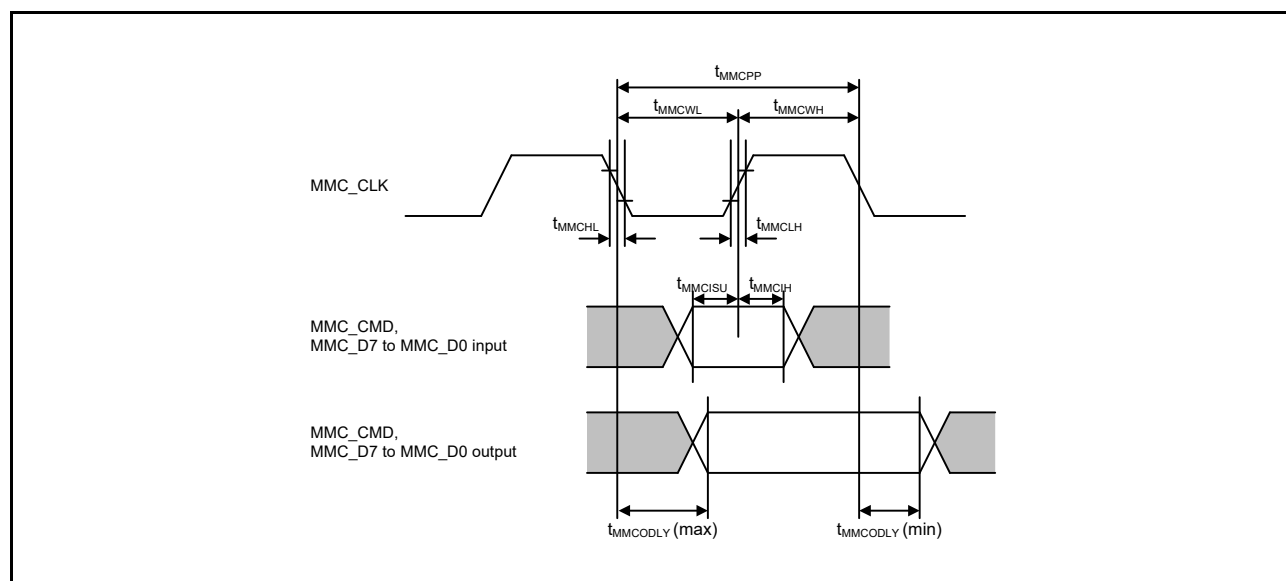
**Table 2.41 MMC Host Interface Timing**

Conditions:  $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AV_{CC0}$ ,  
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the driving ability control register.

|       | Item                                                             | Symbol       | Min.*1               | Max. | Unit | Test Conditions*2 |
|-------|------------------------------------------------------------------|--------------|----------------------|------|------|-------------------|
| MMCIF | MMC_CLK clock cycle                                              | $t_{MMCPP}$  | $2 \times t_{PBcyc}$ | —    | ns   | Figure 2.65       |
|       | MMC_CLK clock high level width                                   | $t_{MMCWH}$  | 6.5                  | —    | ns   |                   |
|       | MMC_CLK clock low level width                                    | $t_{MMCWL}$  | 6.5                  | —    | ns   |                   |
|       | MMC_CLK clock rising time                                        | $t_{MMCCLH}$ | —                    | 3    | ns   |                   |
|       | MMC_CLK clock falling time                                       | $t_{MMCCHL}$ | —                    | 3    | ns   |                   |
|       | MMC_CMD, MMC_D7 to MMC_D0 output data delay (data transfer mode) | $t_{MMCODY}$ | –6.6                 | 6.6  | ns   |                   |
|       | MMC_CMD, MMC_D7 to MMC_D0 input data setup                       | $t_{MMCISU}$ | 8                    | —    | ns   |                   |
|       | MMC_CMD, MMC_D7 to MMC_D0 input data hold                        | $t_{MMCIH}$  | 2.5                  | —    | ns   |                   |

Note 1.  $t_{PBcyc}$ : PCLKB cycle

Note 2. When a letter "A", "B", etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All MMC AC timings are measured in combination with the pins in the same group.

**Figure 2.65 MMC Interface**

## 2.4.7.14 ETHERC

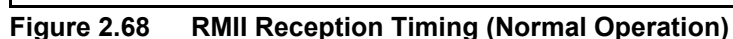
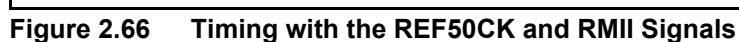
**Table 2.42 ETHERC Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
High-drive output is selected by the driving ability control register.

|               | Item                                       | Symbol        | Min. | Max.         | Unit | Test Conditions            |
|---------------|--------------------------------------------|---------------|------|--------------|------|----------------------------|
| ETHERC (RMII) | REF50CK cycle time                         | $T_{ck}$      | 20   | —            | ns   | Figure 2.66 to Figure 2.69 |
|               | REF50CK frequency Typ. 50 MHz              | —             | —    | 50 + 100 ppm | MHz  |                            |
|               | REF50CK duty                               | —             | 35   | 65           | %    |                            |
|               | REF50CK rise/fall time                     | $T_{ckr/ckf}$ | 0.5  | 3.5          | ns   |                            |
|               | RMII0_*** <sup>*1</sup> output delay time  | $T_{co}$      | 2.5  | 15.0         | ns   |                            |
|               | RMII0_*** <sup>*2</sup> setup time         | $T_{su}$      | 3    | —            | ns   |                            |
|               | RMII0_*** <sup>*2</sup> hold time          | $T_{hd}$      | 1    | —            | ns   |                            |
|               | RMII0_*** <sup>*1, *2</sup> rise/fall time | $T_r/T_f$     | 0.5  | 5            | ns   |                            |
|               | ET0_WOL output delay time                  | $t_{WOLd}$    | 1    | 23.5         | ns   | Figure 2.70                |
| ETHERC (MII)  | ET0_TX_CLK cycle time                      | $t_{Tcyc}$    | 40   | —            | ns   | —                          |
|               | ET0_TX_EN output delay time                | $t_{TEND}$    | 1    | 20           | ns   | Figure 2.71                |
|               | ET0_ETXD0 to ET0_ETXD3 output delay time   | $t_{MTDd}$    | 1    | 20           | ns   |                            |
|               | ET0_CRS setup time                         | $t_{CRSs}$    | 10   | —            | ns   |                            |
|               | ET0_CRS hold time                          | $t_{CRSh}$    | 10   | —            | ns   |                            |
|               | ET0_COL setup time                         | $t_{COLs}$    | 10   | —            | ns   | Figure 2.72                |
|               | ET0_COL hold time                          | $t_{COLh}$    | 10   | —            | ns   |                            |
|               | ET0_RX_CLK cycle time                      | $t_{TRcyc}$   | 40   | —            | ns   | —                          |
|               | ET0_RX_DV setup time                       | $t_{RDVs}$    | 10   | —            | ns   | Figure 2.73                |
|               | ET0_RX_DV hold time                        | $t_{RDVh}$    | 10   | —            | ns   |                            |
|               | ET0_ERXD0 to ET0_ERXD3 setup time          | $t_{MRDs}$    | 10   | —            | ns   |                            |
|               | ET0_ERXD0 to ET0_ERXD3 hold time           | $t_{MRDh}$    | 10   | —            | ns   |                            |
|               | ET0_RX_ER setup time                       | $t_{RERs}$    | 10   | —            | ns   | Figure 2.74                |
|               | ET0_RX_ER hold time                        | $t_{RERh}$    | 10   | —            | ns   |                            |
|               | ET0_WOL output delay time                  | $t_{WOLd}$    | 1    | 23.5         | ns   | Figure 2.75                |

Note 1. RMII0\_TXD\_EN, RMII0\_TXD1, RMII0\_TXD0

Note 2. RMII0\_CRS\_DV, RMII0\_RXD1, RMII0\_RXD0, RMII0\_RX\_ER



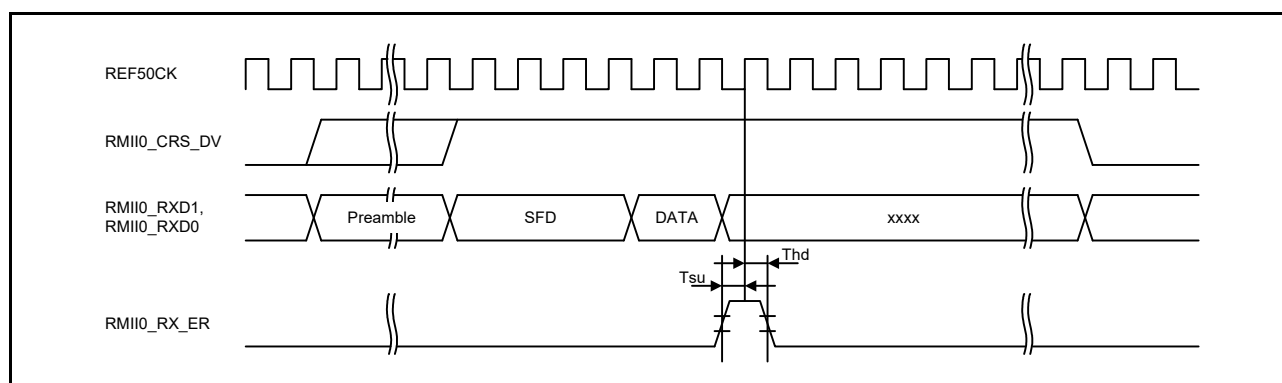


Figure 2.69 RMII Reception Timing (Error Occurrence)

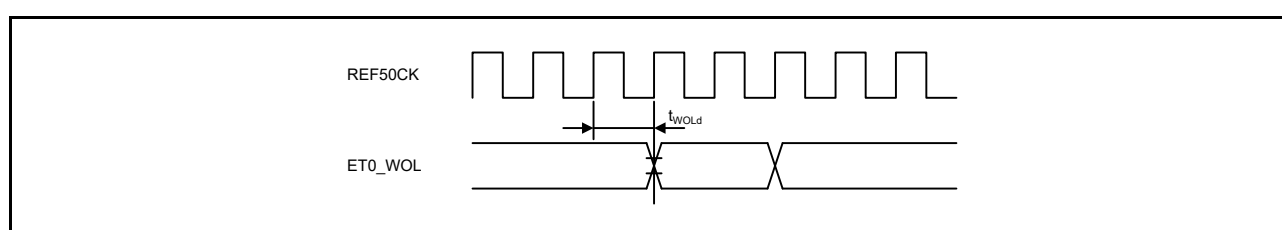


Figure 2.70 WOL Output Timing (RMII)

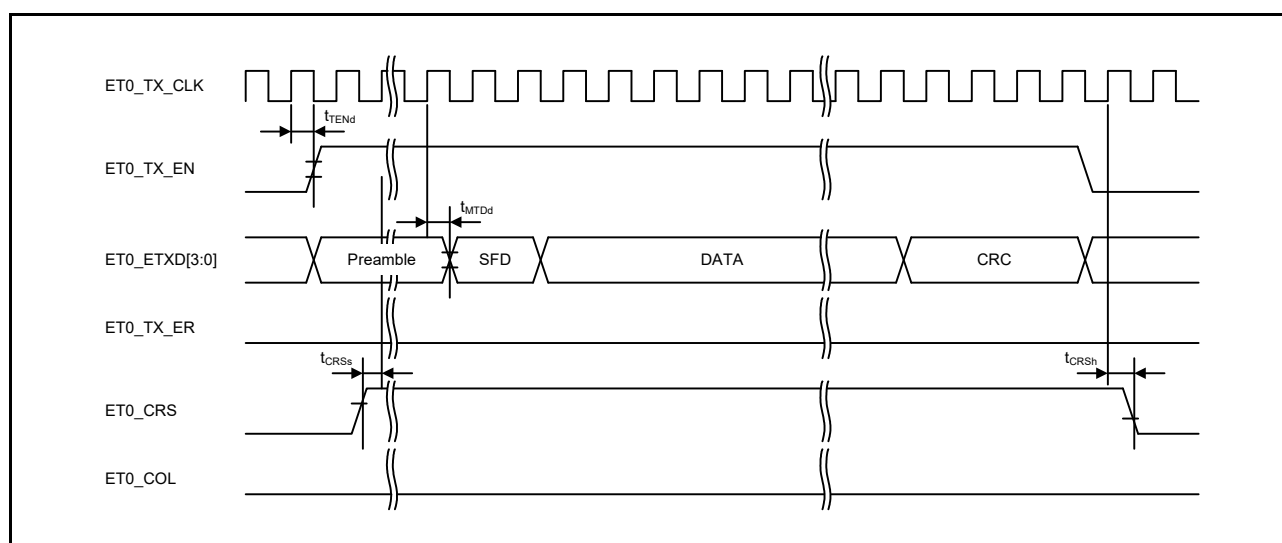


Figure 2.71 MII Transmission Timing (Normal Operation)

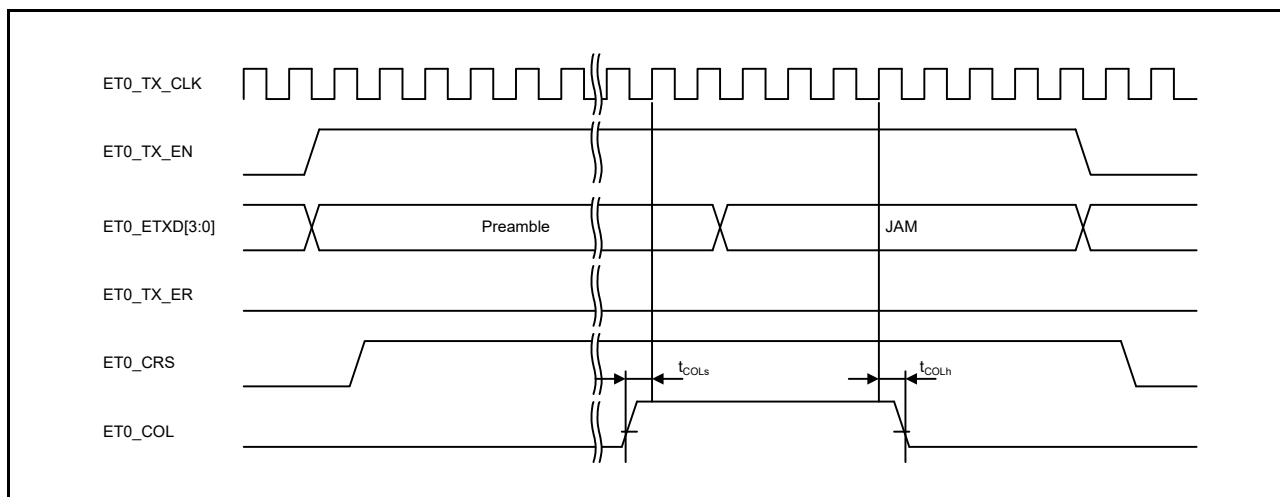


Figure 2.72 MII Transmission Timing (Conflict Occurrence)

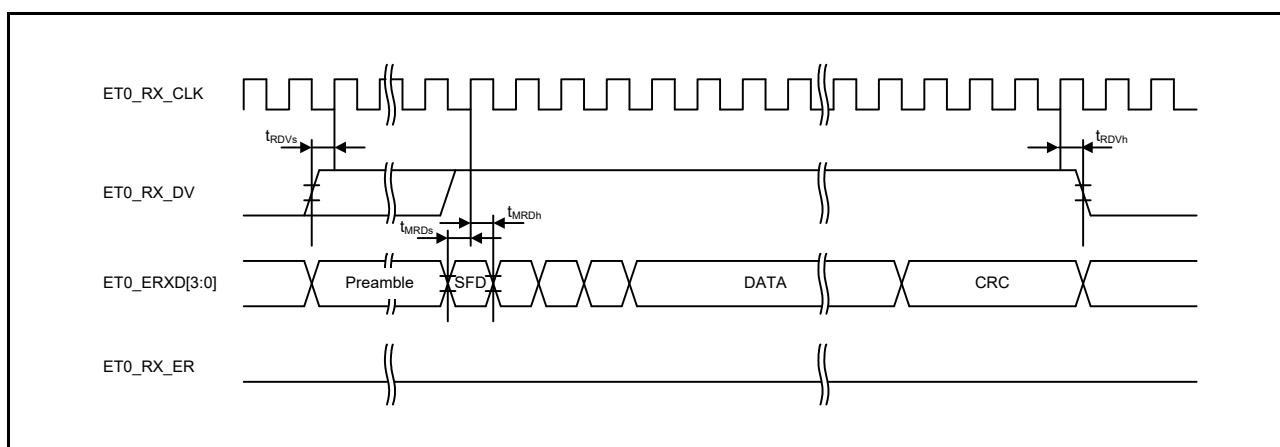


Figure 2.73 MII Reception Timing (Normal Operation)

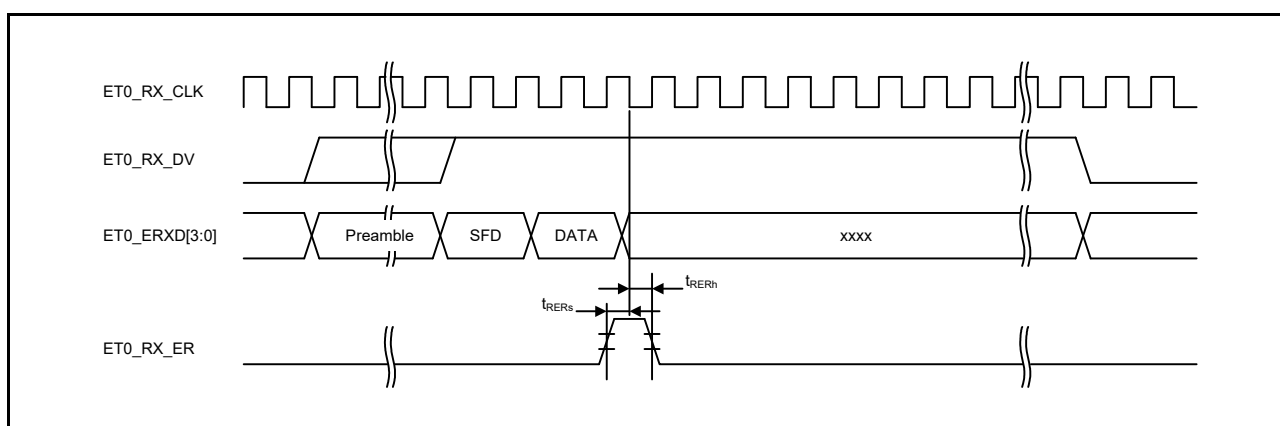
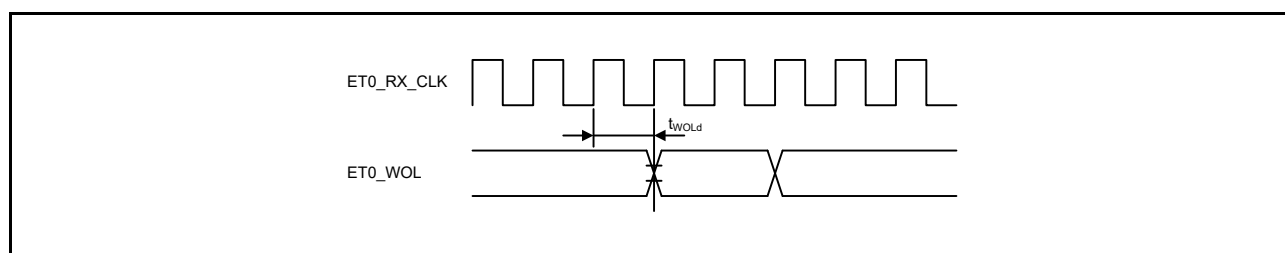


Figure 2.74 MII Reception Timing (Error Occurrence)

**Figure 2.75 WOL Output Timing (MII)**

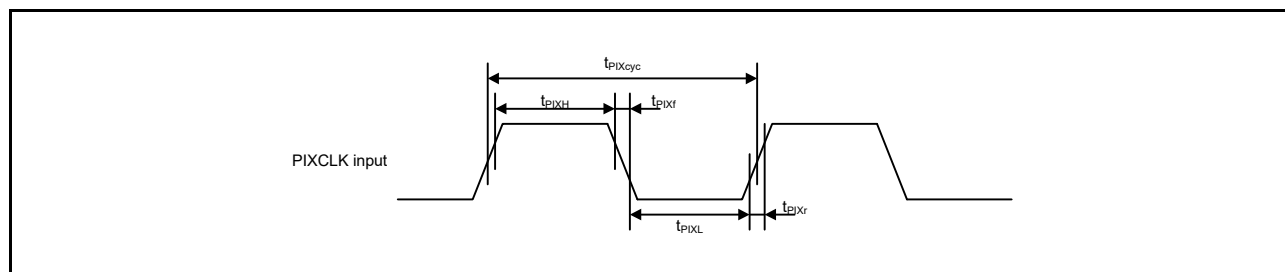
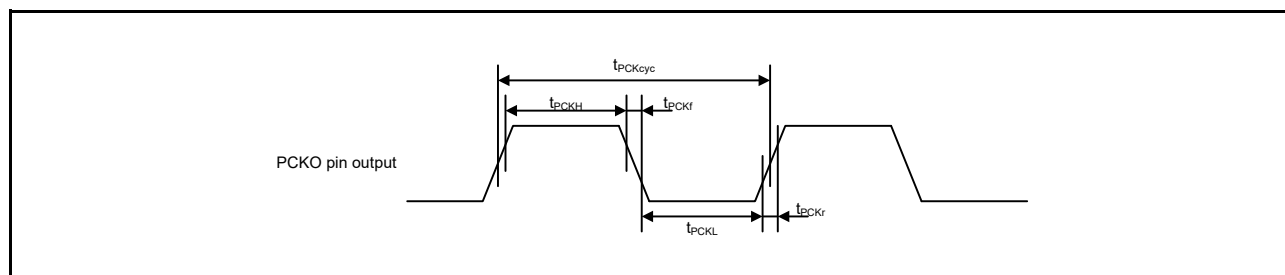
## 2.4.7.15 PDC

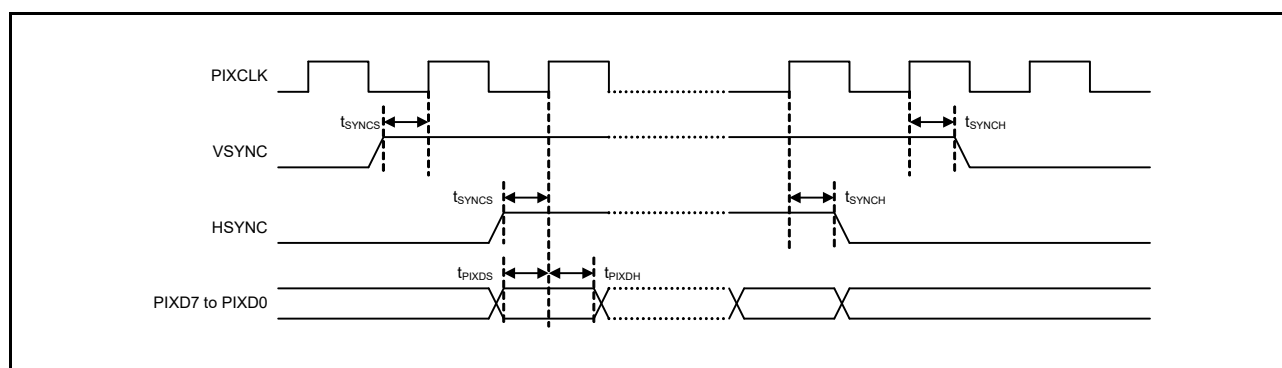
**Table 2.43 PDC Timing**

Conditions:  $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AV_{CC0}$ ,  
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the driving ability control register.

| Item |                               | Symbol  | Min.*1                          | Max. | Unit | Test Conditions |
|------|-------------------------------|---------|---------------------------------|------|------|-----------------|
| PDC  | PIXCLK input cycle time       | tPIXcyc | 37                              | —    | ns   | Figure 2.76     |
|      | PIXCLK input high pulse width | tPIXH   | 10                              | —    | ns   |                 |
|      | PIXCLK input low pulse width  | tPIXL   | 10                              | —    | ns   |                 |
|      | PIXCLK rising time            | tPIXr   | —                               | 5    | ns   |                 |
|      | PIXCLK falling time           | tPIXf   | —                               | 5    | ns   |                 |
|      | PCKO output cycle time        | tPCKcyc | 2 × tPBcyc                      | —    | ns   | Figure 2.77     |
|      | PCKO output high pulse width  | tPCKH   | (tPCKcyc – tPCKr – tPCKf)/2 – 3 | —    | ns   |                 |
|      | PCKO output low pulse width   | tPCKL   | (tPCKcyc – tPCKr – tPCKf)/2 – 3 | —    | ns   |                 |
|      | PCKO rising time              | tPCKr   | —                               | 5    | ns   |                 |
|      | PCKO falling time             | tPCKf   | —                               | 5    | ns   |                 |
|      | VSYNC/HSYNC input setup time  | tSYNCS  | 10                              | —    | ns   | Figure 2.78     |
|      | VSYNC/HSYNC input hold time   | tSYNCH  | 5                               | —    | ns   |                 |
|      | PIXD input setup time         | tPIXDS  | 10                              | —    | ns   |                 |
|      | PIXD input hold time          | tPIXDH  | 5                               | —    | ns   |                 |

Note 1.  $t_{PBcyc}$ : PCLKB cycle

**Figure 2.76 PDC Input Clock Timing****Figure 2.77 PDC Output Clock Timing**

**Figure 2.78 PDC AC Timing**

## 2.4.7.16 GLCDC

**Table 2.44 GLCDC Timing**

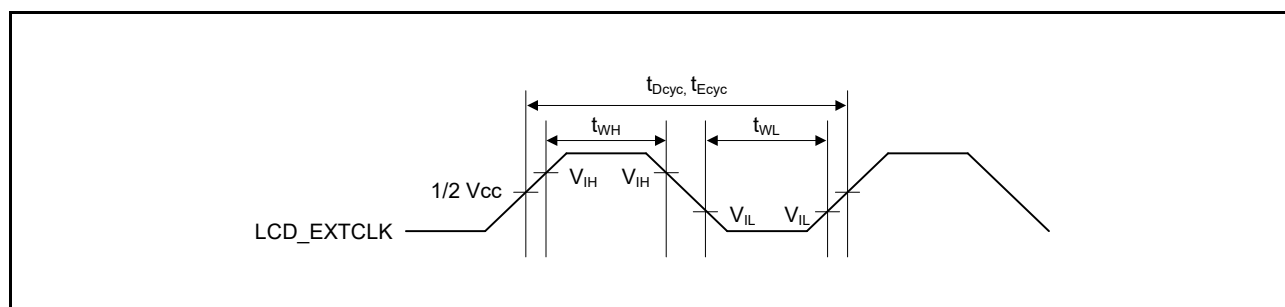
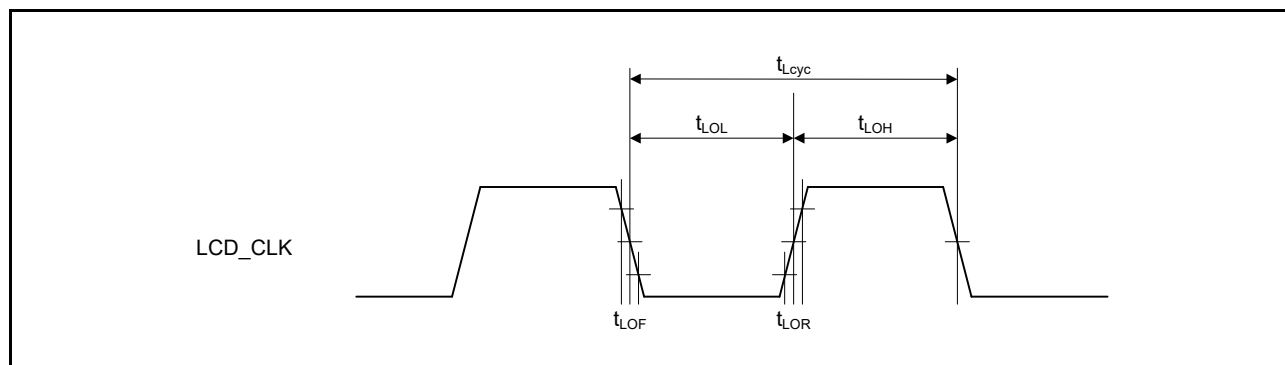
Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF

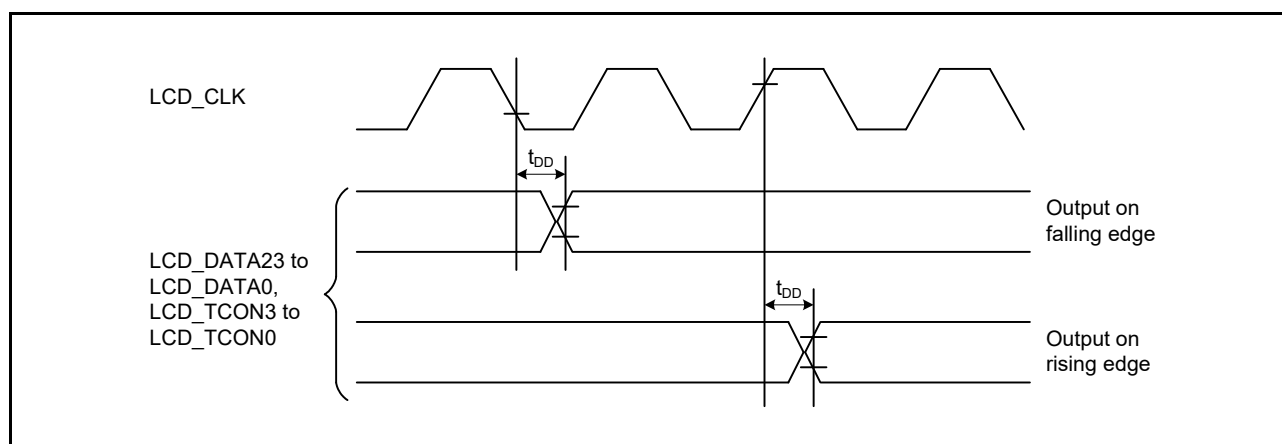
| Item                                    | Symbol        | Min.        | Typ. | Max.     | Unit          | Test Conditions |
|-----------------------------------------|---------------|-------------|------|----------|---------------|-----------------|
| LCD_EXTCLK input clock frequency        | $t_{E_{cyc}}$ | —           | —    | 30*1     | MHz           | Figure 2.79     |
| LCD_EXTCLK input clock low pulse width  | $t_{WL}$      | 0.45        | —    | 0.55     | $t_{E_{cyc}}$ |                 |
| LCD_EXTCLK input clock high pulse width | $t_{WH}$      | 0.45        | —    | 0.55     | $t_{E_{cyc}}$ |                 |
| LCD_CLK output clock frequency          | $t_{L_{cyc}}$ | —           | —    | 30*1     | MHz           | Figure 2.80     |
| LCD_CLK output clock low pulse width    | $t_{LOL}$     | 0.4         | —    | 0.6      | $t_{L_{cyc}}$ |                 |
| LCD_CLK output clock high pulse width   | $t_{LOH}$     | 0.4         | —    | 0.6      | $t_{L_{cyc}}$ |                 |
| LCD_CLK output clock rise time          | $t_{LOR}$     | —           | —    | 5        | ns            |                 |
| LCD_CLK output clock fall time          | $t_{LOF}$     | —           | —    | 5        | ns            |                 |
| LCD data output delay timing            | $t_{DD}$      | $-3.5^{*2}$ | —    | $4^{*2}$ | ns            | Figure 2.81     |

Note 1. Parallel RGB888,666,565: Max. 27 MHz  
 Serial RGB888: Max. 30 MHz (4x speed)

Note 2. When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All GLCDC AC timings are measured in combination with the pins in the same group.

If we use group “-A” and “-B” combination, “LCD data output Delay timing ( $t_{DD}$ )” is Min =  $-5.0$  ns, Max =  $5.5$  ns.

**Figure 2.79 LCD\_EXTCLK Clock Input Timing****Figure 2.80 LCD\_CLK Clock Output Timing**

**Figure 2.81 LCD Output Data Timing**

## 2.4.7.17 SDHI

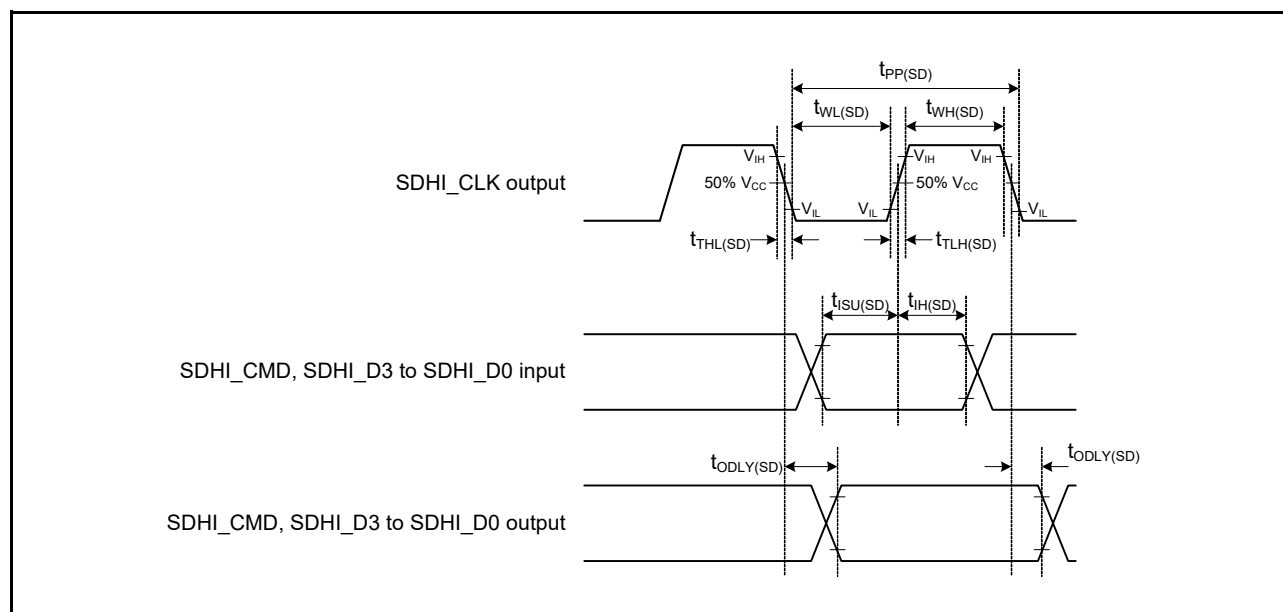
**Table 2.45 SDHI Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the driving ability control register.\*1

| Item |                                                                                      | Symbol                | Min.                      | Max. | Unit | Test Conditions*2 |
|------|--------------------------------------------------------------------------------------|-----------------------|---------------------------|------|------|-------------------|
| SDHI | SDHI_CLK pin output cycle time                                                       | t <sub>PP(SD)</sub>   | 20                        | —    | ns   | Figure 2.82       |
|      | SDHI_CLK pin output high pulse width                                                 | t <sub>WH(SD)</sub>   | 0.4 × t <sub>PP(SD)</sub> | —    | ns   |                   |
|      | SDHI_CLK pin output low pulse width                                                  | t <sub>WL(SD)</sub>   | 0.4 × t <sub>PP(SD)</sub> | —    | ns   |                   |
|      | SDHI_CLK pin output rise time                                                        | t <sub>TLH(SD)</sub>  | —                         | 3    | ns   |                   |
|      | SDHI_CLK pin output fall time                                                        | t <sub>THL(SD)</sub>  | —                         | 3    | ns   |                   |
|      | Output data delay time (data transfer mode) for SDHI_CMD and SDHI_D0 to SDHI_D3 pins | t <sub>ODLY(SD)</sub> | −6.5                      | 4    | ns   |                   |
|      | Input data setup time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins                       | t <sub>ISU(SD)</sub>  | 6                         | —    | ns   |                   |
|      | Input data hold time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins                        | t <sub>IH(SD)</sub>   | 2                         | —    | ns   |                   |

Note 1. In the G-version products, the AC characteristics are measured by setting the drive capacity control register 2 corresponding the SDHI\_CLK-C pin as a high-speed interface high-drive output.

Note 2. When a letter "A", "B", etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All SDHI AC timings are measured in combination with the pins in the same group.

**Figure 2.82 SD Host Interface Input/Output Signal Timing**

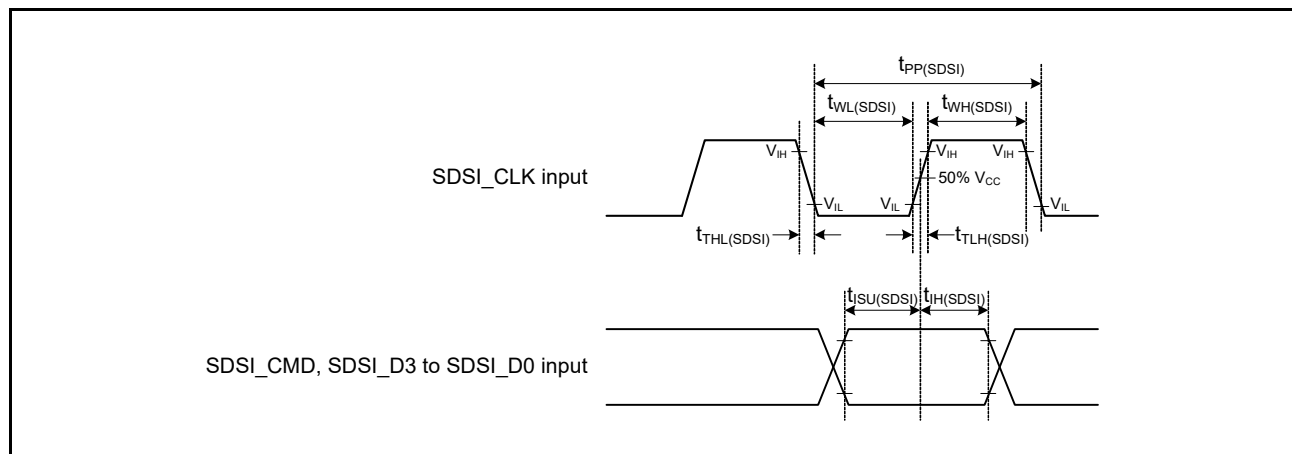
## 2.4.7.18 SDSI

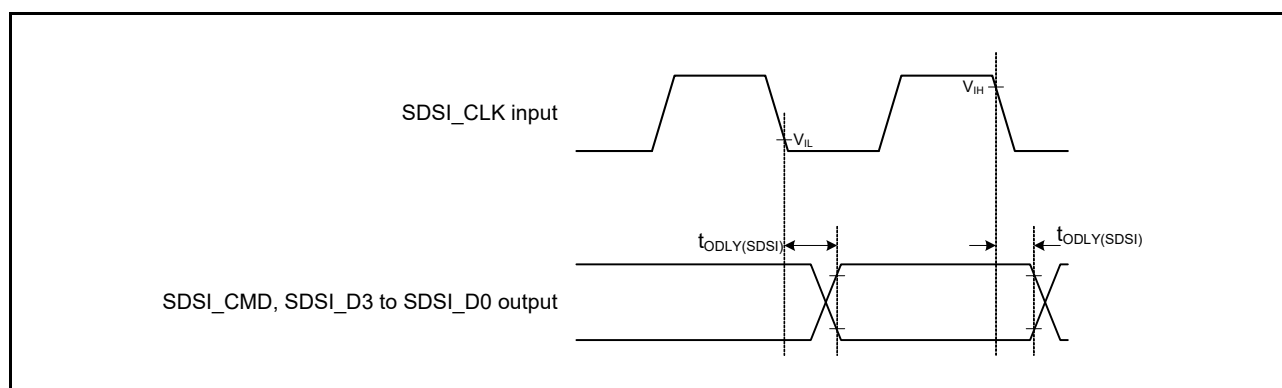
**Table 2.46 SDSI Timing**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKA = 8$  to  $120$  MHz,  $PCLKB = 8$  to  $60$  MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,  
 High-drive output is selected by the driving ability control register.

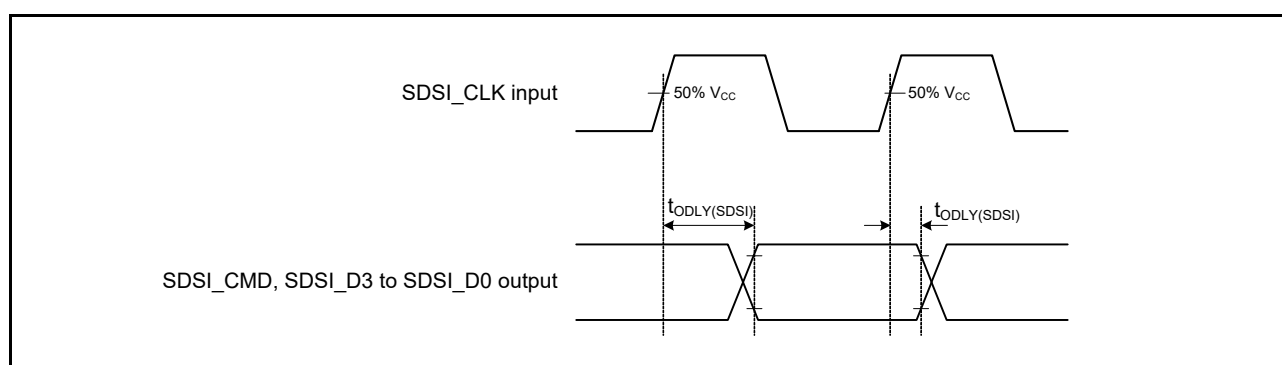
|      | Item                                                                              | Symbol                                                                               | Min.                            | Max. | Unit | Test Conditions*1 |
|------|-----------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|---------------------------------|------|------|-------------------|
| SDSI | SDSI_CLK pin input cycle time                                                     | t <sub>PP</sub> (SDSI)                                                               | 20                              | —    | ns   | Figure 2.83       |
|      | SDSI_CLK pin input high pulse width                                               | t <sub>WH</sub> (SDSI)                                                               | 0.4 ×<br>t <sub>PP</sub> (SDSI) | —    | ns   |                   |
|      | SDSI_CLK pin input low pulse width                                                | t <sub>WL</sub> (SDSI)                                                               | 0.4 ×<br>t <sub>PP</sub> (SDSI) | —    | ns   |                   |
|      | SDSI_CLK pin input rise time                                                      | t <sub>TLH</sub> (SDSI)                                                              | —                               | 3    | ns   |                   |
|      | SDSI_CLK pin input fall time                                                      | t <sub>THL</sub> (SDSI)                                                              | —                               | 3    | ns   |                   |
|      | Input data setup time for SDSI_CMD and SDSI_D0 to SDSI_D3 pins                    | t <sub>SU</sub> (SDSI)                                                               | 5                               | —    | ns   |                   |
|      | Input data hold time for SDSI_CMD and SDSI_D0 to SDSI_D3 pins                     | t <sub>IH</sub> (SDSI)                                                               | 2                               | —    | ns   |                   |
|      |                                                                                   | Output data delay time for SDSI_CMD and SDSI_D0 to SDSI_D3 pins (default speed mode) | t <sub>ODLY</sub> (SDSI)        | 0    | 14   | ns                |
|      | Output data delay time for SDSI_CMD and SDSI_D0 to SDSI_D3 pins (high speed mode) | 2.5                                                                                  |                                 | 14   | ns   | Figure 2.85       |

Note 1. When a letter "A", "B", etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All SDSI AC timings are measured in combination with the pins in the same group.

**Figure 2.83 SD Slave Interface Input Signal Timing**



**Figure 2.84 SD Slave Interface Output Signal Timing (Default Speed Mode)**



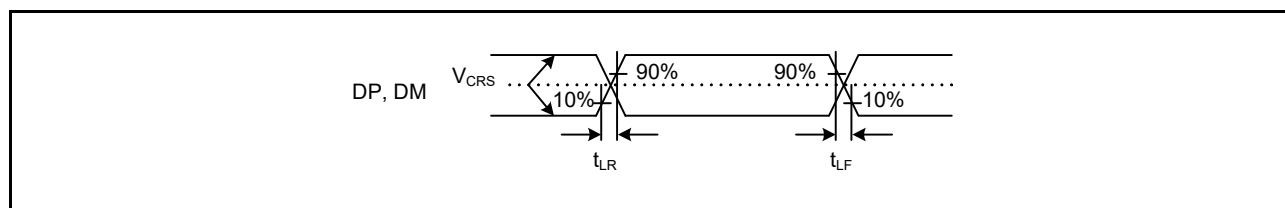
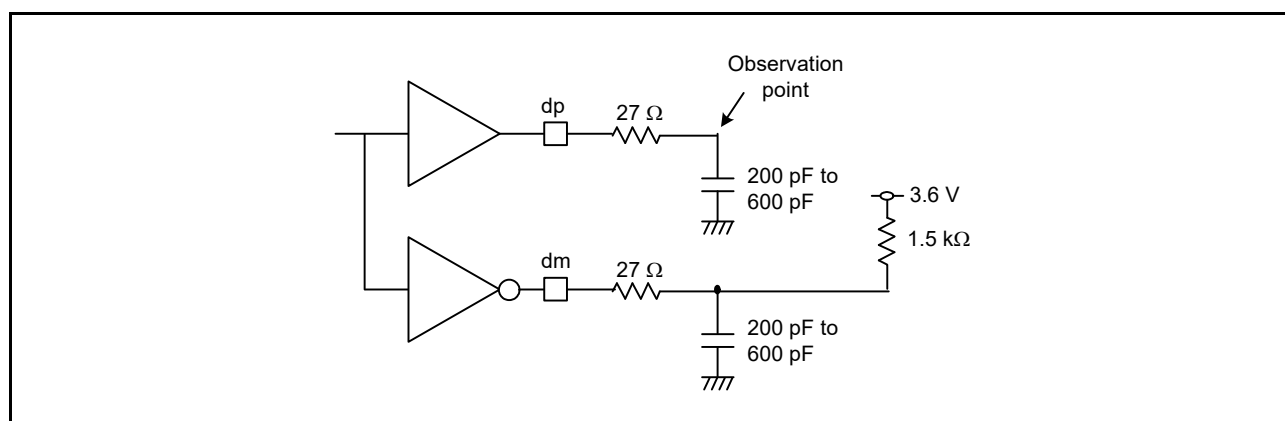
**Figure 2.85 SD Slave Interface Output Signal Timing (High Speed Mode)**

## 2.5 USB Characteristics

**Table 2.47 On-Chip USB Low Speed (Host Only) Characteristics (DP and DM Pin Characteristics)**

Conditions:  $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC\_USB} = V_{BATT} = 3.0$  to  $3.6$  V,  $3.0$  V  $\leq V_{REFH0} \leq AV_{CC0}$ ,  
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $U_{CLK} = 48$  MHz,  $P_{CLKA} = 8$  to  $120$  MHz,  $P_{CLKB} = 8$  to  $60$  MHz,  $T_a = T_{opr}$

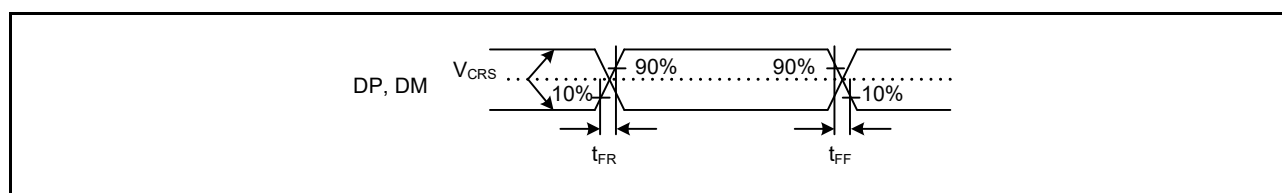
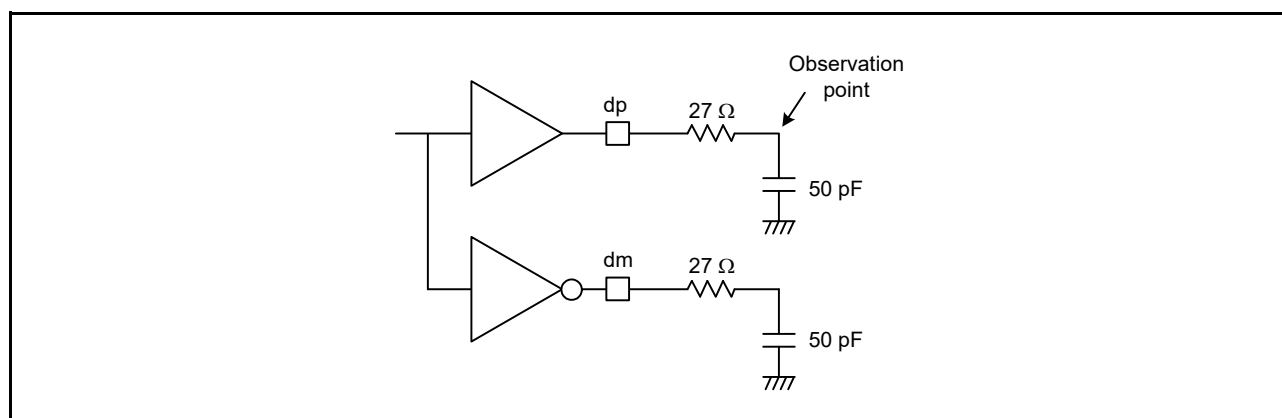
|                           | Item                                                                       | Symbol          | Min.  | Typ. | Max.  | Unit       | Test Conditions         |
|---------------------------|----------------------------------------------------------------------------|-----------------|-------|------|-------|------------|-------------------------|
| Input characteristics     | Input high level voltage                                                   | $V_{IH}$        | 2.0   | —    | —     | V          |                         |
|                           | Input low level voltage                                                    | $V_{IL}$        | —     | —    | 0.8   | V          |                         |
|                           | Differential input sensitivity                                             | $V_{DI}$        | 0.2   | —    | —     | V          | DP – DM                 |
|                           | Differential common mode range                                             | $V_{CM}$        | 0.8   | —    | 2.5   | V          |                         |
| Output characteristics    | Output high level voltage                                                  | $V_{OH}$        | 2.8   | —    | 3.6   | V          | $I_{OH} = -200$ $\mu$ A |
|                           | Output low level voltage                                                   | $V_{OL}$        | 0.0   | —    | 0.3   | V          | $I_{OL} = 2$ mA         |
|                           | Cross-over voltage                                                         | $V_{CRS}$       | 1.3   | —    | 2.0   | V          | Figure 2.86             |
|                           | Rise time                                                                  | $t_{LR}$        | 75    | —    | 300   | ns         |                         |
|                           | Fall time                                                                  | $t_{LF}$        | 75    | —    | 300   | ns         |                         |
|                           | Rise/fall time ratio                                                       | $t_{LR}/t_{LF}$ | 80    | —    | 125   | %          | $t_{LR}/t_{LF}$         |
| Pull-down characteristics | DP/DM pull-down resistance (when the host controller function is selected) | $R_{pd}$        | 14.25 | —    | 24.80 | k $\Omega$ |                         |

**Figure 2.86 DP and DM Output Timing (Low Speed)****Figure 2.87 Test Circuit (Low Speed)**

**Table 2.48 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)**

Conditions:  $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC\_USB} = V_{BATT} = 3.0$  to  $3.6$  V,  $3.0$  V  $\leq V_{REFH0} \leq AV_{CC0}$ ,  
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $U_{CLK} = 48$  MHz,  $P_{CLKA} = 8$  to  $120$  MHz,  $P_{CLKB} = 8$  to  $60$  MHz,  $T_a = T_{opr}$

| Item                                  | Symbol                                                                     | Min.            | Typ.  | Max. | Unit   | Test Conditions |
|---------------------------------------|----------------------------------------------------------------------------|-----------------|-------|------|--------|-----------------|
| Input characteristics                 | Input high level voltage                                                   | $V_{IH}$        | 2.0   | —    | —      | V               |
|                                       | Input low level voltage                                                    | $V_{IL}$        | —     | —    | 0.8    | V               |
|                                       | Differential input sensitivity                                             | $V_{DI}$        | 0.2   | —    | —      | V               |
|                                       | Differential common mode range                                             | $V_{CM}$        | 0.8   | —    | 2.5    | V               |
| Output characteristics                | Output high level voltage                                                  | $V_{OH}$        | 2.8   | —    | 3.6    | V               |
|                                       | Output low level voltage                                                   | $V_{OL}$        | 0.0   | —    | 0.3    | V               |
|                                       | Cross-over voltage                                                         | $V_{CRS}$       | 1.3   | —    | 2.0    | V               |
|                                       | Rise time                                                                  | $t_{FR}$        | 4     | —    | 20     | ns              |
|                                       | Fall time                                                                  | $t_{FF}$        | 4     | —    | 20     | ns              |
|                                       | Rise/fall time ratio                                                       | $t_{FR}/t_{FF}$ | 90    | —    | 111.11 | %               |
|                                       | Output resistance                                                          | $Z_{DRV}$       | 28    | —    | 44     | $\Omega$        |
| Pull-up and pull-down characteristics | DP pull-up resistance (when the function controller function is selected)  | $R_{pu}$        | 0.900 | —    | 1.575  | k $\Omega$      |
|                                       |                                                                            |                 | 1.425 | —    | 3.090  | k $\Omega$      |
|                                       | DP/DM pull-down resistance (when the host controller function is selected) | $R_{pd}$        | 14.25 | —    | 24.80  | k $\Omega$      |

**Figure 2.88 DP and DM Output Timing (Full-Speed)****Figure 2.89 Test Circuit (Full-Speed)**

## 2.6 A/D Conversion Characteristics

**Table 2.49 12-Bit A/D (Unit 0) Conversion Characteristics**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKB = PCLKC = 1$  MHz to  $60$  MHz,  $T_a = T_{opr}$ ,  
Source impedance =  $1.0$  k $\Omega$

| Item                                                                   |                                                     | Min.                   | Typ.      | Max.               | Unit    | Test Conditions                                                                                                                                      |
|------------------------------------------------------------------------|-----------------------------------------------------|------------------------|-----------|--------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| Resolution                                                             |                                                     | 8                      | —         | 12                 | Bit     |                                                                                                                                                      |
| Analog input capacitance                                               |                                                     | —                      | —         | 30                 | pF      |                                                                                                                                                      |
| Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)     | Conversion time*1 (Operation at PCLKC = 60 MHz)     | 1.06<br>(0.4 + 0.25)*2 | —         | —                  | $\mu$ s | <ul style="list-style-type: none"> <li>Sampling of channel-dedicated sample-and-hold circuits in 24 states</li> <li>Sampling in 15 states</li> </ul> |
|                                                                        | Offset error                                        | —                      | $\pm 1.5$ | $\pm 3.5$          | LSB     | AN000 to AN002 = 0.25 V                                                                                                                              |
|                                                                        | Full-scale error                                    | —                      | $\pm 1.5$ | $\pm 3.5$          | LSB     | AN000 to AN002 = $V_{REFH0} - 0.25$ V                                                                                                                |
|                                                                        | Quantization error                                  | —                      | $\pm 0.5$ | —                  | LSB     |                                                                                                                                                      |
|                                                                        | Absolute accuracy                                   | —                      | $\pm 3.0$ | $\pm 5.5$          | LSB     |                                                                                                                                                      |
|                                                                        | DNL differential nonlinearity error                 | —                      | $\pm 1.0$ | $\pm 2.0$          | LSB     |                                                                                                                                                      |
|                                                                        | INL integral nonlinearity error                     | —                      | $\pm 1.5$ | $\pm 3.0$          | LSB     |                                                                                                                                                      |
|                                                                        | Holding characteristics of sample-and-hold circuits | —                      | —         | 20                 | $\mu$ s |                                                                                                                                                      |
|                                                                        | Dynamic range                                       | 0.25                   | —         | $V_{REFH0} - 0.25$ | V       |                                                                                                                                                      |
| Channel-dedicated sample-and-hold circuits not in use (AN000 to AN007) | Conversion time*1 (Operation at PCLKC = 60 MHz)     | 0.48<br>(0.267)*2      | —         | —                  | $\mu$ s | Sampling in 16 states                                                                                                                                |
|                                                                        | Offset error                                        | —                      | $\pm 1.0$ | $\pm 2.5$          | LSB     |                                                                                                                                                      |
|                                                                        | Full-scale error                                    | —                      | $\pm 1.0$ | $\pm 2.5$          | LSB     |                                                                                                                                                      |
|                                                                        | Quantization error                                  | —                      | $\pm 0.5$ | —                  | LSB     |                                                                                                                                                      |
|                                                                        | Absolute accuracy                                   | —                      | $\pm 2.5$ | $\pm 4.5$          | LSB     |                                                                                                                                                      |
|                                                                        | DNL differential nonlinearity error                 | —                      | $\pm 0.5$ | $\pm 1.5$          | LSB     |                                                                                                                                                      |
|                                                                        | INL integral nonlinearity error                     | —                      | $\pm 1.0$ | $\pm 2.5$          | LSB     |                                                                                                                                                      |

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

**Table 2.50 12-Bit A/D (Unit 1) Conversion Characteristics**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKB = PCLKD = 1$  MHz to  $60$  MHz,  $T_a = T_{opr}$ ,  
Source impedance =  $1.0$  k $\Omega$

| Item                                                                 | Min.              | Typ.      | Max.      | Unit    | Test Conditions                          |
|----------------------------------------------------------------------|-------------------|-----------|-----------|---------|------------------------------------------|
| Resolution                                                           | 8                 | —         | 12        | Bit     |                                          |
| Conversion time*1<br>(Operation at PCLKD = 60 MHz)                   | 0.88<br>(0.633)*2 | —         | —         | $\mu$ s | Sampling in 38 states<br>(ADSAM.SAM = 1) |
| Conversion time*1<br>(Operation at PCLKD = 30 MHz)                   | 1<br>(0.500)*2    | —         | —         | $\mu$ s | Sampling in 15 states<br>(ADSAM.SAM = 1) |
| Analog input capacitance                                             | —                 | —         | 30        | pF      |                                          |
| Offset error                                                         | —                 | $\pm 2.0$ | $\pm 3.5$ | LSB     |                                          |
| Full-scale error                                                     | —                 | $\pm 2.0$ | $\pm 3.5$ | LSB     |                                          |
| Quantization error                                                   | —                 | $\pm 0.5$ | —         | LSB     |                                          |
| Absolute accuracy                                                    | —                 | $\pm 4.0$ | $\pm 6.0$ | LSB     |                                          |
| DNL differential nonlinearity error<br>(Operation at PCLKD = 60 MHz) | —                 | $\pm 1.5$ | $\pm 4.0$ | LSB     |                                          |
| DNL differential nonlinearity error<br>(Operation at PCLKD = 30 MHz) | —                 | $\pm 1.5$ | $\pm 2.5$ | LSB     |                                          |
| INL integral nonlinearity error<br>(Operation at PCLKD = 60 MHz)     | —                 | $\pm 2.0$ | $\pm 4.0$ | LSB     |                                          |
| INL integral nonlinearity error<br>(Operation at PCLKD = 30 MHz)     | —                 | $\pm 2.0$ | $\pm 3.5$ | LSB     |                                          |

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

**Table 2.51 A/D Internal Reference Voltage Characteristics**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $PCLKB = PCLKD = 60$  MHz,  $T_a = T_{opr}$

| Item                           | Min. | Typ. | Max. | Unit | Test Conditions |
|--------------------------------|------|------|------|------|-----------------|
| A/D internal reference voltage | 1.13 | 1.18 | 1.23 | V    |                 |

## 2.7 D/A Conversion Characteristics

**Table 2.52 D/A Conversion Characteristics**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $T_a = T_{opr}$

| Item              |                                 | Symbol | Min. | Typ.      | Max.          | Unit       | Test Conditions                                  |
|-------------------|---------------------------------|--------|------|-----------|---------------|------------|--------------------------------------------------|
| Resolution        |                                 | —      | 12   | 12        | 12            | Bit        |                                                  |
| Unbuffered output | Absolute accuracy               | —      | —    | —         | $\pm 6.0$     | LSB        | 2-M $\Omega$ resistive load<br>10-bit conversion |
|                   | Differential nonlinearity error | DNL    | —    | $\pm 1.0$ | $\pm 2.0$     | LSB        | 2-M $\Omega$ resistive load                      |
|                   | Output resistance               | $R_O$  | —    | 8.6       | —             | k $\Omega$ |                                                  |
|                   | Setting time                    | $t_S$  | —    | —         | 3             | $\mu$ s    | 20-pF capacitive load                            |
| Buffered output   | Load resistance                 | $R_L$  | 5    | —         | —             | k $\Omega$ |                                                  |
|                   | Load capacitance                | $C_L$  | —    | —         | 50            | pF         |                                                  |
|                   | Output voltage                  | $V_O$  | 0.2  | —         | $AVCC1 - 0.2$ | V          |                                                  |
|                   | Differential nonlinearity error | DNL    | —    | $\pm 1.0$ | $\pm 2.0$     | LSB        |                                                  |
|                   | Integral nonlinearity error     | INL    | —    | $\pm 2.0$ | $\pm 4.0$     | LSB        |                                                  |
|                   | Setting time                    | $t_S$  | —    | —         | 4             | $\mu$ s    |                                                  |

## 2.8 Temperature Sensor Characteristics

**Table 2.53 Temperature Sensor Characteristics**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $T_a = T_{opr}$

| Item                          | Min. | Typ.    | Max. | Unit             | Test Conditions      |
|-------------------------------|------|---------|------|------------------|----------------------|
| Relative accuracy             | —    | $\pm 1$ | —    | $^{\circ}$ C     |                      |
| Temperature slope             | —    | 4       | —    | mV/ $^{\circ}$ C |                      |
| Output voltage                | —    | 1.21    | —    | V                | $T_a = 25^{\circ}$ C |
| Temperature sensor start time | —    | —       | 30   | $\mu$ s          |                      |
| Sampling time*1               | 4.15 | —       | —    | $\mu$ s          |                      |

Note 1. Set the S12AD1.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.

## 2.9 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

**Table 2.54 Power-on Reset Circuit and Voltage Detection Circuit Characteristics**

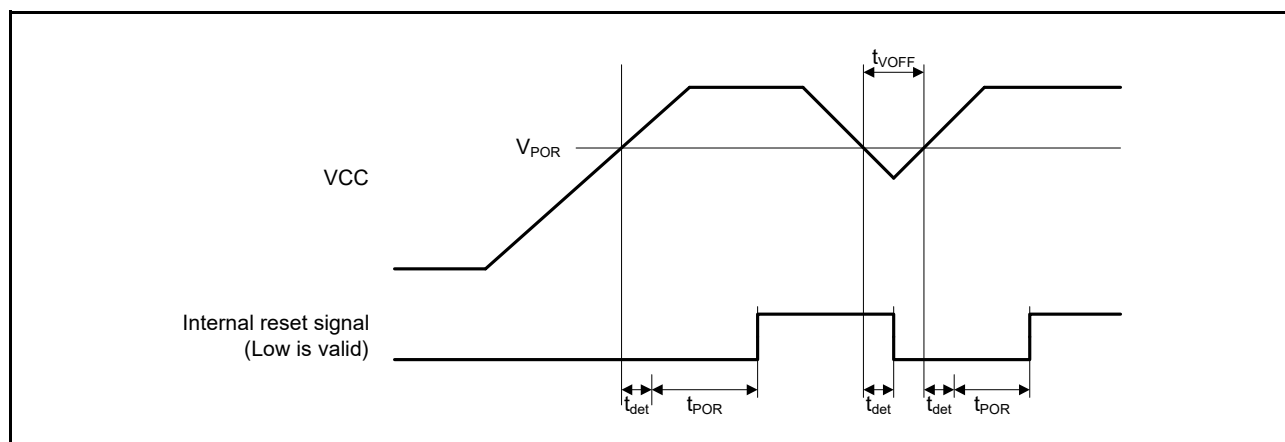
Conditions:  $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AV_{CC0}$ ,  
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 $T_a = T_{opr}$

| Item                                                    |                                  |                                           | Symbol              | Min. | Typ. | Max. | Unit | Test Conditions            |
|---------------------------------------------------------|----------------------------------|-------------------------------------------|---------------------|------|------|------|------|----------------------------|
| Voltage detection level                                 | Power-on reset (POR)             | Low power consumption function disabled*1 | V <sub>POR</sub>    | 2.5  | 2.6  | 2.7  | V    | Figure 2.90                |
|                                                         |                                  | Low power consumption function enabled*2  |                     | 1.8  | 2.25 | 2.7  |      |                            |
|                                                         | Voltage detection circuit (LVD0) |                                           | V <sub>det0_1</sub> | 2.84 | 2.94 | 3.04 |      | Figure 2.91                |
|                                                         |                                  |                                           | V <sub>det0_2</sub> | 2.77 | 2.87 | 2.97 |      |                            |
|                                                         |                                  |                                           | V <sub>det0_3</sub> | 2.70 | 2.80 | 2.90 |      |                            |
|                                                         | Voltage detection circuit (LVD1) |                                           | V <sub>det1_1</sub> | 2.89 | 2.99 | 3.09 |      | Figure 2.92                |
|                                                         |                                  |                                           | V <sub>det1_2</sub> | 2.82 | 2.92 | 3.02 |      |                            |
|                                                         |                                  |                                           | V <sub>det1_3</sub> | 2.75 | 2.85 | 2.95 |      |                            |
|                                                         | Voltage detection circuit (LVD2) |                                           | V <sub>det2_1</sub> | 2.89 | 2.99 | 3.09 |      | Figure 2.93                |
|                                                         |                                  |                                           | V <sub>det2_2</sub> | 2.82 | 2.92 | 3.02 |      |                            |
|                                                         |                                  |                                           | V <sub>det2_3</sub> | 2.75 | 2.85 | 2.95 |      |                            |
| Internal reset time                                     | Power-on reset time              |                                           | t <sub>POR</sub>    | —    | 4.6  | —    | ms   | Figure 2.90                |
|                                                         | LVD0 reset time                  |                                           | t <sub>LVD0</sub>   | —    | 0.70 | —    |      | Figure 2.91                |
|                                                         | LVD1 reset time                  |                                           | t <sub>LVD1</sub>   | —    | 0.57 | —    |      | Figure 2.92                |
|                                                         | LVD2 reset time                  |                                           | t <sub>LVD2</sub>   | —    | 0.57 | —    |      | Figure 2.93                |
| Minimum VCC down time                                   |                                  |                                           | t <sub>VOFF</sub>   | 200  | —    | —    | μs   | Figure 2.90, Figure 2.91   |
| Response delay time                                     |                                  |                                           | t <sub>det</sub>    | —    | —    | 200  | μs   | Figure 2.90 to Figure 2.93 |
| LVD operation stabilization time (after LVD is enabled) |                                  |                                           | t <sub>d(E-A)</sub> | —    | —    | 10   | μs   | Figure 2.92, Figure 2.93   |
| Hysteresis width (LVD1 and LVD2)                        |                                  |                                           | V <sub>LVH</sub>    | —    | 70   | —    | mV   |                            |

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels  $V_{POR}$ ,  $V_{det1}$ , and  $V_{det2}$  for the POR/ LVD.

Note 1. The low power consumption function is disabled and DEEPCUT[1:0] = 00b or 01b.

Note 2. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

**Figure 2.90 Power-on Reset Timing**

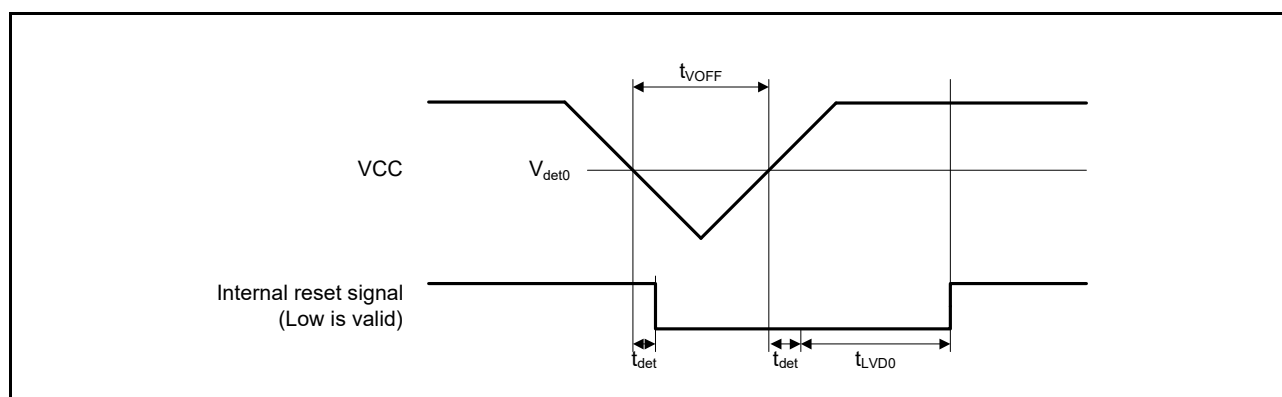


Figure 2.91 Voltage Detection Circuit Timing ( $V_{det0}$ )

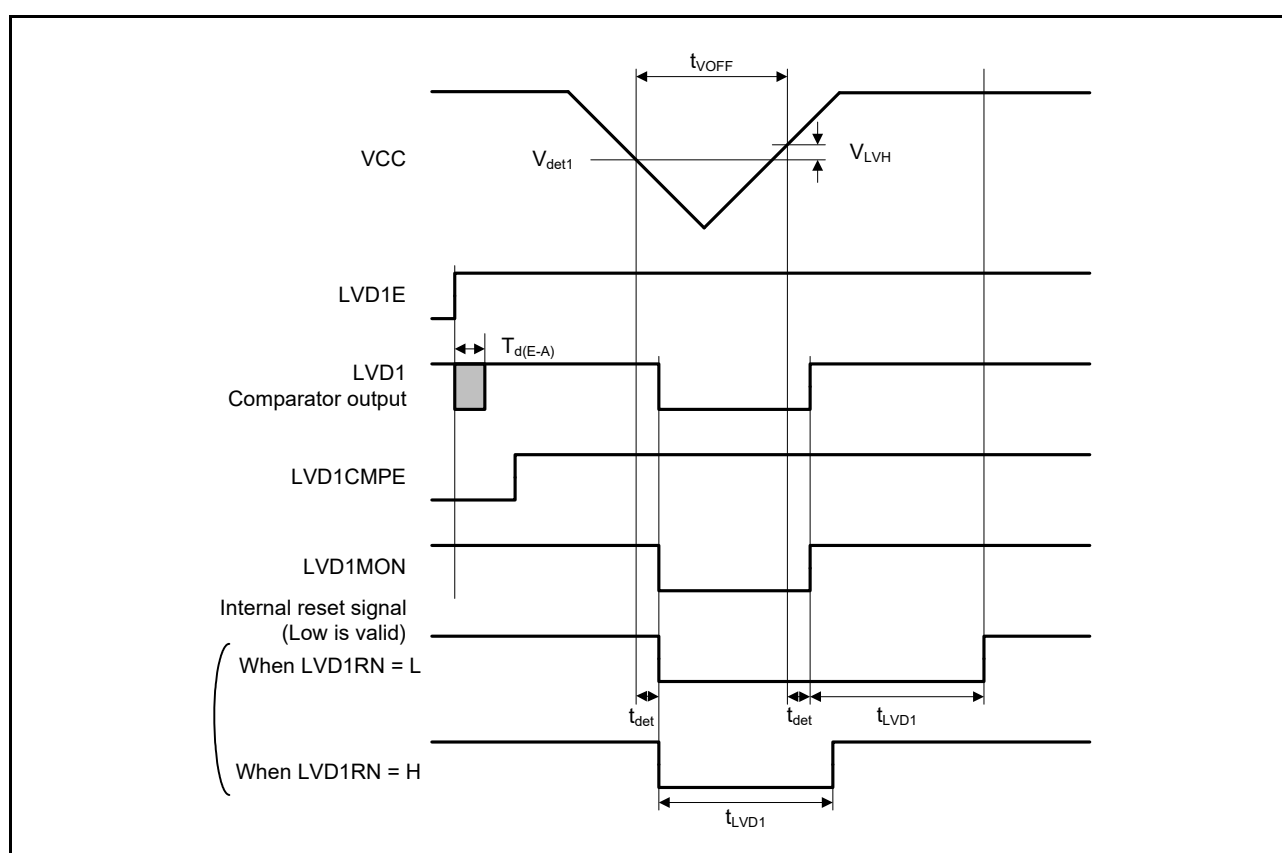
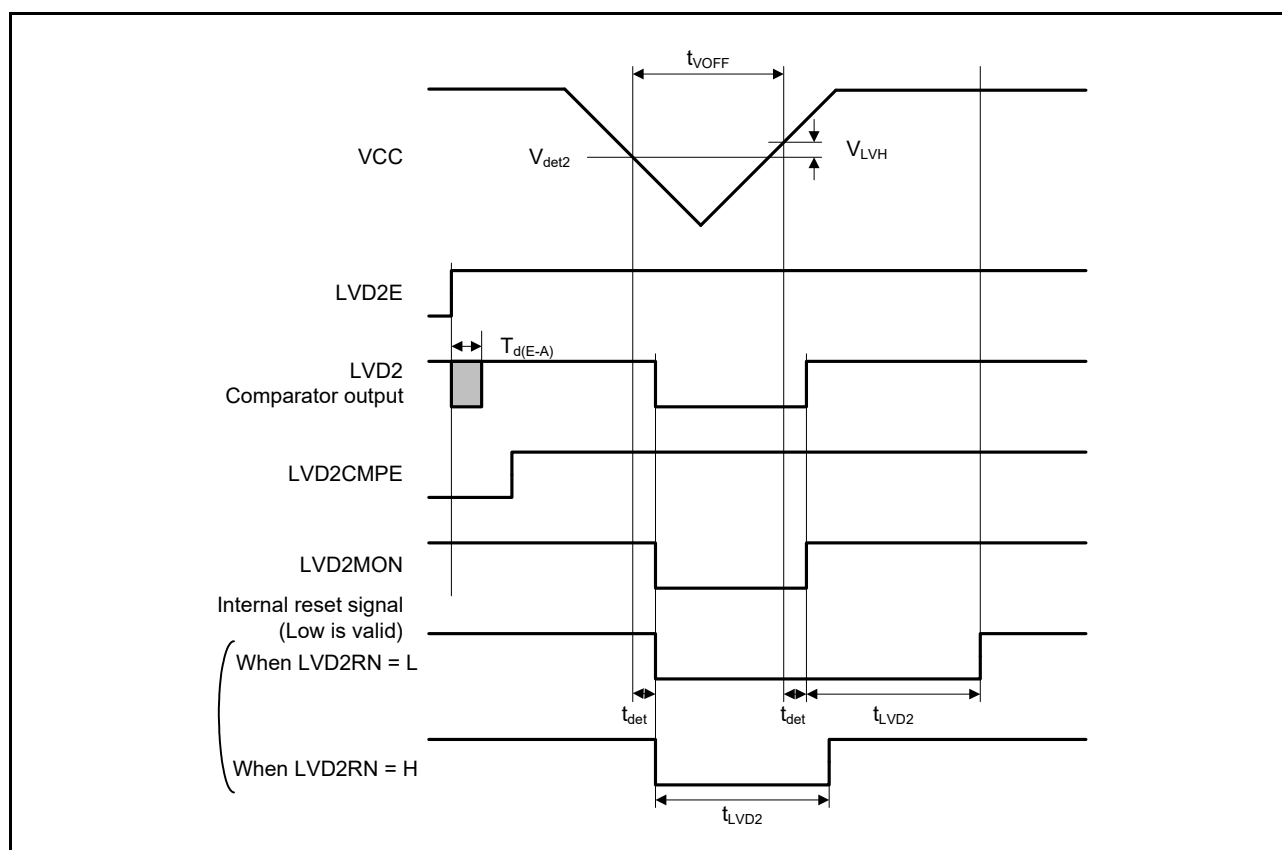


Figure 2.92 Voltage Detection Circuit Timing ( $V_{det1}$ )



**Figure 2.93** Voltage Detection Circuit Timing (V<sub>det2</sub>)

2.10 Oscillation Stop Detection Timing

**Table 2.55 Oscillation Stop Detection Circuit Characteristics**  
Conditions: VCC = AVCC0 = AVCC1 = VCC\_USB = V<sub>BATT</sub> = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,  
VSS = AVSS0 = AVSS1 = VREFL0 = VSS\_USB = 0 V,  
T<sub>a</sub> = T<sub>opr</sub>

| Item           | Symbol          | Min. | Typ. | Max. | Unit | Test Conditions |
|----------------|-----------------|------|------|------|------|-----------------|
| Detection time | t <sub>dr</sub> | —    | —    | 1    | ms   | Figure 2.94     |

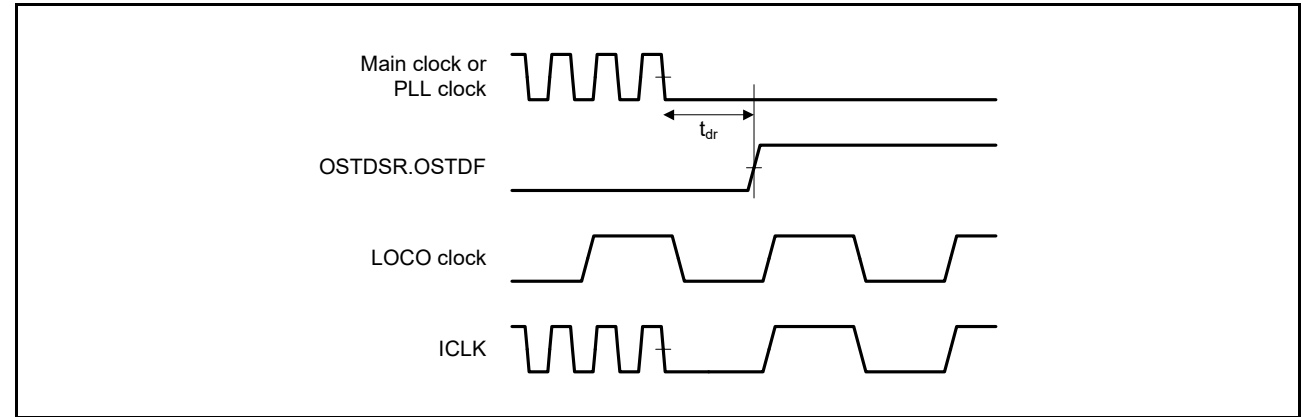


Figure 2.94 Oscillation Stop Detection Timing

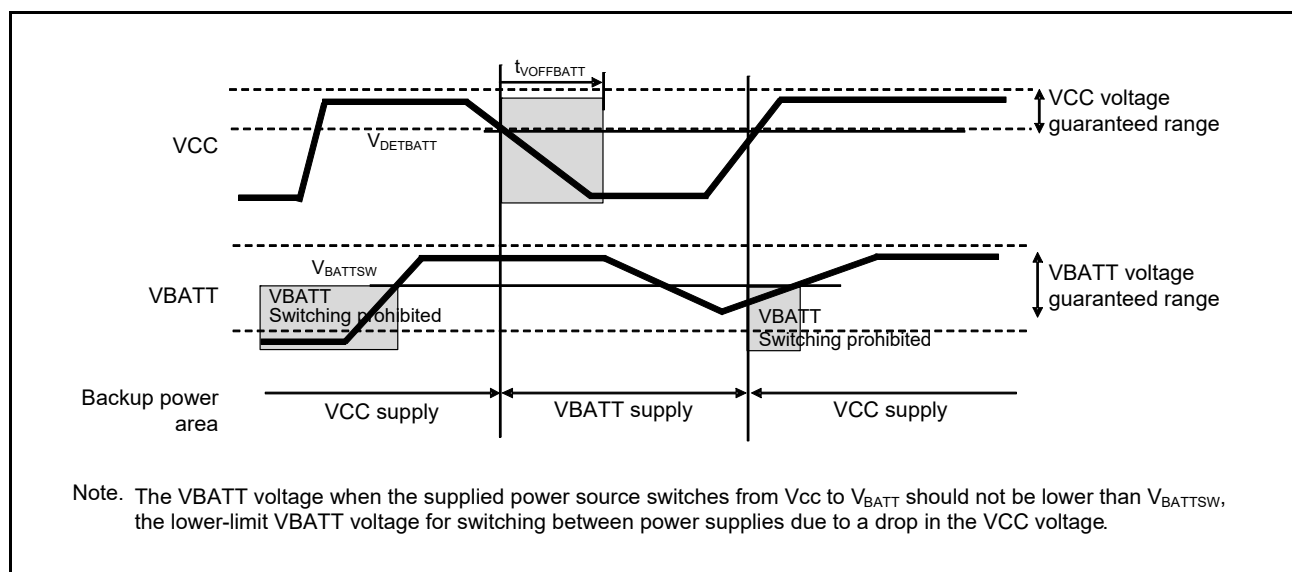
## 2.11 Battery Backup Function Characteristics

### Table 2.56 Battery Backup Function Characteristics

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = 2.7 \text{ to } 3.6 \text{ V}$ ,  $2.7 \text{ V} \leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0 \text{ V}$ ,  
 $V_{BATT} = 1.62 \text{ to } 3.6 \text{ V}$ ,  $T_a = T_{opr}$

| Item                                                                                     | Symbol                | Min. | Typ. | Max. | Unit | Test Conditions |
|------------------------------------------------------------------------------------------|-----------------------|------|------|------|------|-----------------|
| Voltage level for switching to battery backup                                            | V <sub>DETBATT</sub>  | 2.50 | 2.60 | 2.70 | V    | Figure 2.95     |
| Lower-limit V <sub>BATT</sub> voltage for power supply switching due to VCC voltage drop | V <sub>BATTSW</sub>   | 2.70 | —    | —    |      |                 |
| VCC-off period for starting power supply switching                                       | t <sub>VOFFBATT</sub> | 200  | —    | —    | μs   |                 |

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ( $V_{DET BATT}$ ).



**Figure 2.95 Battery Backup Function Characteristics**

## 2.12 Flash Memory Characteristics

**Table 2.57 Code Flash Memory Characteristics**

Conditions:  $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AV_{CC0}$ ,  
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 Temperature range for programming/erase:  $T_a = T_{opr}$

| Item                                                                   |           | Symbol             | FCLK = 4 MHz |      |      | FCLK = 15 MHz |      |      | 20 MHz ≤ FCLK ≤ 60 MHz |      |      | Unit  | Test Conditions        |
|------------------------------------------------------------------------|-----------|--------------------|--------------|------|------|---------------|------|------|------------------------|------|------|-------|------------------------|
|                                                                        |           |                    | Min.         | Typ. | Max. | Min.          | Typ. | Max. | Min.                   | Typ. | Max. |       |                        |
| Programming time<br>N <sub>PEC</sub> ≤ 100 times                       | 128 bytes | t <sub>P128</sub>  | —            | 0.75 | 13.2 | —             | 0.38 | 6.6  | —                      | 0.34 | 6    | ms    |                        |
|                                                                        | 8 Kbytes  | t <sub>P8K</sub>   | —            | 49   | 176  | —             | 25   | 88   | —                      | 22   | 80   | ms    |                        |
|                                                                        | 32 Kbytes | t <sub>P32K</sub>  | —            | 194  | 704  | —             | 97   | 352  | —                      | 88   | 320  | ms    |                        |
| Programming time<br>N <sub>PEC</sub> > 100 times                       | 128 bytes | t <sub>P128</sub>  | —            | 0.91 | 15.8 | —             | 0.46 | 8    | —                      | 0.41 | 7.2  | ms    |                        |
|                                                                        | 8 Kbytes  | t <sub>P8K</sub>   | —            | 60   | 212  | —             | 30   | 106  | —                      | 27   | 96   | ms    |                        |
|                                                                        | 32 Kbytes | t <sub>P32K</sub>  | —            | 234  | 848  | —             | 117  | 424  | —                      | 106  | 384  | ms    |                        |
| Erasure time<br>N <sub>PEC</sub> ≤ 100 times                           | 8 Kbytes  | t <sub>E8K</sub>   | —            | 78   | 216  | —             | 48   | 132  | —                      | 43   | 120  | ms    |                        |
|                                                                        | 32 Kbytes | t <sub>E32K</sub>  | —            | 283  | 864  | —             | 173  | 528  | —                      | 157  | 480  | ms    |                        |
| Erasure time<br>N <sub>PEC</sub> > 100 times                           | 8 Kbytes  | t <sub>E8K</sub>   | —            | 94   | 260  | —             | 58   | 158  | —                      | 52   | 144  | ms    |                        |
|                                                                        | 32 Kbytes | t <sub>E32K</sub>  | —            | 341  | 1040 | —             | 208  | 632  | —                      | 189  | 576  | ms    |                        |
| Programming/erasure cycle*1                                            |           | N <sub>PEC</sub>   | 10000<br>*2  | —    | —    | 10000<br>*2   | —    | —    | 10000<br>*2            | —    | —    | Times |                        |
| Suspend delay time during programming                                  |           | t <sub>SPD</sub>   | —            | —    | 264  | —             | —    | 132  | —                      | —    | 120  | μs    |                        |
| First suspend delay time during erasing<br>(in suspend priority mode)  |           | t <sub>SESD1</sub> | —            | —    | 216  | —             | —    | 132  | —                      | —    | 120  | μs    |                        |
| Second suspend delay time during erasure<br>(in suspend priority mode) |           | t <sub>SESD2</sub> | —            | —    | 1.7  | —             | —    | 1.7  | —                      | —    | 1.7  | ms    |                        |
| Suspend delay time during erasure<br>(in erasure priority mode)        |           | t <sub>SEED</sub>  | —            | —    | 1.7  | —             | —    | 1.7  | —                      | —    | 1.7  | ms    |                        |
| Forced stop command                                                    |           | t <sub>FD</sub>    | —            | —    | 32   | —             | —    | 22   | —                      | —    | 20   | μs    |                        |
| Data hold time*3, *4                                                   |           | t <sub>DRP</sub>   | 20           | —    | —    | 20            | —    | —    | 20                     | —    | —    | Year  | T <sub>a</sub> ≤ 85°C  |
|                                                                        |           |                    | 10           | —    | —    | 10            | —    | —    | 10                     | —    | —    |       | T <sub>a</sub> ≤ 105°C |

Note 1. Definition of program/erase cycle:

The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is  $n$ , each block can be erased  $n$  times. For instance, when 128-byte program is performed 64 times for different addresses in 8-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.

Note 4. These values are based on the results of reliability testing.

**Table 2.58 Data Flash Memory Characteristics**

Conditions:  $V_{CC} = AVCC0 = AVCC1 = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AVCC0$ ,  
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS\_USB} = 0$  V,  
 Temperature range for programming/erasure:  $T_a = T_{opr}$

| Item                                                                |           | Symbol      | FCLK = 4 MHz |      |      | FCLK = 15 MHz |      |      | 20 MHz $\leq$ FCLK $\leq$ 60 MHz |      |      | Unit    | Test Conditions              |
|---------------------------------------------------------------------|-----------|-------------|--------------|------|------|---------------|------|------|----------------------------------|------|------|---------|------------------------------|
|                                                                     |           |             | Min.         | Typ. | Max. | Min.          | Typ. | Max. | Min.                             | Typ. | Max. |         |                              |
| Programming time                                                    | 4 bytes   | $t_{DP4}$   | —            | 0.36 | 3.8  | —             | 0.18 | 1.9  | —                                | 0.16 | 1.7  | ms      |                              |
| Erasure time                                                        | 64 bytes  | $t_{DP64}$  | —            | 3.1  | 18   | —             | 1.9  | 11   | —                                | 1.7  | 10   | ms      |                              |
|                                                                     | 128 bytes | $t_{DP128}$ | —            | 4.7  | 27   | —             | 2.9  | 16   | —                                | 2.6  | 15   | ms      |                              |
|                                                                     | 256 bytes | $t_{DP256}$ | —            | 8.9  | 50   | —             | 5.4  | 31   | —                                | 4.9  | 28   | ms      |                              |
| Blank check time                                                    | 4 bytes   | $t_{DBC4}$  | —            | —    | 84   | —             | —    | 33   | —                                | —    | 30   | $\mu$ s |                              |
|                                                                     | 64 bytes  | $t_{DBC64}$ | —            | —    | 280  | —             | —    | 110  | —                                | —    | 100  | $\mu$ s |                              |
|                                                                     | 2 Kbytes  | $t_{DBC2K}$ | —            | —    | 6160 | —             | —    | 2420 | —                                | —    | 2200 | $\mu$ s |                              |
| Programming/erasure cycle*1                                         |           | $N_{DPEC}$  | 100000<br>*2 | —    | —    | 100000<br>*2  | —    | —    | 100000<br>*2                     | —    | —    | Times   |                              |
| Suspend delay time during programming                               |           | $t_{DSPD}$  | —            | —    | 264  | —             | —    | 132  | —                                | —    | 120  | $\mu$ s |                              |
| First suspend delay time during erasure (in suspend priority mode)  | 64 bytes  | —           | —            | —    | 216  | —             | —    | 132  | —                                | —    | 120  | $\mu$ s |                              |
|                                                                     | 128 bytes | —           | —            | —    | 216  | —             | —    | 132  | —                                | —    | 120  | $\mu$ s |                              |
|                                                                     | 256 bytes | —           | —            | —    | 216  | —             | —    | 132  | —                                | —    | 120  | $\mu$ s |                              |
| Second suspend delay time during erasure (in suspend priority mode) | 64 bytes  | —           | —            | —    | 300  | —             | —    | 300  | —                                | —    | 300  | $\mu$ s |                              |
|                                                                     | 128 bytes | —           | —            | —    | 390  | —             | —    | 390  | —                                | —    | 390  | $\mu$ s |                              |
|                                                                     | 256 bytes | —           | —            | —    | 570  | —             | —    | 570  | —                                | —    | 570  | $\mu$ s |                              |
| Suspend delay time during erasing (in suspend priority mode)        | 64 bytes  | —           | —            | —    | 300  | —             | —    | 300  | —                                | —    | 300  | $\mu$ s |                              |
|                                                                     | 128 bytes | —           | —            | —    | 390  | —             | —    | 390  | —                                | —    | 390  | $\mu$ s |                              |
|                                                                     | 256 bytes | —           | —            | —    | 570  | —             | —    | 570  | —                                | —    | 570  | $\mu$ s |                              |
| Forced stop command                                                 |           | $t_{FD}$    | —            | —    | 32   | —             | —    | 22   | —                                | —    | 20   | $\mu$ s |                              |
| Data hold time*3, *4                                                |           | $t_{DDRP}$  | 20           | —    | —    | 20            | —    | —    | 20                               | —    | —    | Year    | $T_a \leq 85^\circ\text{C}$  |
|                                                                     |           |             | 10           | —    | —    | 10            | —    | —    | 10                               | —    | —    |         | $T_a \leq 105^\circ\text{C}$ |

Note 1. Definition of program/erase cycle:

The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 4-byte program is performed 512 times for different addresses in 2-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.

Note 4. These values are based on the results of reliability testing.

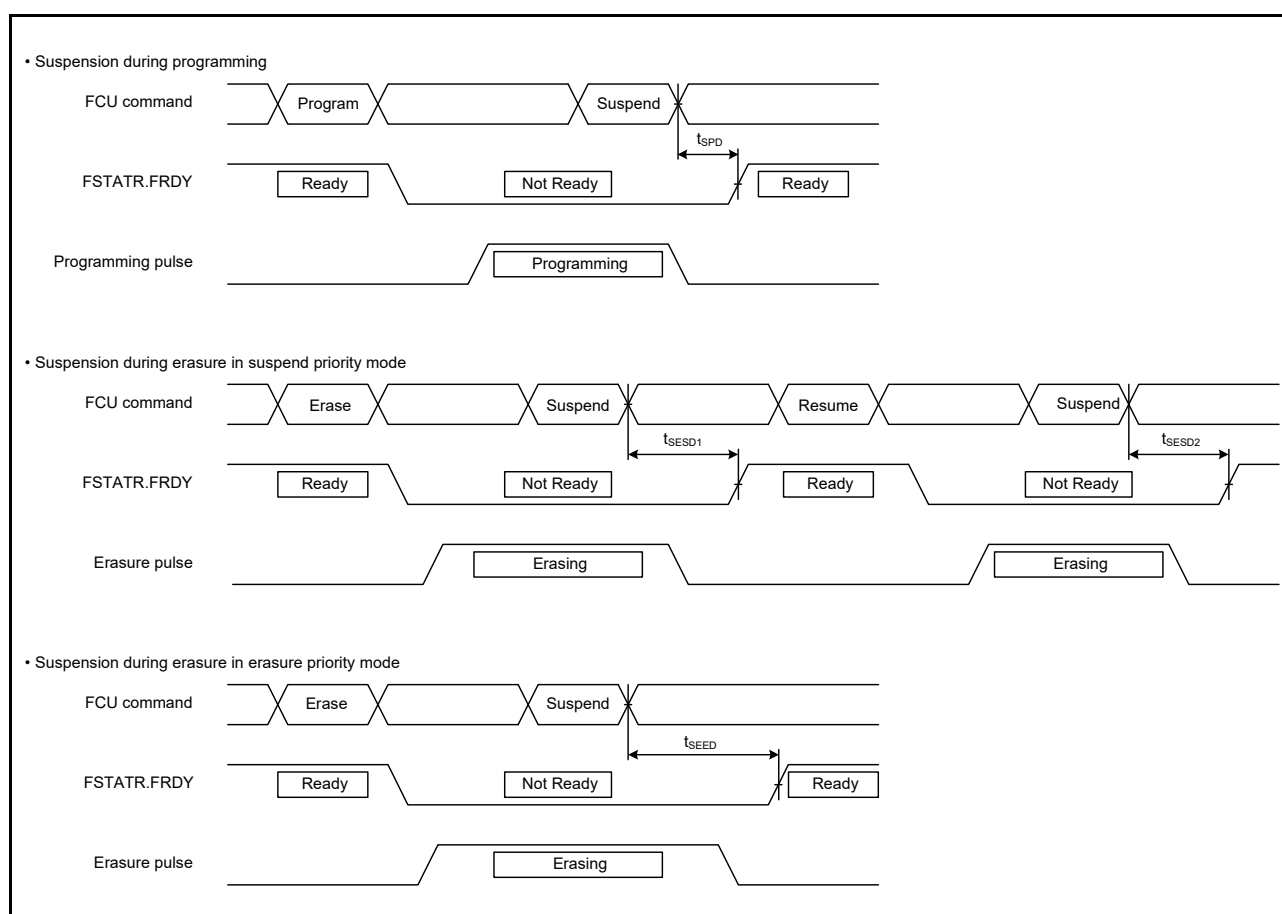


Figure 2.96 Flash Memory Programming/Erase Suspension Timing

## 2.13 Boundary Scan

**Table 2.59 Boundary Scan Characteristics**

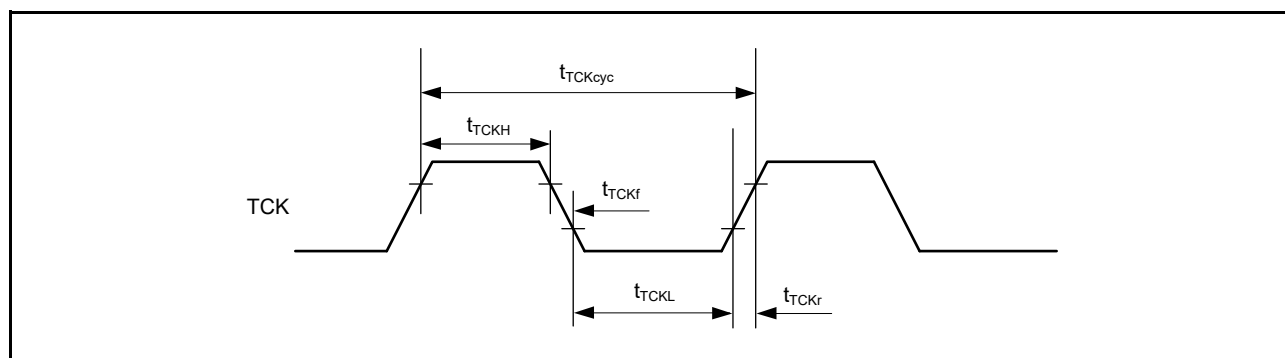
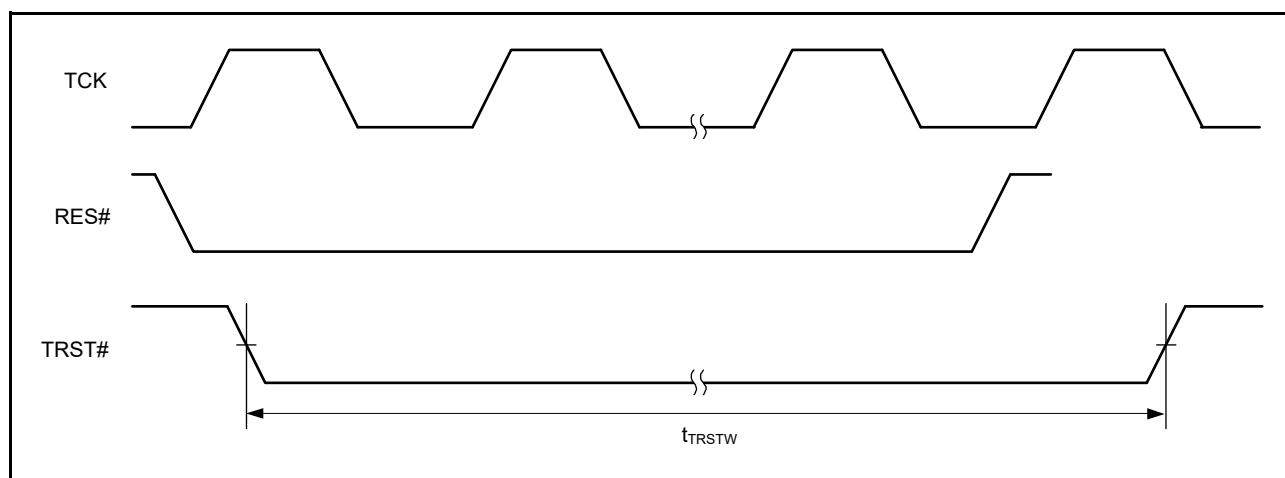
Conditions:  $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC\_USB} = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq V_{REFH0} \leq AV_{CC0}$ ,  
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS\_USB} = 0$  V,

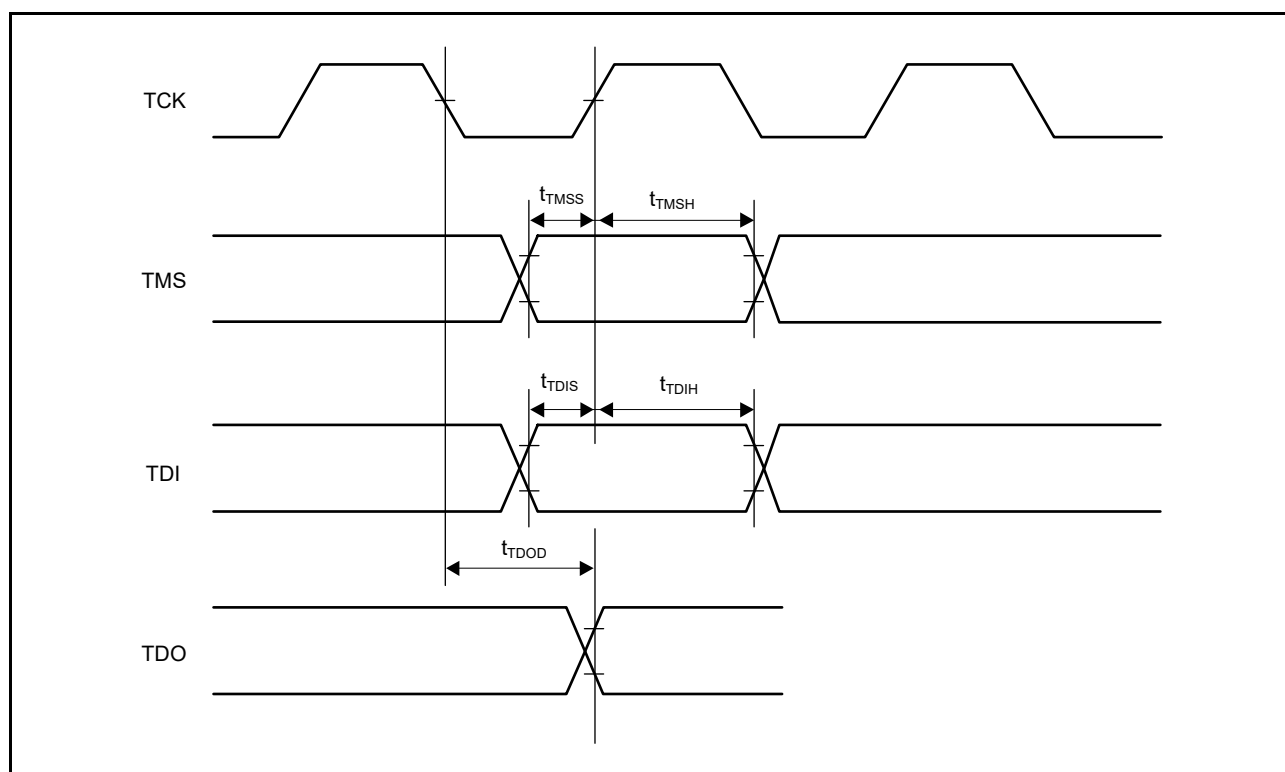
$T_a = T_{opr}$ ,

Output load conditions:  $V_{OH} = 0.5 \times V_{CC}$ ,  $V_{OL} = 0.5 \times V_{CC}$ ,  $C = 30$  pF,

High-drive output is selected by the driving ability control register.

| Item                       | Symbol       | Min. | Typ. | Max. | Unit         | Test Conditions |
|----------------------------|--------------|------|------|------|--------------|-----------------|
| TCK clock cycle time       | $t_{TCKcyc}$ | 100  | —    | —    | ns           | Figure 2.97     |
| TCK clock high pulse width | $t_{TCKH}$   | 45   | —    | —    | ns           |                 |
| TCK clock low pulse width  | $t_{TCKL}$   | 45   | —    | —    | ns           |                 |
| TCK clock rise time        | $t_{TCKr}$   | —    | —    | 5    | ns           |                 |
| TCK clock fall time        | $t_{TCKf}$   | —    | —    | 5    | ns           |                 |
| TRST# pulse width          | $t_{TRSTW}$  | 20   | —    | —    | $t_{TCKcyc}$ | Figure 2.98     |
| TMS setup time             | $t_{TMSS}$   | 20   | —    | —    | ns           | Figure 2.99     |
| TMS hold time              | $t_{TMSH}$   | 20   | —    | —    | ns           |                 |
| TDI setup time             | $t_{TDIS}$   | 20   | —    | —    | ns           |                 |
| TDI hold time              | $t_{TDIH}$   | 20   | —    | —    | ns           |                 |
| TDO data delay time        | $t_{TDOD}$   | —    | —    | 40   | ns           |                 |

**Figure 2.97 Boundary Scan TCK Timing****Figure 2.98 Boundary Scan TRST# Timing**

**Figure 2.99** Boundary Scan Input/Output Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

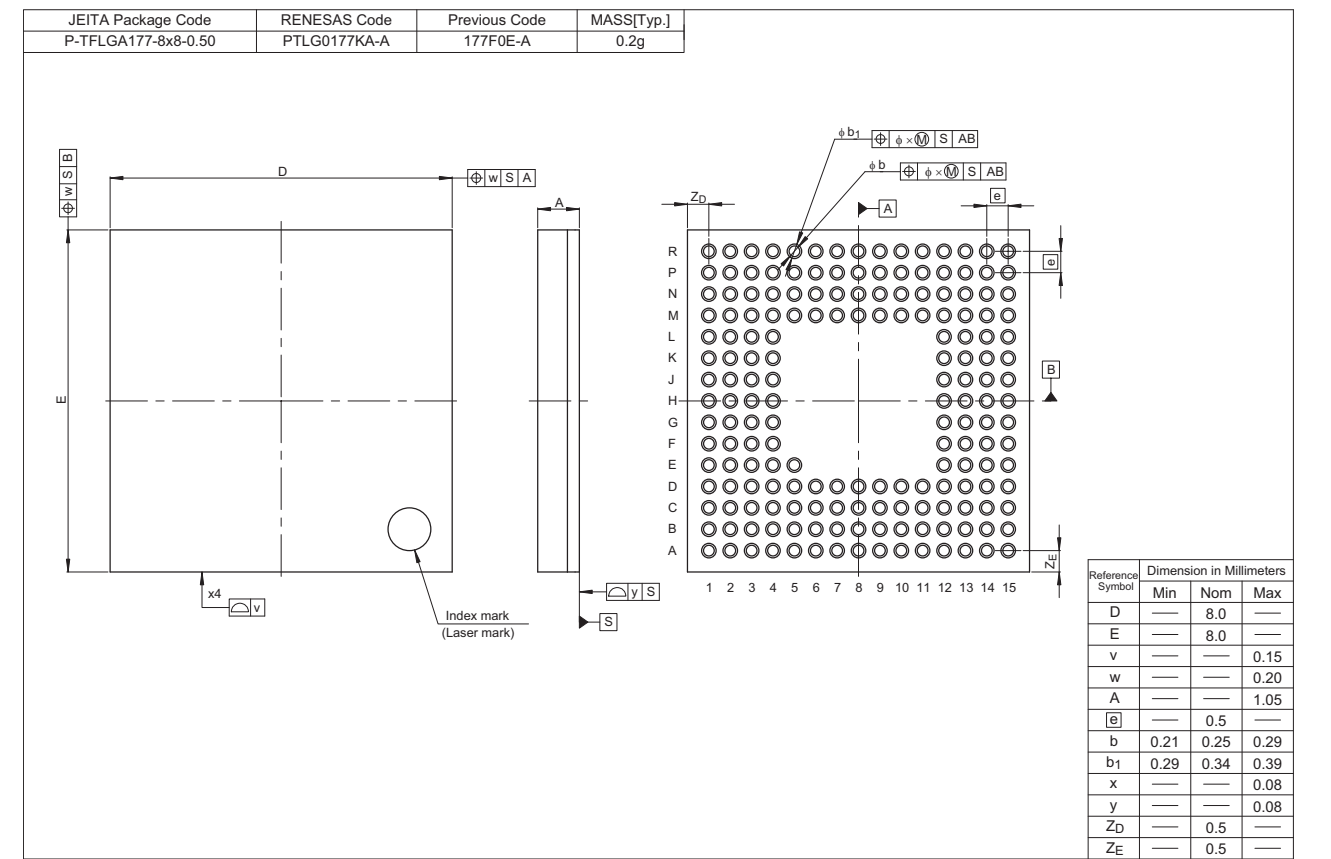


Figure A 177-Pin TFLGA (PTLG0177KA-A)

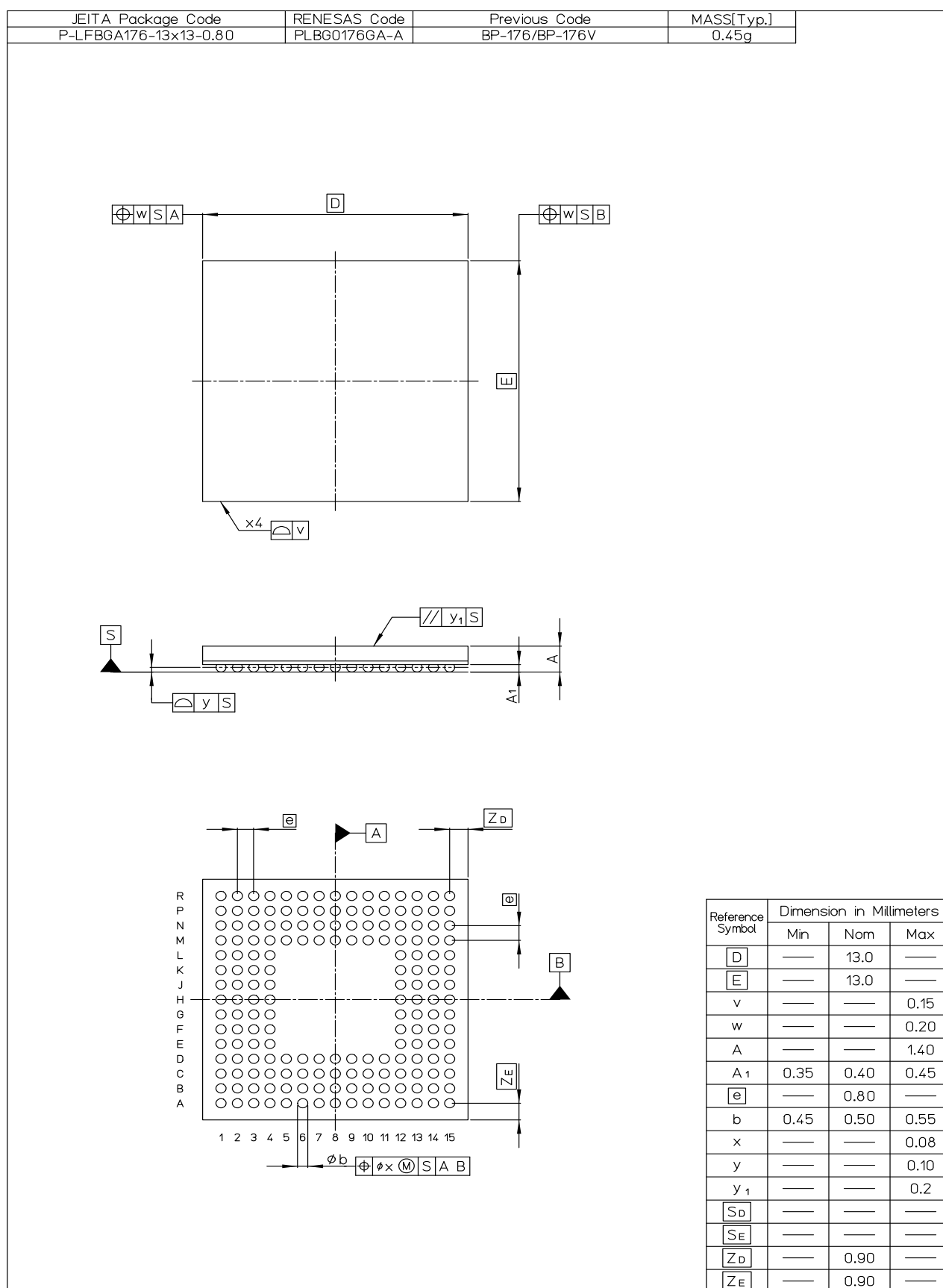


Figure B 176-Pin LFBGA (PLBG0176GA-A)

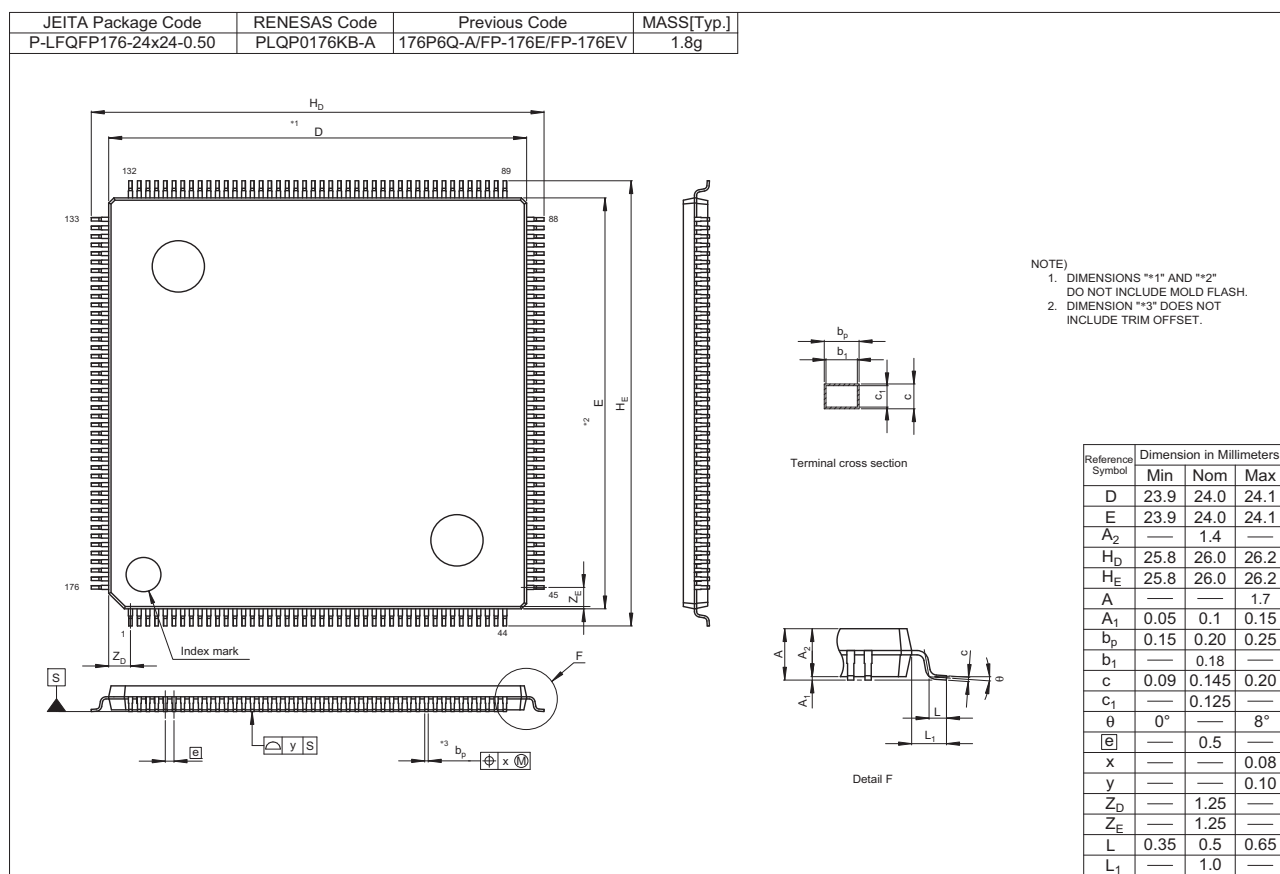


Figure C 176-Pin LFQFP (PLQP0176KB-A)

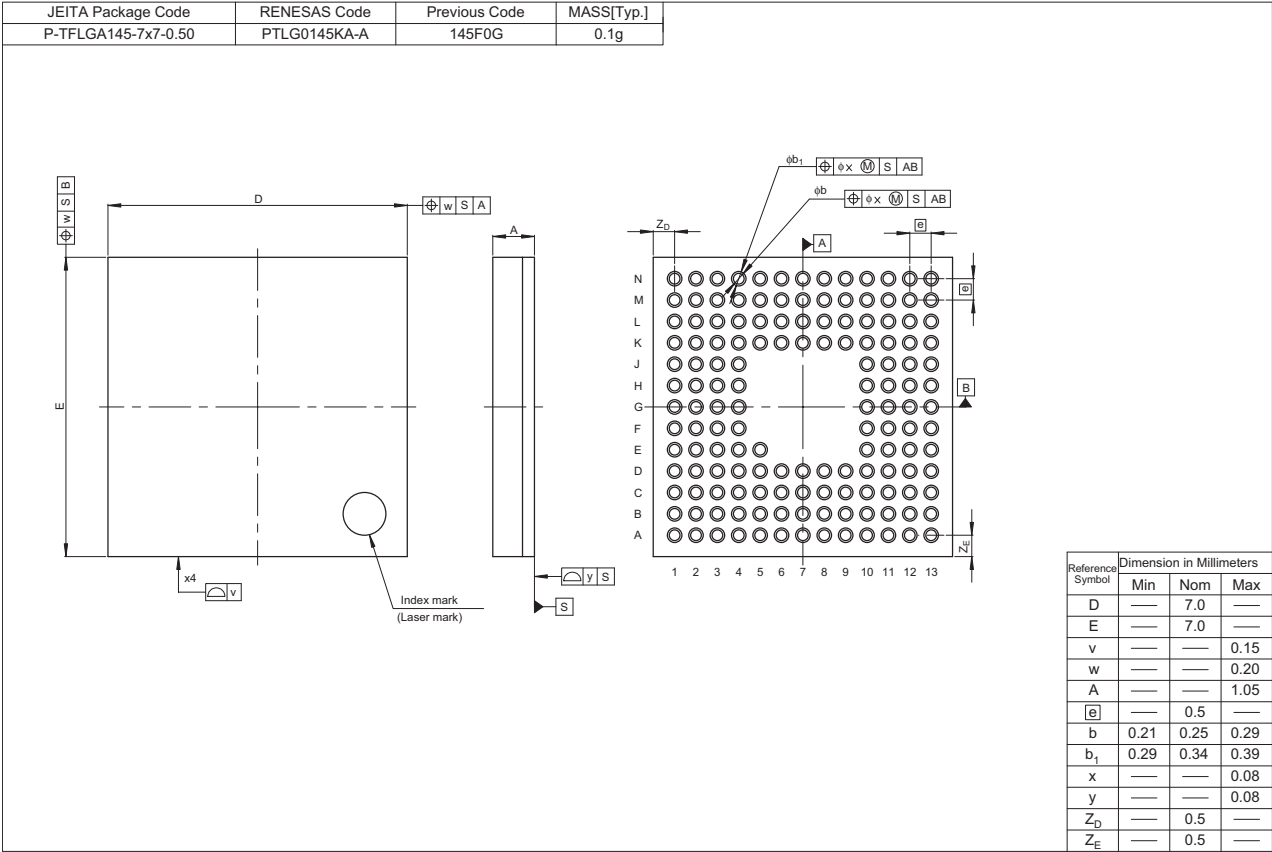
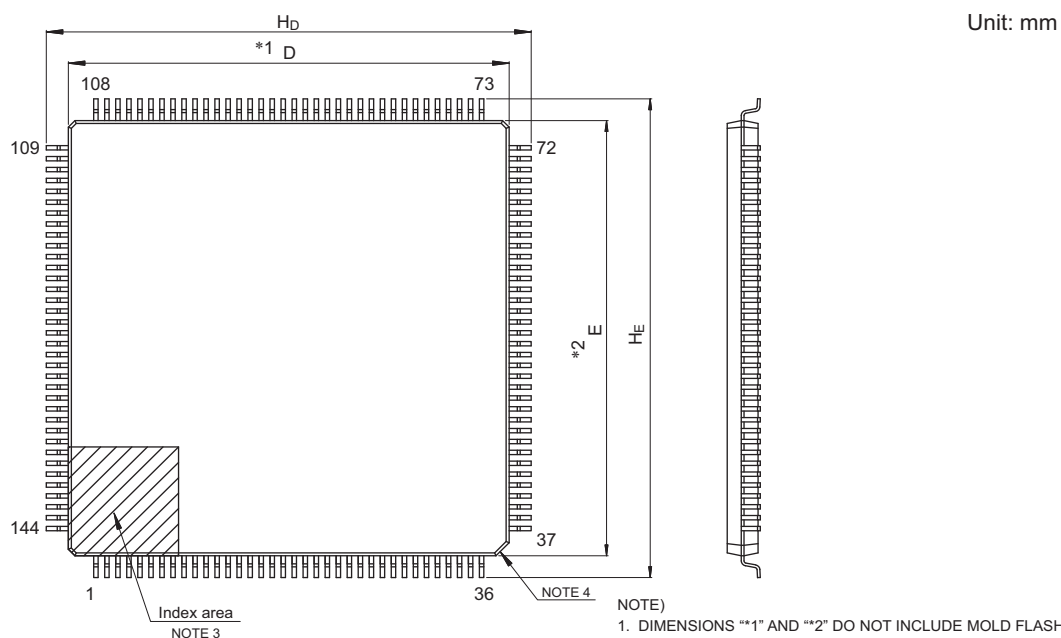


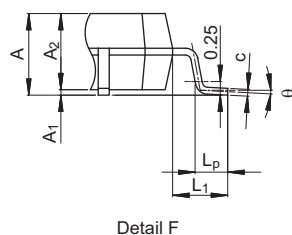
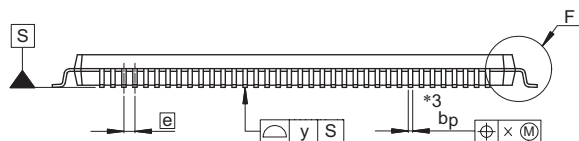
Figure D 145-Pin TFLGA (PTLG0145KA-A)

| JEITA Package Code    | RENESAS Code | Previous Code | MASS (Typ) [g] |
|-----------------------|--------------|---------------|----------------|
| P-LFQFP144-20x20-0.50 | PLQP0144KA-B | —             | 1.2            |



NOTE)

1. DIMENSIONS \*\*\*1" AND \*\*\*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION \*\*\*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL. SIZE MAY VARY.



| Reference Symbol                                                | Dimensions in millimeters |      |      |
|-----------------------------------------------------------------|---------------------------|------|------|
|                                                                 | Min                       | Nom  | Max  |
| D                                                               | 19.9                      | 20.0 | 20.1 |
| E                                                               | 19.9                      | 20.0 | 20.1 |
| A <sub>2</sub>                                                  | —                         | 1.4  | —    |
| H <sub>D</sub>                                                  | 21.8                      | 22.0 | 22.2 |
| H <sub>E</sub>                                                  | 21.8                      | 22.0 | 22.2 |
| A                                                               | —                         | —    | 1.7  |
| A <sub>1</sub>                                                  | 0.05                      | —    | 0.15 |
| b <sub>p</sub>                                                  | 0.17                      | 0.20 | 0.27 |
| c                                                               | 0.09                      | —    | 0.20 |
| θ                                                               | 0°                        | 3.5° | 8°   |
| <span style="border: 1px solid black; padding: 0 2px;">e</span> | —                         | 0.5  | —    |
| x                                                               | —                         | —    | 0.08 |
| y                                                               | —                         | —    | 0.10 |
| L <sub>p</sub>                                                  | 0.45                      | 0.6  | 0.75 |
| L <sub>1</sub>                                                  | —                         | 1.0  | —    |

Figure E 144-Pin LFQFP (PLQP0144KA-B)

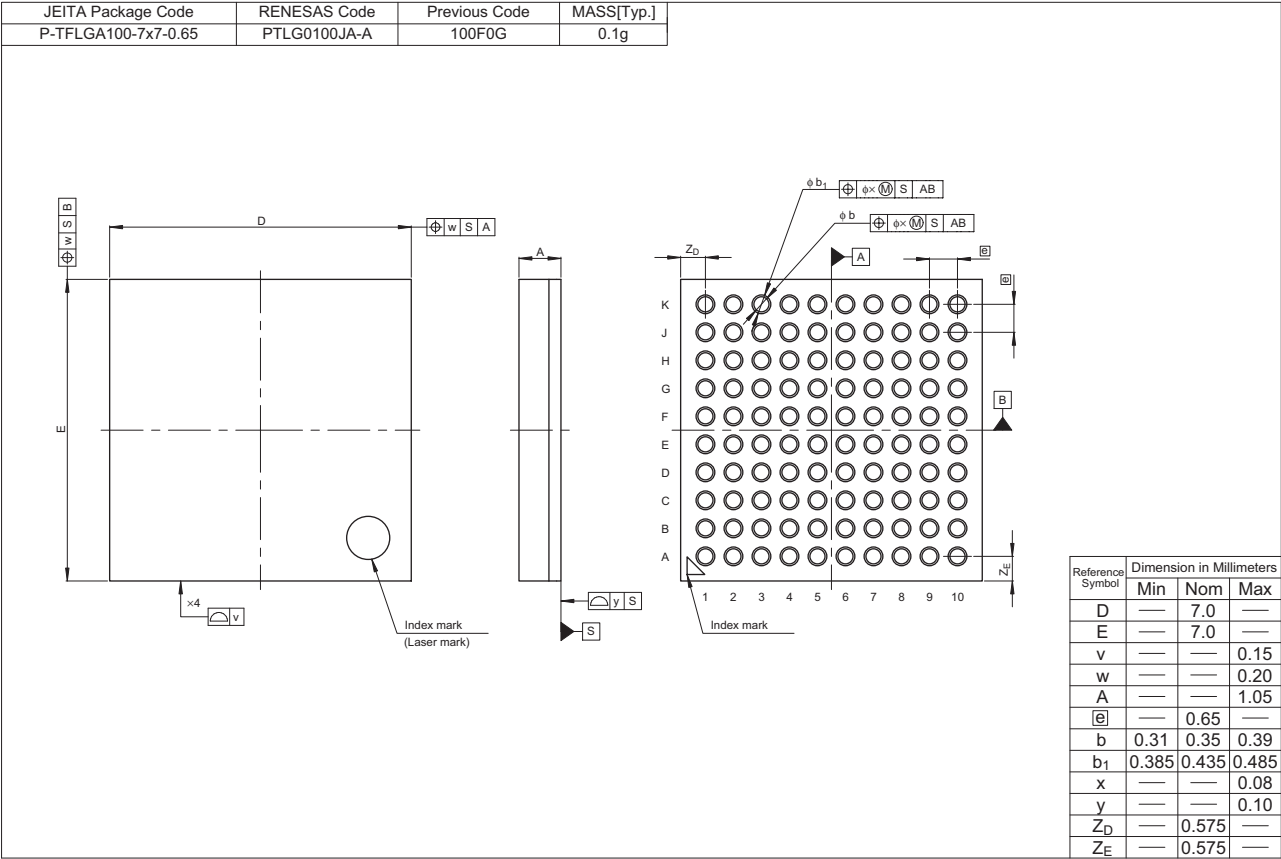
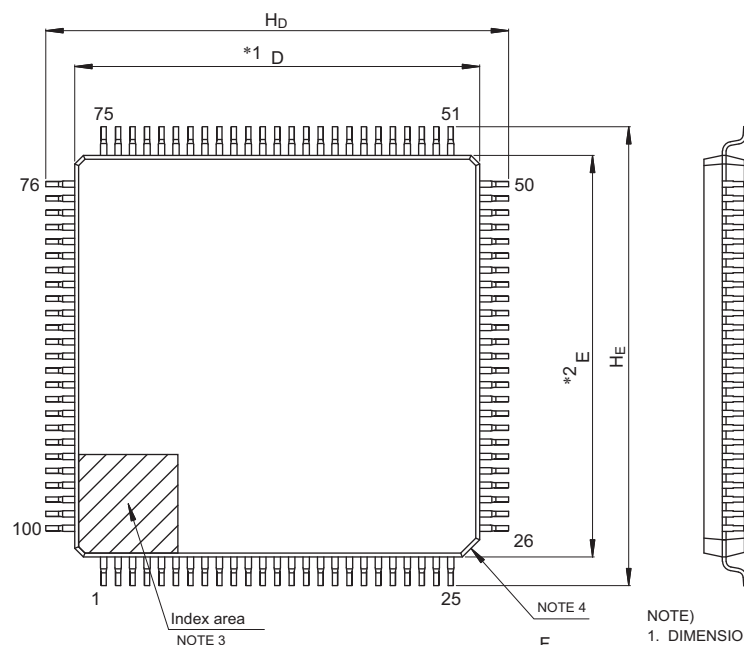


Figure F 100-Pin TFLGA (PTLG0100JA-A)

| JEITA Package Code    | RENESAS Code | Previous Code | MASS (Typ) [g] |
|-----------------------|--------------|---------------|----------------|
| P-LFQFP100-14x14-0.50 | PLQP0100KB-B | —             | 0.6            |



Unit: mm

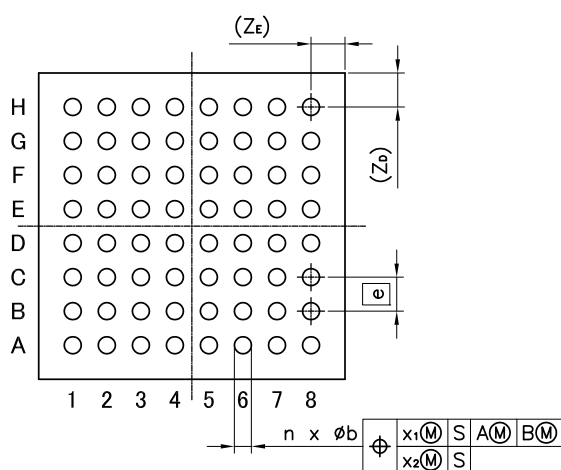
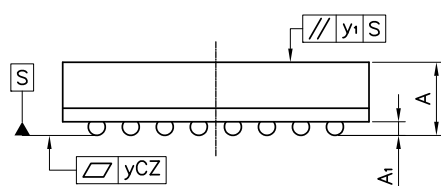
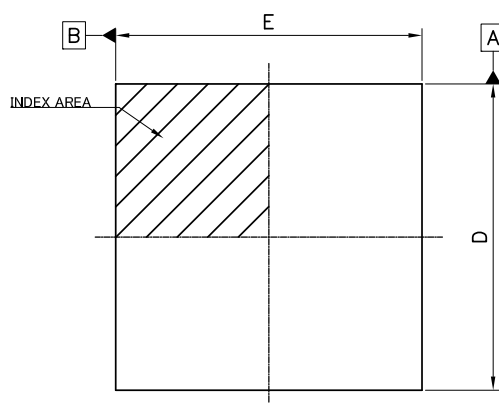
NOTE)

1. DIMENSIONS "1" AND "2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters |      |      |
|------------------|---------------------------|------|------|
|                  | Min                       | Nom  | Max  |
| D                | 13.9                      | 14.0 | 14.1 |
| E                | 13.9                      | 14.0 | 14.1 |
| A <sub>2</sub>   | —                         | 1.4  | —    |
| H <sub>D</sub>   | 15.8                      | 16.0 | 16.2 |
| H <sub>E</sub>   | 15.8                      | 16.0 | 16.2 |
| A                | —                         | —    | 1.7  |
| A <sub>1</sub>   | 0.05                      | —    | 0.15 |
| b <sub>p</sub>   | 0.15                      | 0.20 | 0.27 |
| c                | 0.09                      | —    | 0.20 |
| θ                | 0°                        | 3.5° | 8°   |
| e                | —                         | 0.5  | —    |
| x                | —                         | —    | 0.08 |
| y                | —                         | —    | 0.08 |
| L <sub>p</sub>   | 0.45                      | 0.6  | 0.75 |
| L <sub>1</sub>   | —                         | 1.0  | —    |

Figure G 100-Pin LFQFP (PLQP0100KB-B)

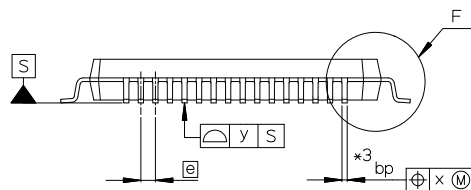
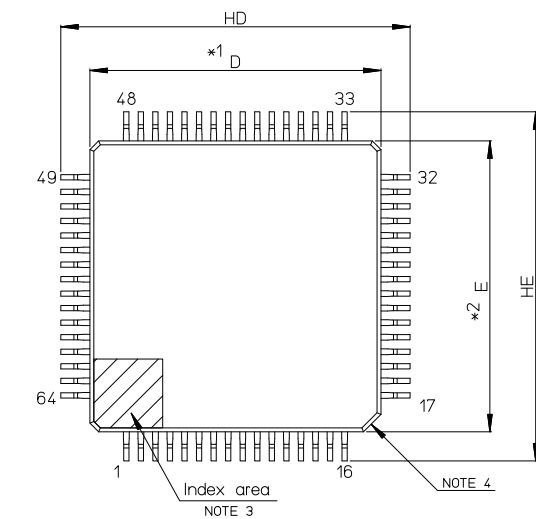
|                          |              |                 |
|--------------------------|--------------|-----------------|
| JEITA Package Code       | RENESAS Code | MASS (Typ.) [g] |
| P-TFBGA64-4.5 × 4.5-0.50 | PTBG0064KB-A | 0.04            |



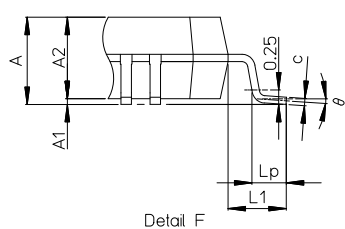
| Reference Symbol | Dimension in Millimeters |      |      |
|------------------|--------------------------|------|------|
|                  | Min.                     | Nom. | Max. |
| D                | 4.42                     | 4.50 | 4.58 |
| E                | 4.42                     | 4.50 | 4.58 |
| A                | —                        | —    | 1.20 |
| A <sub>1</sub>   | 0.15                     | 0.20 | 0.25 |
| e                | —                        | 0.50 | —    |
| b                | 0.20                     | 0.25 | 0.30 |
| x <sub>1</sub>   | —                        | —    | 0.15 |
| x <sub>2</sub>   | —                        | —    | 0.05 |
| y                | —                        | —    | 0.08 |
| y <sub>1</sub>   | —                        | —    | 0.20 |
| n                | —                        | 64   | —    |
| Z <sub>D</sub>   | —                        | 0.50 | —    |
| Z <sub>E</sub>   | —                        | 0.50 | —    |

Figure H 64-Pin TFBGA (PTBG0064KB-A)

| JEITA Package Code   | RENESAS Code | Previous Code | MASS[Typ.] |
|----------------------|--------------|---------------|------------|
| P-LFQFP64-10x10-0.50 | PLQP0064KB-C | —             | 0.3g       |



- NOTE)
1. DIMENSIONS \*1" AND \*2" DO NOT INCLUDE MOLD FLASH.
  2. DIMENSION \*3" DOES NOT INCLUDE TRIM OFFSET.
  3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
  4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.



| Reference Symbol | Dimension in Millimeters |      |      |
|------------------|--------------------------|------|------|
|                  | Min                      | Nom  | Max  |
| D                | 9.9                      | 10.0 | 10.1 |
| E                | 9.9                      | 10.0 | 10.1 |
| A2               | —                        | 1.4  | —    |
| HD               | 11.8                     | 12.0 | 12.2 |
| HE               | 11.8                     | 12.0 | 12.2 |
| A                | —                        | —    | 1.7  |
| A1               | 0.05                     | —    | 0.15 |
| bp               | 0.15                     | 0.20 | 0.27 |
| c                | 0.09                     | —    | 0.20 |
| θ                | 0°                       | 3.5° | 8°   |
| e                | —                        | 0.5  | —    |
| x                | —                        | —    | 0.08 |
| y                | —                        | —    | 0.08 |
| Lp               | 0.45                     | 0.6  | 0.75 |
| L1               | —                        | 1.0  | —    |

Figure I 64-Pin LFQFP (PLQP0064KB-C)

| REVISION HISTORY | RX65N Group, RX651 Group Datasheet |
|------------------|------------------------------------|
|------------------|------------------------------------|

## Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

| Rev. | Date         | Description                   |                                                                                                                                                                         | Classification                   |
|------|--------------|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|
|      |              | Page                          | Summary                                                                                                                                                                 |                                  |
| 1.00 | Aug 24, 2016 | —                             | First edition, issued                                                                                                                                                   |                                  |
| 2.10 | Oct 02, 2017 | —                             | Products with at least 1.5 Mbytes of code flash memory added<br>The conventional products indicated as "products with 1 Mbyte of code flash memory or less"             |                                  |
|      |              | 1. Overview                   |                                                                                                                                                                         |                                  |
|      |              | 6, 9                          | Table 1.1 Outline of Specifications (5/9), Note added                                                                                                                   | TN-RX*-A164B/E                   |
|      |              | 8                             | Table 1.1 Outline of Specifications (8/9)<br>Description of the 12-bit D/A converter (R12DA) changed                                                                    | TN-RX*-A165A/E                   |
|      |              | 4. I/O Registers              |                                                                                                                                                                         |                                  |
|      |              | 131                           | Table 4.1 List of I/O Registers (Address Order) (46 / 61), changed                                                                                                      | TN-RX*-A176A/E                   |
|      |              | 5. Electrical Characteristics |                                                                                                                                                                         |                                  |
|      |              | 147                           | Table 5.1 Absolute Maximum Rating, changed                                                                                                                              |                                  |
|      |              | 150                           | Table 5.5 DC Characteristics (3) (Products with 1 Mbyte of code flash memory or less), changed                                                                          | TN-RX*-A164B/E                   |
|      |              | 152                           | Table 5.7 DC Characteristics (4), changed                                                                                                                               | TN-RX*-A164B/E<br>TN-RX*-A176A/E |
|      |              | 153                           | Table 5.9 Heat Resistance Value (Reference), added                                                                                                                      |                                  |
|      |              | 162                           | Table 5.21 Timing of Recovery from Low Power Consumption Modes (1), changed                                                                                             | TN-RX*-A176A/E                   |
|      |              | 189                           | Table 5.35 RSPI Timing, changed                                                                                                                                         |                                  |
|      |              | 212                           | Table 5.49 D/A Conversion Characteristics, changed                                                                                                                      | TN-RX*-A165A/E                   |
|      |              | 218                           | Table 5.54 Code Flash Memory Characteristics, changed                                                                                                                   |                                  |
|      |              | 219                           | Table 5.55 Data Flash Memory Characteristics, changed                                                                                                                   |                                  |
| 2.30 | Jun 20, 2019 | —                             | 64-pin Package Products added<br>Terms unified:<br>pull-up MOS → pull-up resistors<br>pull-down MOS → pull-down resistors                                               |                                  |
|      |              | 1. Overview                   |                                                                                                                                                                         |                                  |
|      |              | 14 to 22                      | Table 1.3 List of Products, changed                                                                                                                                     | TN-RX*-A204A/E                   |
|      |              | 30                            | Table 1.4 Pin Functions (6/8), changed                                                                                                                                  | TN-RX*-A0211A/E                  |
|      |              | 47 to 49                      | Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA), changed                                                                                         | TN-RX*-A182A/E                   |
|      |              | 52                            | Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP), changed                                                                                                        |                                  |
|      |              | 4. I/O Registers              |                                                                                                                                                                         |                                  |
|      |              | 136 to 138                    | Table 4.1 List of I/O Registers (Address Order), changed                                                                                                                | TN-RX*-A0211A/E                  |
|      |              | 5. Electrical Characteristics |                                                                                                                                                                         |                                  |
|      |              | 157                           | Table 5.5 DC Characteristics (3) (Products with 1 Mbyte of code flash memory or less), changed                                                                          | TN-RX*-A0211A/E                  |
|      |              | 158, 159                      | Table 5.6 DC Characteristics (3) (Products for products with at least 1.5 Mbytes of code flash memory), changed                                                         |                                  |
|      |              | 159                           | Table 5.7 DC Characteristics (4), changed                                                                                                                               |                                  |
|      |              | 161                           | Table 5.9 Thermal Resistance Value (Reference), changed                                                                                                                 | TN-RX*-A182A/E                   |
|      |              | 164                           | Table 5.13 Reset Timing, Unit changed                                                                                                                                   | TN-RX*-A202A/E                   |
|      |              | 206                           | Figure 5.54 IIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing, changed                                                             |                                  |
|      |              | 216                           | Table 5.44 SDHI Timing, added<br>Figure 5.72 SD Host Interface Input/Output Signal Timing, added                                                                        | TN-RX*-A196A/E                   |
|      |              | 217, 218                      | Table 5.45 SDSDI Timing, added<br>Figure 5.73 SD Slave Interface Input Signal Timing to<br>Figure 5.75 SD Slave Interface Output Signal Timing (High Speed Mode), added |                                  |
|      |              | 221                           | Table 5.48 12-Bit A/D (Unit 0) Conversion Characteristics, changed                                                                                                      | TN-RX*-A182A/E                   |

| Rev. | Date         | Description                   |                                                                                                                        | Classification  |
|------|--------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------|-----------------|
|      |              | Page                          | Summary                                                                                                                |                 |
| 2.30 | Jun 20, 2019 | 230                           | Table 5.57 Data Flash Memory Characteristics, changed (64-bytes and 2-Kbytes blank check time added)                   |                 |
| 2.40 | Oct 31, 2023 | 1. Overview                   |                                                                                                                        |                 |
|      |              | 11                            | Table 1.1 Outline of Specifications (10/10), changed                                                                   | TN-RX*-A0250A/E |
|      |              | 14 to 25                      | Table 1.3 List of Products, changed                                                                                    | TN-RX*-A0233A/E |
|      |              | 2. Electrical Characteristics |                                                                                                                        |                 |
|      |              | 90                            | Table 2.2 Recommended Operating Conditions (1), changed                                                                | TN-RX*-A0250A/E |
|      |              | 90                            | Table 2.3 Recommended Operating Conditions (2), added                                                                  | TN-RX*-A0272A/E |
|      |              | 91                            | Table 2.4 DC Characteristics (1) Note 3, changed                                                                       | TN-RX*-A0250A/E |
|      |              | 92                            | Table 2.5 DC Characteristics (2), changed                                                                              |                 |
|      |              | 93, 94                        | Table 2.6 DC Characteristics (3) (Products with 1 Mbyte of code flash memory or less), changed                         | TN-RX*-A0250A/E |
|      |              | 94, 95                        | Table 2.7 DC Characteristics (3) (Products for products with at least 1.5 Mbytes of code flash memory) Note 3, changed | TN-RX*-A0250A/E |
|      |              | 105                           | Table 2.21 Sub-Clock Timing, changed                                                                                   | TN-RX*-A0250A/E |
|      |              | 170                           | Table 2.56 Battery Backup Function Characteristics, changed                                                            | TN-RX*-A0250A/E |
|      |              | 171                           | Table 2.57 Code Flash Memory Characteristics, changed                                                                  | TN-RX*-A0248A/E |
|      |              | 172                           | Table 2.58 Data Flash Memory Characteristics, changed                                                                  | TN-RX*-A0248A/E |

## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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