650V 38mΩ SolidGaN with DESAT Protection

1. Features

- 38mΩ E-Mode GaN with Integrated Gate Clamp
- 650V Continuous, 800V Transient Voltage Rating
- Wide 10V to 24V Gate Input Voltage Range
- Adjustable Turn-On and Turn-Off Slew Rate by External Gate Resistors
- Accurate LDO-Based Integrated Gate Clamp to Protect GaN Device
- Integrated Miller Clamp for dv/dt-Induced Shoot-Through Protection: dv/dt Immunity up to 200V/ns
- Paralleling Capability
- Zero Reverse Recovery Charge
- High Frequency Operation up to 2MHz
- Built-In DESAT, Input UVLO, and OTP Protection
- Available in TOLL-4L Package

2. Applications

- High-Power Switch-Mode Power Supplies
- AC-DC, DC-DC, DC-AC Converters
- Half-Bridge and Full-Bridge Converters
- TV Power, Air Conditioner Power
- Solar Micro Inverter, Motor Drive, OBC

3. Description

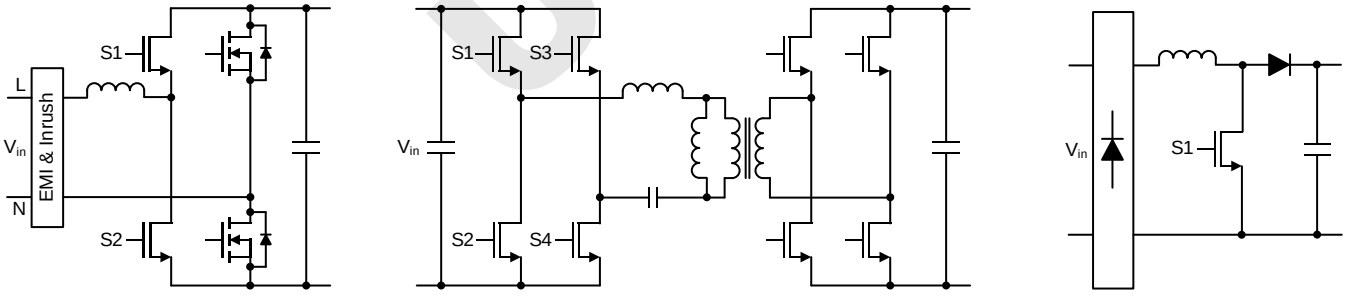
The ISG6123 SolidGaN IC seamlessly integrates a 650V E-Mode GaN FET with advanced features, setting a new standard for performance, easy-of-use, and reliability in power electronics. The integrated gate clamp, driven by an accurate LDO-based circuitry, maintains a tightly regulated driving voltage for the GaN FET within a flexible gate-input voltage range of 10V to 24V, ensuring full protection of the GaN power transistor against excessive voltage stress while maximizing GaN performance.

Equipped with built-in protections including DESAT protection, Input UVLO, and OTP, the ISG6123 further ensures device robustness and system safety. The integrated miller clamp prevents false turn-ons caused by the high dv/dt slope of the drain voltage.

The ISG6123 offers users the ability to adjust the turn-on and turn-off slew rate of the GaN FET using external gate resistors. This feature optimizes both electromagnetic interference (EMI) and switching loss.

The ISG6123's high integration level with a GaN FET and robust protections, makes it suitable for a range of applications, from simple setups with low component counts to high-frequency and high-power applications.

4. Typical Application



Totem Pole PFC　　LLC or CLLC　　Boost PFC

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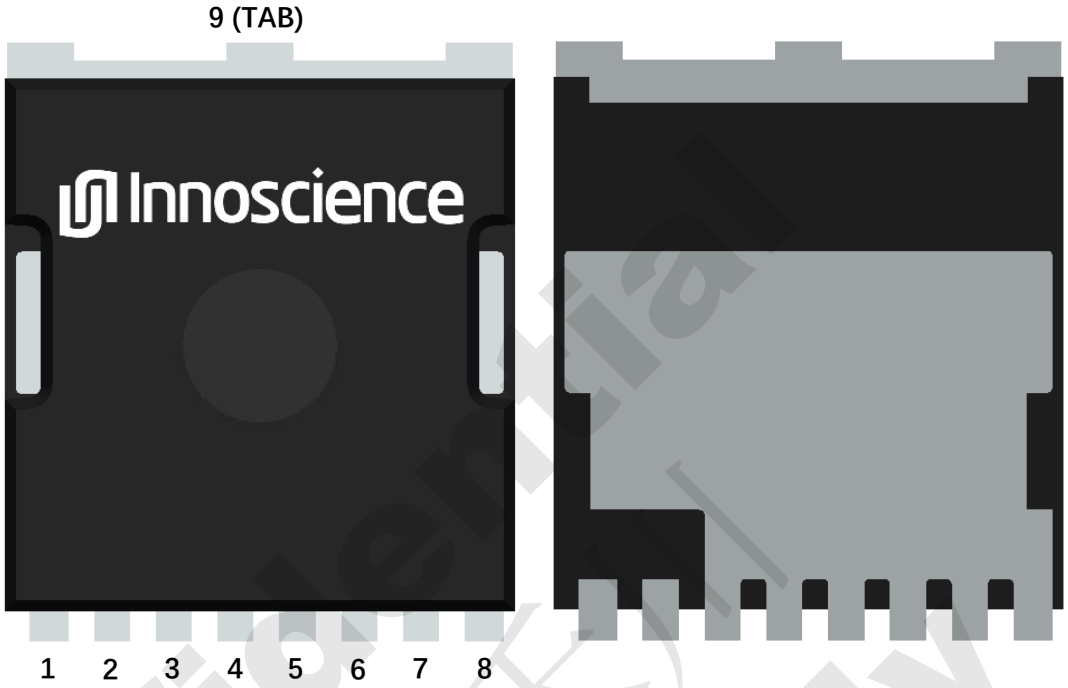
5. Revision history

Major changes since the last revision

Revision	Date	Description of changes
0.1	2024-01-08	Preliminary datasheet

6. Pin Configuration and Functions



4-Lead TOLL Package – Top and Bottom View

Pin Number	Pin Name	Description
9 (TAB)	D	Drain of Power GaN FET.
1-6	S	Source of Power GaN FET.
7	K	Kelvin Source.
8	G	Gate Input. Connect to the drive output of controller or gate driver.

7. Absolute Maximum Ratings

All pins are referred to S pins, unless otherwise specified. Stress beyond the absolute maximum ratings can cause permanent damage or deteriorate device lifetime.

Parameter	Min	Max	Unit
Drain Voltage, Continuous	-7	650	V
Drain Voltage, Transient (1)		800	V
Drain Voltage, Pulsed (2)		750	V
Drain Current, Continuous (T_C = 25°C)		32	A
Drain Current, Continuous (T_C = 125°C)		21	A
Drain Current, Pulsed (10us @ T_C = 25°C)		58	A
Drain Current, Pulsed (10us @ T_C = 125°C)		29	A
Gate Input Voltage	-0.3	27	V
Drain-to-Source Slew Rate – dV/dt		200	V/ns
Operating Junction Temperature T_J	-55	150	˚C
Storage Temperature	-55	150	˚C

(1) $V_{DS(TRAN)}$ is intended for non-repetitive events, t_{PULSE} < 200us.

(2) $V_{DS(PULS)}$ is intended for repetitive events, t_{PULSE} < 100ns.

8. ESD Ratings

T_J = 25°C unless otherwise specified.

Parameter	Value	Unit
Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
Charged Device Model (CDM), per ANSI/ESDA/JEDEC JS-002	±1000	V

9. Recommended Operating Conditions

Parameter	Min	Max	Unit
Drain Voltage	-5	520	V
Gate Input High Voltage	10	24	V
Gate Input Low Voltage	-0.3	0.3	V

10. Thermal Information

Symbol	Parameter	ISG6123TA	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	40	˚C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.3	˚C/W

11. Electrical Characteristics

T_J = 25°C, V_{GS} = 15V, V_{DS} = 400V, I_{DS} = 30A, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Gate Characteristics						
Gate input threshold voltage	$V_{G(TH)}$		4		V	Gate Rising
Gate quiescent current	I_{G_Q}		1800		uA	V_{GS} = 15V, V_{DS} = 0V
Gate turn-on peak current (3)	I_{GON_PK}		1.4		A	V_{GS} = 15V
Miller clamp pull-down Resistance (3)	R_{GOFF_MC}		0.5		Ω	V_{GS} = 0V
Protection						
DESAT protection threshold (3)	V_{D_DESAT}		7.3		V	
DESAT blanking time	t_{BLK_DESAT}		300		ns	
Gate UVLO threshold	V_{G_UVLO}		8.5		V	
Over temperature threshold (3)	T_{OTP}		160		°C	
Over temperature hysteresis (3)	T_{HYS}		20		°C	
Power GaN FET						
Drain-source leakage current	I_{DSS}		8	102	uA	V_{DS} = 650V, V_{GS} = 0V
Drain-source resistance	$R_{DS(ON)}$		38	49	mΩ	V_{GS} = 15V, I_{DS} = 21A
Source-drain reverse voltage	V_{SD}		4		V	V_{GS} = 0V, I_{SD} = 21A
Output charge (3)	Q_{OSS}		TBA		nC	V_{DS} = 400V, V_{GS} = 0V
Reverse recovery charge (3)	Q_{RR}		0		nC	
Output capacitance (3)	C_{OSS}		110		pF	V_{DS} = 400V, V_{GS} = 0V
Effective output capacitance, energy related (3)	$C_{O(er)}$		165		pF	V_{DS} = 400V, V_{GS} = 0V
Effective output capacitance, time related (3)	$C_{O(tr)}$		236		pF	V_{DS} = 400V, V_{GS} = 0V

12. Switching Characteristics

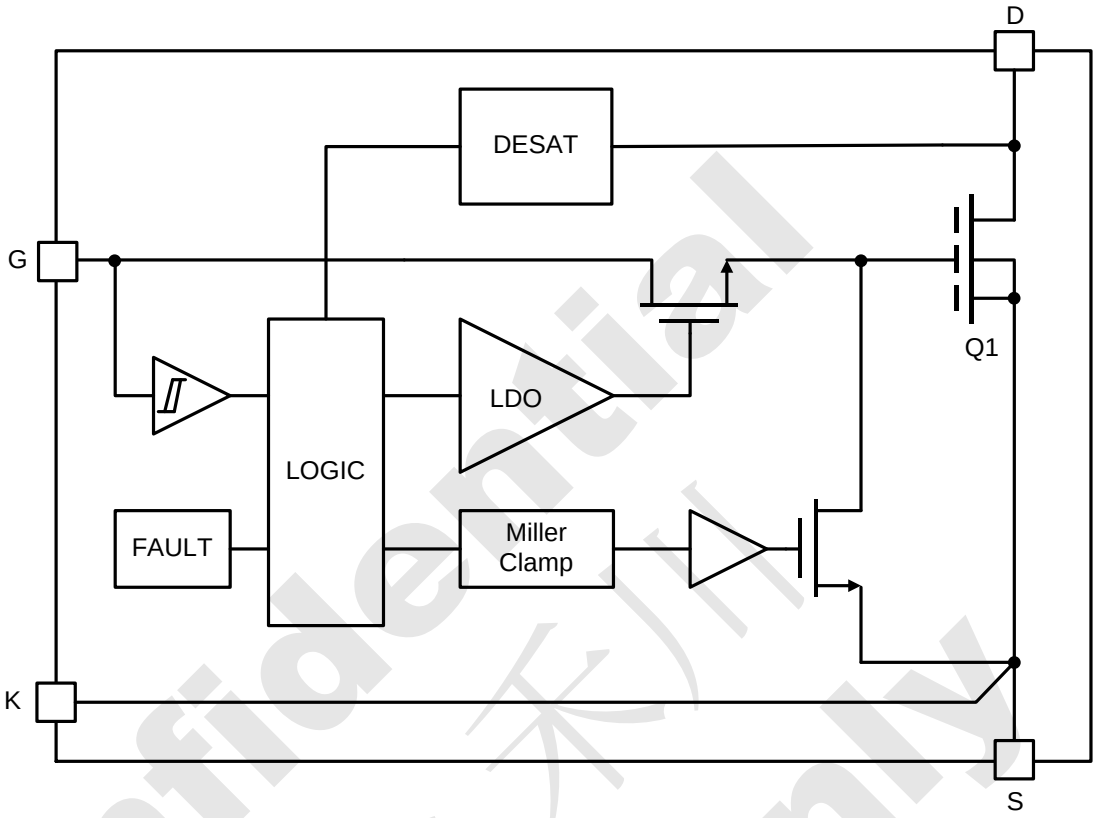
T_J = 25°C, V_{GS} = 15V, V_{DS} = 400V, I_{DS} = 30A, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Minimum input pulse width that changes the output (3)	t_{GH_PW}		10		ns	
Turn-on propagation delay (3)	t_{ON_PD}		25		ns	
Turn-off propagation delay (3)	t_{OFF_PD}		15		ns	
Minimum on time (3)			40		ns	

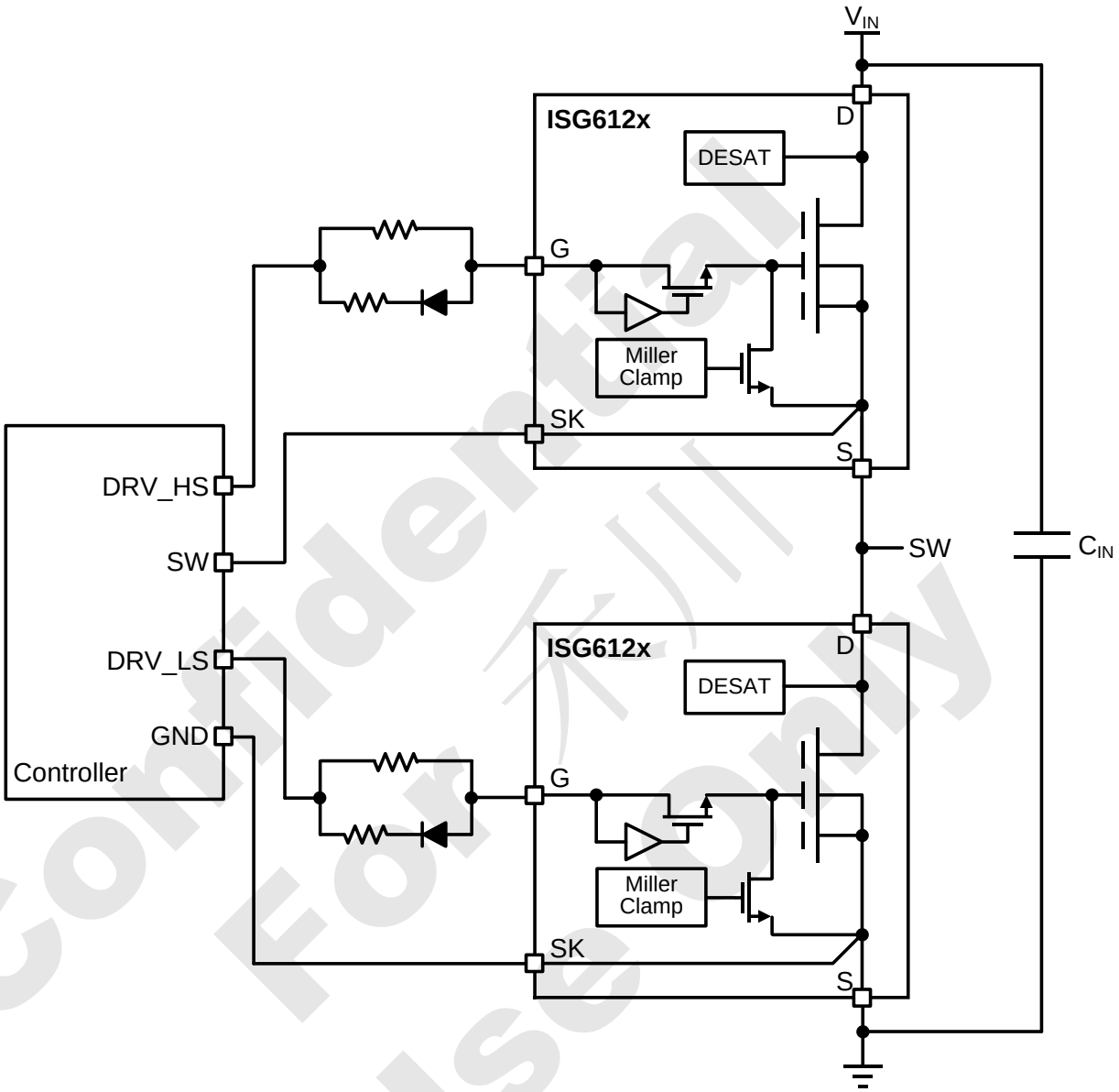
(3) Not 100% tested and guaranteed by design.

13. Typical Characteristics

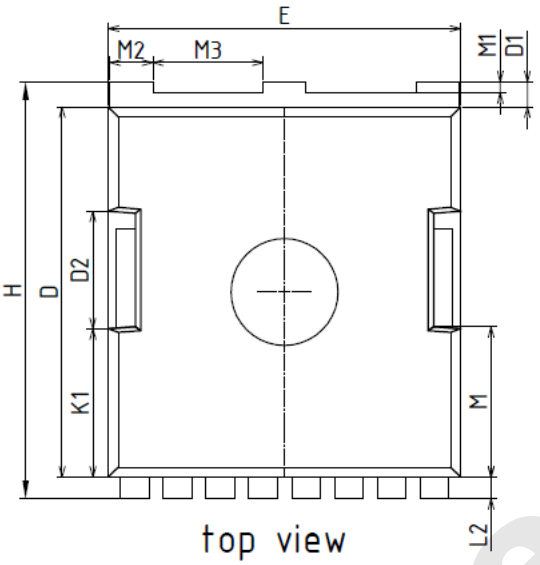
14. Block Diagram

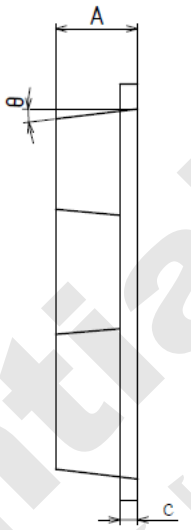


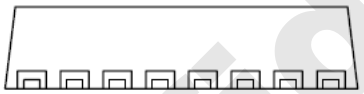
15. Function Description

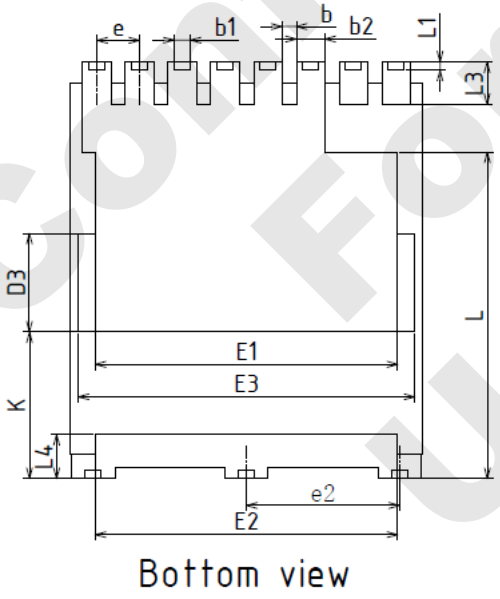


16. Package Information









SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.15	2.30	2.45
b	0.30	0.40	0.50
b1	0.31	0.43	0.55
b2	0.65	0.80	0.90
c	0.40	0.50	0.60
D	10.18	10.38	10.58
D1	0.50	0.70	0.90
D2	3.30REF		
D3	2.77REF		
E	9.70	9.90	10.10
E1	8.50REF		
E2	8.50REF		
E3	9.46REF		
e	1.10	1.20	1.30
H	11.48	11.68	11.88
K	4.08REF		
K1	4.18REF		
L	9.13REF		
L1	0.23REF		
L2	0.50	0.60	0.70
L3	1.00	1.20	1.40
L4	1.00	1.20	1.40
M	4.18REF		
M1	0.26REF		
M2	1.10	1.20	1.30
M3	3.10REF		
Θ	10.00REF		
e2	4.20	4.30	4.40

17. Tape and Reel Information

TBA

18. Recommended Land Pattern

TBA

19. Order Information

Ordering Code	Package	Product Code	MSL	Packing (Tape & Reel)
ISG6123TA	TOLL-4L	6123TA	TBD	13” 2500PCS/reel

Important Notice

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