

RJF0619JPD

60V, 30A Silicon N Channel Thermal FET
Power Switching

R07DS1108EJ0100
Rev.1.00
Sep. 02, 2013

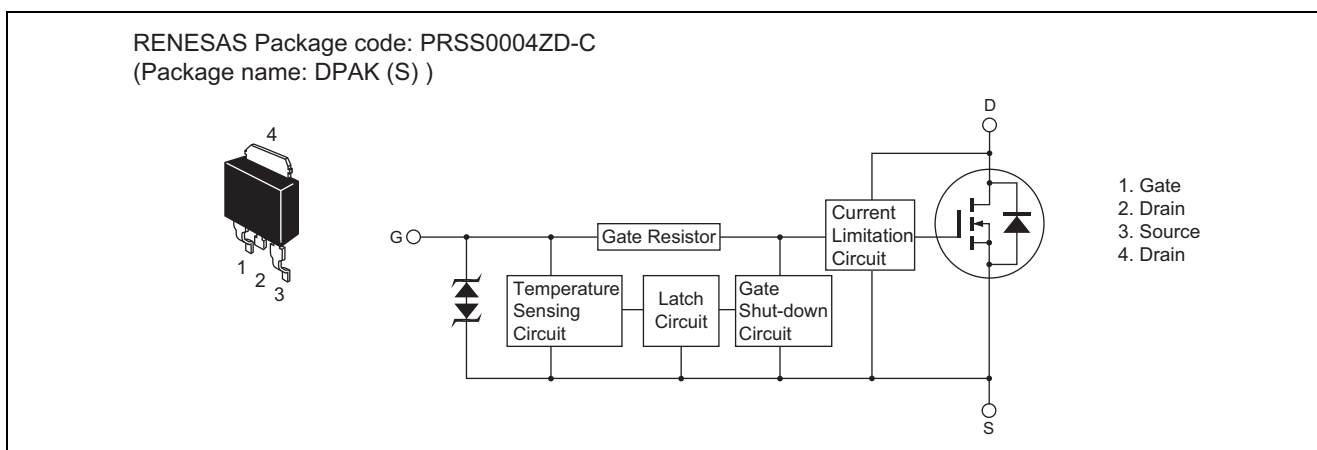
Description

This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features

- Logic level operation (4 V Gate drive).
- Built-in the over temperature shut-down circuit.
- High endurance capability against to the short circuit.
- Latch type shut down operation (need 0 voltage recovery).
- Built-in the current limitation circuit.
- Power supply voltage applies 12 V and 24 V.
- AEC-Q101 Compliant
- Endurance capability against to ESD.

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	16	V
Gate to source voltage	V_{GSS}	-2.5	V
Drain current	I_D ^{Note 3}	30	A
Body-drain diode reverse drain current	I_{DR} ^{Note 2}	30	A
Avalanche current	I_{AP} ^{Note 2}	6.7	A
Avalanche energy	E_{AR} ^{Note 2}	192	mJ
Channel dissipation	P_{ch} ^{Note 1}	40	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. Value at $T_c = 25^\circ\text{C}$
 2. $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
 3. It provides by the current limitation lower bound value.

Typical Operation Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	3.5	—	—	V	
	V _{IL}	—	—	1.2	V	
Input current (Gate non shut down)	I _{IH1}	—	—	100	μA	V _i = 8 V, V _{DS} = 0
	I _{IH2}	—	—	50	μA	V _i = 3.5 V, V _{DS} = 0
	I _{IL}	—	—	1	μA	V _i = 1.2 V, V _{DS} = 0
Input current (Gate shut down)	I _{IH(sD)1}	—	0.8	—	mA	V _i = 8 V, V _{DS} = 0
	I _{IH(sD)2}	—	0.35	—	mA	V _i = 3.5 V, V _{DS} = 0
Shut down temperature	T _{sd}	—	175	—	°C	Channel temperature
Gate operation voltage	V _{op}	3.5	—	12	V	
Drain current (Current limitation value)	I _{D limit}	30	—	—	A	V _{GS} = 5 V, V _{DS} = 10 V ^{Note 4}

Note; 4. Pulse test

Electrical Characteristics

(Ta = 25°C)

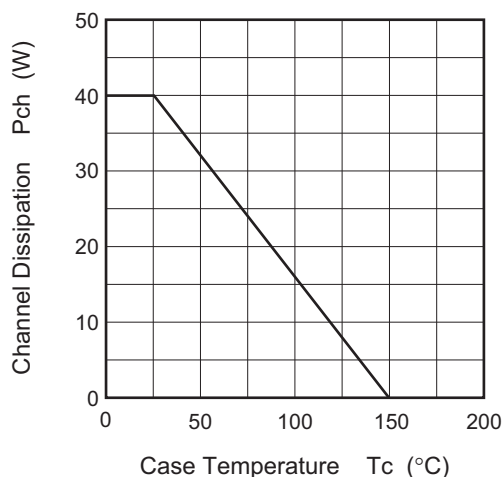
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I _{D1}	—	—	45	A	V _{GS} = 3.5 V, V _{DS} = 10 V ^{Note 5}
	I _{D2}	—	—	10	mA	V _{GS} = 1.2 V, V _{DS} = 10 V
	I _{D3}	30	—	—	A	V _{GS} = 5 V, V _{DS} = 10 V ^{Note 5}
Drain to source breakdown voltage	V _{(BR)DSS}	60	—	—	V	I _D = 10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	16	—	—	V	I _G = 800 μA, V _{DS} = 0
	V _{(BR)GSS}	-2.5	—	—	V	I _G = -100 μA, V _{DS} = 0
Gate to source leak current	I _{GSS1}	—	—	100	μA	V _{GS} = 8 V, V _{DS} = 0
	I _{GSS2}	—	—	50	μA	V _{GS} = 3.5 V, V _{DS} = 0
	I _{GSS3}	—	—	1	μA	V _{GS} = 1.2 V, V _{DS} = 0
	I _{GSS4}	—	—	-100	μA	V _{GS} = -2.4 V, V _{DS} = 0
Input current (shut down)	I _{GS(OP)1}	—	0.8	—	mA	V _{GS} = 8 V, V _{DS} = 0
	I _{GS(OP)2}	—	0.35	—	mA	V _{GS} = 3.5 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	10	μA	V _{DS} = 32 V, V _{GS} = 0, T _c = 110°C
Gate to source cutoff voltage	V _{GS(off)}	1.1	—	2.1	V	V _{DS} = 10 V, I _D = 1 mA
Forward transfer admittance	y _{fs}	12	27	—	S	I _D = 15 A, V _{DS} = 10 V ^{Note 5}
Static drain to source on state resistance	R _{DS(on)}	—	33	40	mΩ	I _D = 15 A, V _{GS} = 4 V ^{Note 5}
	R _{DS(on)}	—	25	30	mΩ	I _D = 15 A, V _{GS} = 10 V ^{Note 5}
Output capacitance	C _{oss}	—	523	—	pF	V _{DS} = 10 V, V _{GS} = 0, f = 1MHz
Turn-on delay time	t _{d(on)}	—	3.8	—	μs	V _{GS} = 10 V, I _D = 15 A, R _L = 2 Ω
Rise time	t _r	—	13.5	—	μs	
Turn-off delay time	t _{d(off)}	—	4.1	—	μs	
Fall time	t _f	—	7.3	—	μs	
Body-drain diode forward voltage	V _{DF}	—	0.9	—	V	I _F = 30 A, V _{GS} = 0
Body-drain diode reverse recovery time	t _{rr}	—	110	—	ns	I _F = 30 A, V _{GS} = 0 di/dt = 50 A/μs
Over load shut down operation time ^{Note 6}	t _{os1}	—	0.34	—	ms	V _{GS} = 5 V, V _{DD} = 16 V
	t _{os2}	—	0.23	—	ms	V _{GS} = 5 V, V _{DD} = 24 V

Notes: 5. Pulse test

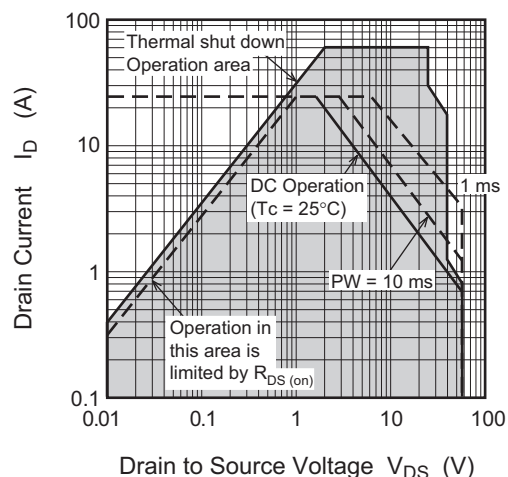
6. Including the junction temperature rise of the over loaded condition.

Main Characteristics

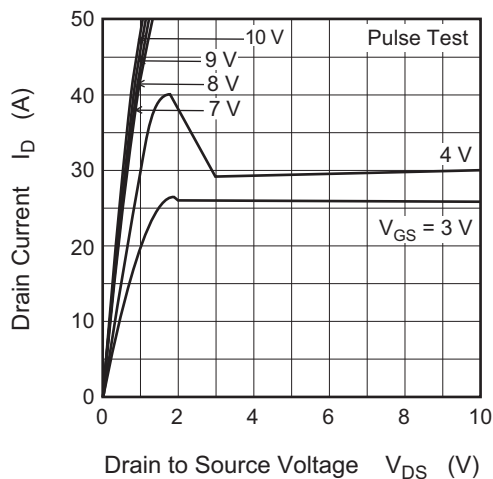
Power vs. Temperature Derating



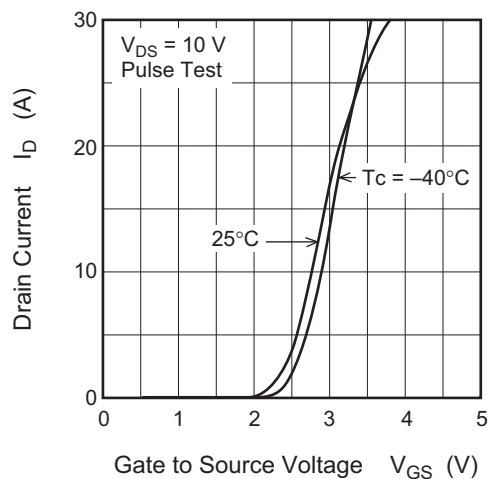
Maximum Safe Operation Area



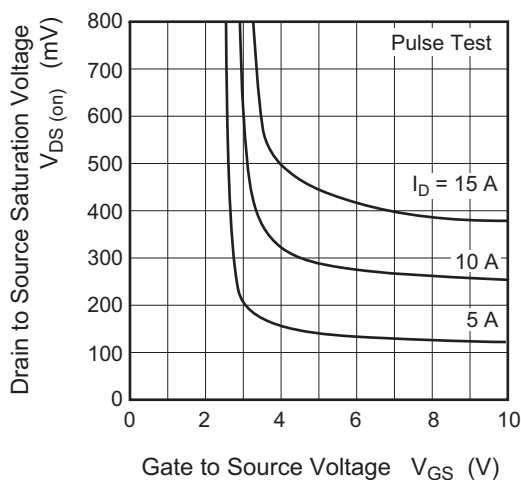
Typical Output Characteristics



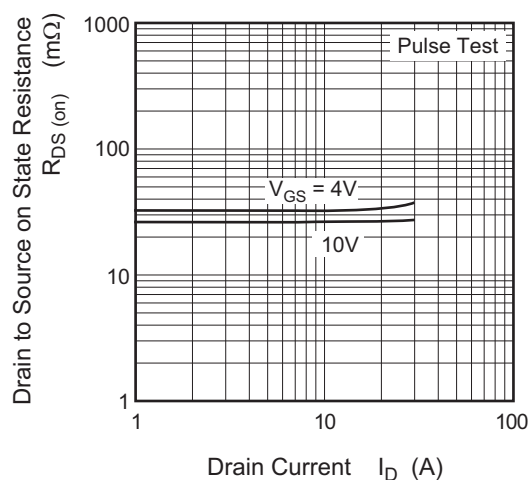
Typical Transfer Characteristics

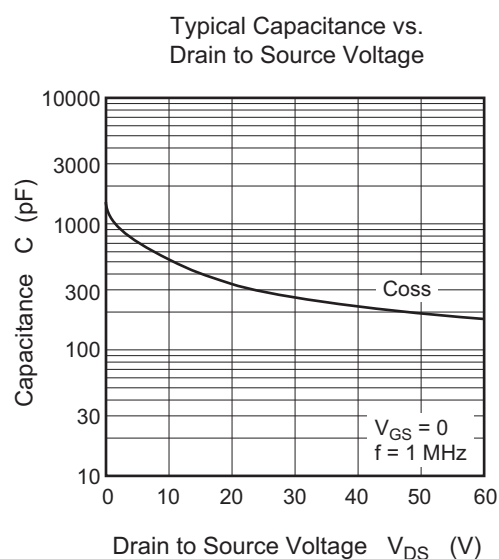
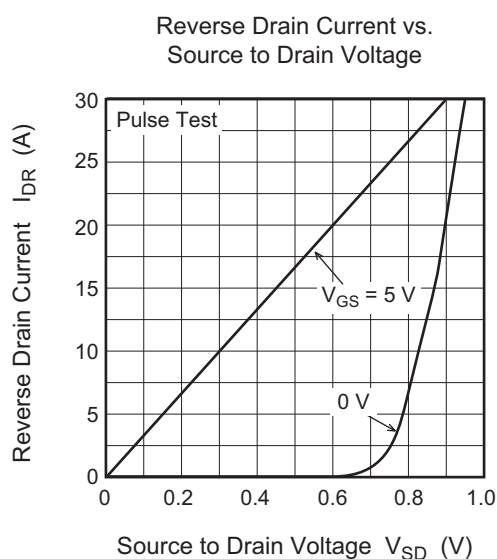
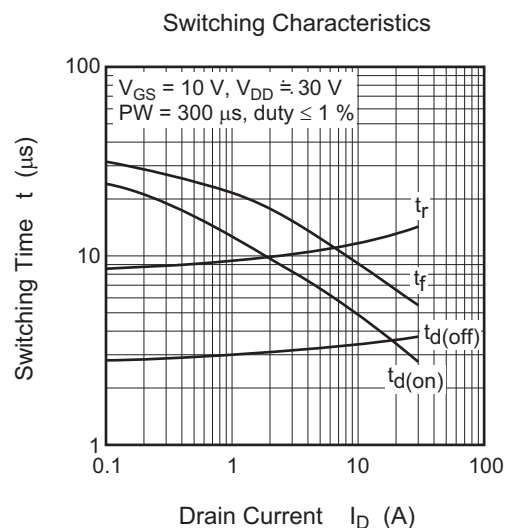
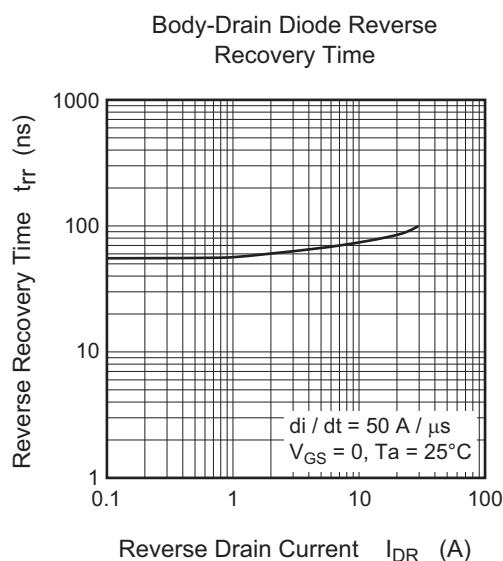
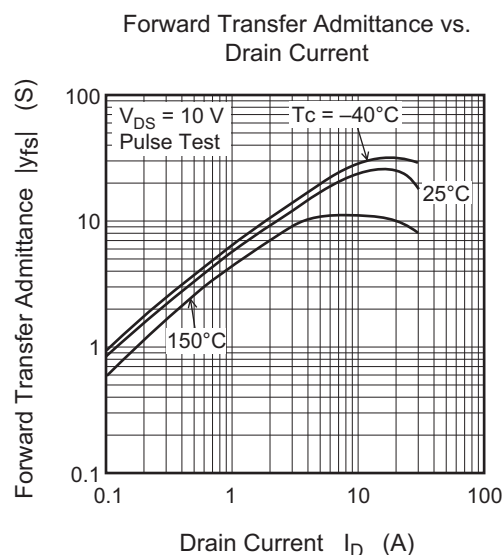
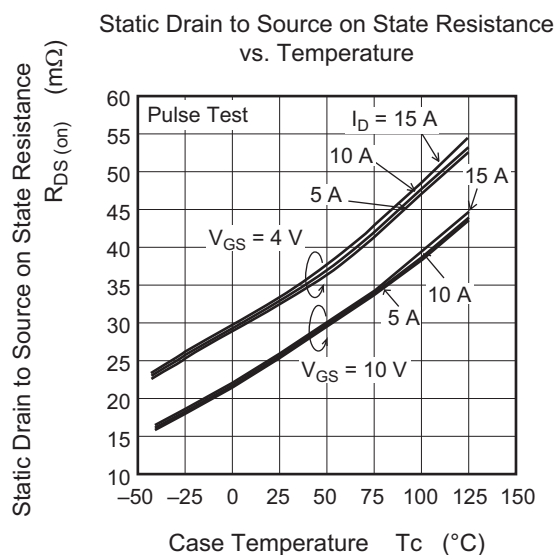


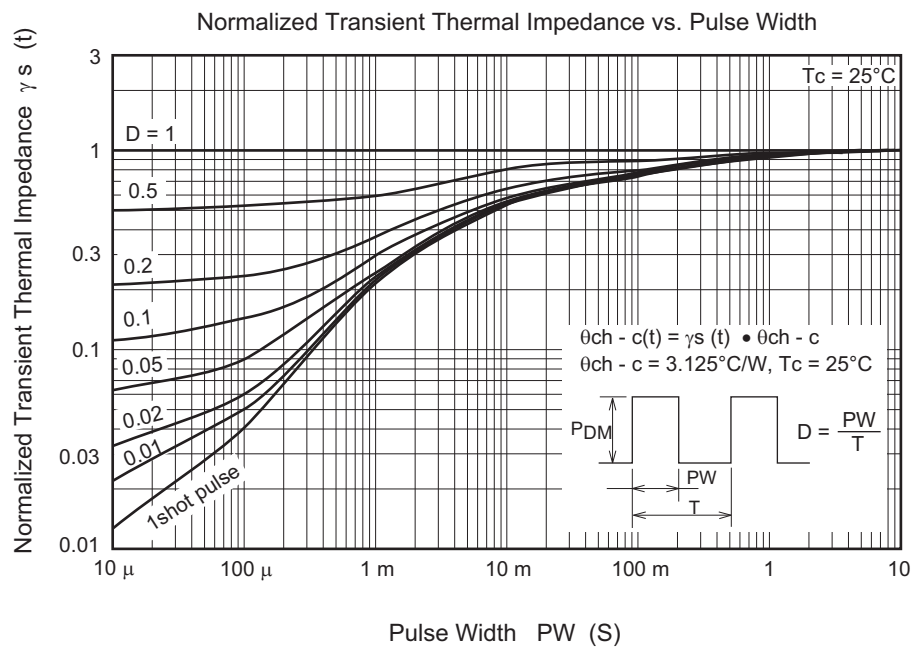
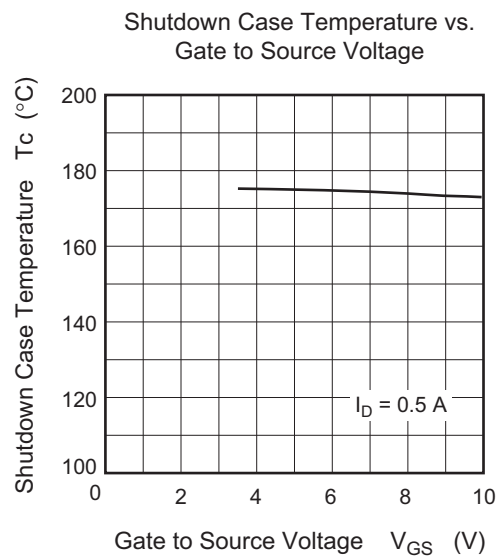
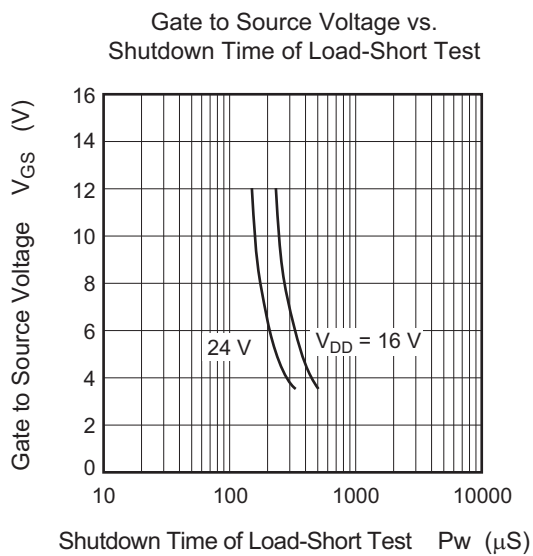
Drain to Source Saturation Voltage vs. Gate to Source Voltage



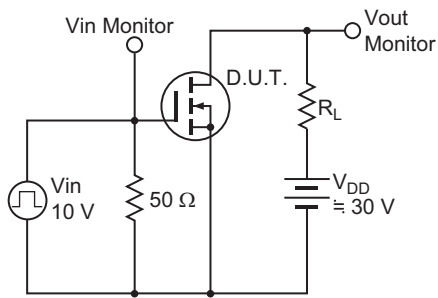
Static Drain to Source on State Resistance vs. Drain Current



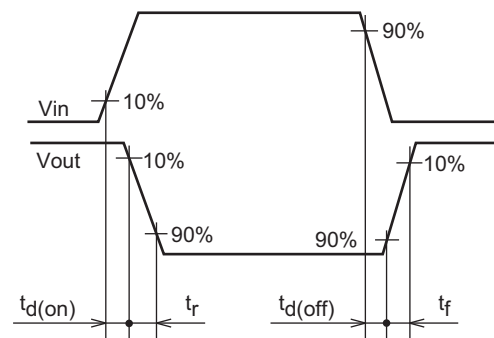




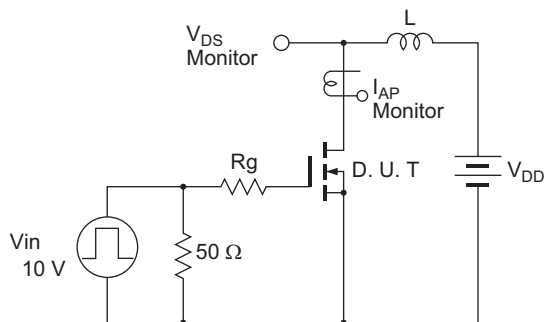
Switching Time Test Circuit



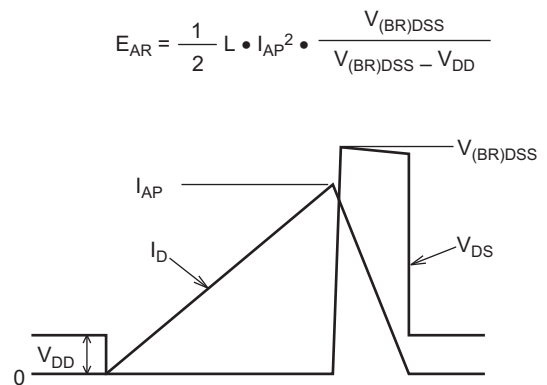
Waveform



Avalanche Test Circuit



Avalanche Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]	Unit: mm
DPAK(S)	SC-63	PRSS0004ZD-C	DPAK(S) / DPAK(S)V	0.28g	

The drawing shows the mechanical dimensions of the RJF0619JPD DPAK(S) package. The top view shows a rectangular package with a width of 6.5 ± 0.3 mm and a length of 5.6 ± 0.5 mm. The side view shows a height of 1.5 ± 0.5 mm and a base width of 2.3 ± 0.2 mm. The bottom view shows a width of 5.1 mm and a length of 5.1 mm. The package has a central mounting pad with a width of 1.2 mm and a length of 1.0 mm. The distance between the mounting pads is 2.29 ± 0.5 mm. The package is shown in a perspective view with dimensions in parentheses.

Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJF0619JPD-00-J3	3000 pcs	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

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