ATWILC3000A

Single Chip IEEE 802.11 b/g/n Link Controller with Integrated Bluetooth® 5.0

Introduction

The ATWILC3000A is a single chip IEEE 802.11 b/g/n RF/Baseband/Medium Access Control (MAC) link controller with Bluetooth 5.0, optimized for low-power mobile applications. This chip supports single stream 1x1 IEEE 802.11n mode, providing up to 72 Mbps PHY rate. The ATWILC3000A features fully integrated Power Amplifier (PA), Low Noise Amplifier (LNA), Transmit/Receive (T/R) switch and power management. The ATWILC3000A offers very low power consumption while simultaneously providing high performance and minimal bill of materials.

The ATWILC3000A utilizes highly optimized IEEE 802.11 Bluetooth coexistence protocols, and provides Serial Peripheral Interface (SPI) and Secure Digital Input Output (SDIO) to interface with the host controller. The only external clock sources required for the ATWILC3000A are a high-speed 26 MHz crystal oscillator and a 32.768 kHz clock for Sleep operation. The ATWILC3000A is available in the QFN package.

Features

IEEE 802.11:

- IEEE 802.11 b/g/n 20 MHz (1x1) Solution
- Single Spatial Stream in 2.4 GHz ISM Band
- Integrated Power Amplifier (PA) and Transmit/Receive (T/R) Switch
- Superior Sensitivity and Range via Advanced PHY Signal Processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Wi-Fi Direct® and Soft-AP Support
- Supports IEEE 802.11 WEP, WPA and WPA2 Enterprise Security
- Superior MAC Throughput through Hardware Accelerated Two-Level A-MSDU/A-MPDU Frame Aggregation and Block Acknowledgment
- On-Chip Memory Management Engine to Reduce Host Load
- SPI and SDIO Host Interfaces
- Operating Conditions:
  - Operating temperature: -40°C to +85°C
  - Input/Output supply voltage (VDDIO): 1.62V to 3.6V
  - Power supply (VBATT): 2.5V to 4.2V
- Wi-Fi Alliance® Certified for Connectivity and Optimizations:
  - ID for ATWILC3000-MR110CA (module based on ATWILC3000A chipset): WFA72428

Bluetooth:

- Bluetooth 5.0 (Basic Rate, Enhanced Data Rate and Bluetooth Low Energy[1])
- Frequency Hopping
- Host Control Interface (HCI) through High Speed UART
- Integrated PA and T/R Switch
- Superior Sensitivity and Range
- Bluetooth SIG 5.0 Certification of ATWILC3000-MR110xA (module based on ATWILC3000A chipset): Declaration ID D039158

[1] Bluetooth SIG QDID qualification is for Bluetooth Low Energy only.

Table of Contents

1. Ordering Information and IC Marking

The following table provides the ordering details for the ATWILC3000A.

Table 1-1. Ordering Details

Ordering Code	Package Type	Package Size	IC Marking
ATWILC3000A-MU-ABCD	QFN in Tape and Reel	6 mm x 6 mm	ATWILC3000A

Note:

1. ABCD interprets as:
   “A” can be “Y” indicating Tray or “T” indicating Tape and Reel.

   “BCD” equals “042” for the part assigned with a MAC ID and blank for a part with no MAC ID.

   The following table lists the possible combinations for ordering the ATWILC3000A.

Table 1-2. Ordering Codes

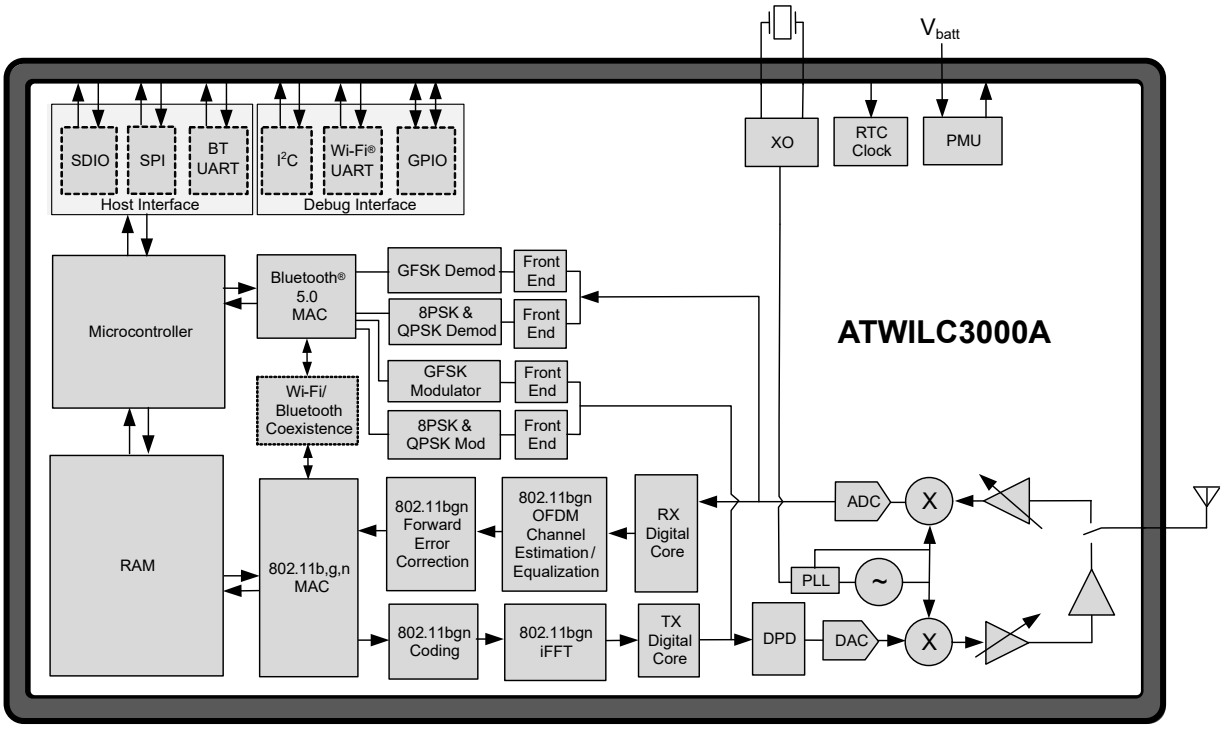
Ordering Code	Description
ATWILC3000A-MU-T	No MAC ID and ship in Tape and Reel
ATWILC3000A-MU-T042	MAC ID assigned and ship in Tape and Reel
ATWILC3000A-MU-Y	No MAC ID and ship in Tray
ATWILC3000A-MU-Y042	MAC ID assigned and ship in Tray

2. Functional Overview

2.1 Block Diagram

The following figure shows the block diagram of the ATWILC3000A.

Figure 2-1. ATWILC3000A Block Diagram



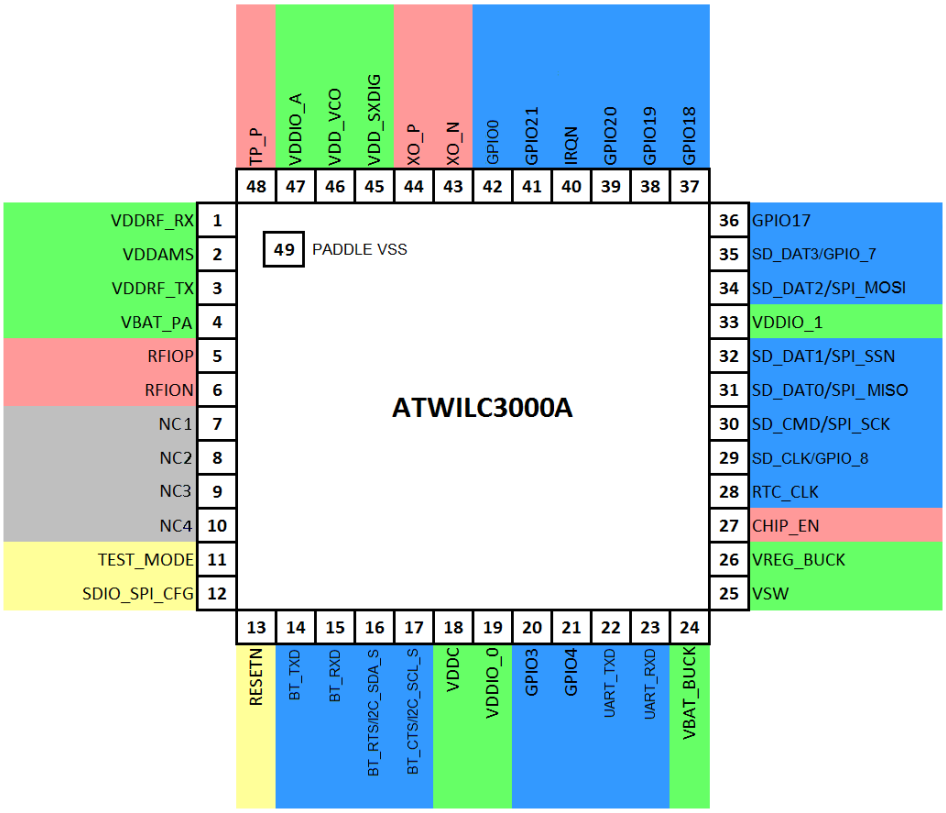
2.2 Pinout and Package Information

2.2.1 Pinout Details

The ATWILC3000A is offered in an exposed pad 48-pin QFN package. This package contains an exposed paddle that must be connected to the system board ground. The following figure shows the QFN package pin assignment. The color shading indicates the pin type as follows:

- Green – Power
- Red – Analog
- Blue – Digital I/O
- Yellow – Digital input
- Grey – Not connected or reserved

Figure 2-2. ATWILC3000A Pin Assignment



The following table provides the ATWILC3000A pin description.

Table 2-1. ATWILC3000A Pin Description

Pin #	Pin Name	Pin Type	Description
1	VDDRF_RX	Power	Tuner RF RX supply
2	VDDAMS	Power	Tuner BB supply
3	VDDRF_TX	Power	Tuner RF TX supply
4	VBAT_PA	Power	Power supply pin for DC/DC converter and PA
5	RFIOP	Analog	Wi-Fi®/Bluetooth® positive RF differential I/O
6	RFION	Analog	Wi-Fi/Bluetooth negative RF differential I/O
7	NC1	—	No connection
8	NC2	—	No connection
9	NC3	—	No connection
10	NC4	—	No connection
11	TEST_MODE	Digital Input	Test mode – the user must connect this pin to a ground
12	SDIO_SPI_CFG	Digital Input	• Connect to VDDIO through a 1 MΩ resistor to enable SPI interface • Connect to GND to enable SDIO interface

.....continued

Pin #	Pin Name	Pin Type	Description
13	RESETN	Digital Input	• Active-low hard Reset • When this pin is asserted low, the module is placed in the Reset state • When this pin is asserted high, the module is taken out of Reset and functions normally • Connect to a host output that defaults low on power-up; if the host output is tri-stated, add a 1 MΩ pull-down resistor to ensure a low level at power-up
14	BT_TXD	Digital I/O, Programmable Pull-up	• Bluetooth UART transmit data output • Connect to UART_RXD of host
15	BT_RXD	Digital I/O, Programmable Pull-up	• Bluetooth UART receive data input • Connect to UART_TXD of host
16	BT_RTS/I2C_SDA_S	Digital I/O, Programmable Pull-up	• I^2C Client data • Used only for debug development purposes • Adding a test point for this pin is recommended. I^2C will be the default configuration. If flow control is enabled, this pin will be configured as UART RTS.
17	BT_CTS/I2C_SCL_S	Digital I/O, Programmable Pull-up	• I^2C Client clock • Used only for debug development purposes • Adding a test point for this pin is recommended. I^2C will be the default configuration. If flow control is enabled, this pin will be configured as UART CTS.
18	VDDC	Power	Digital core power supply
19	VDDIO_0	Power	Digital I/O power supply
20	GPIO3	Digital I/O, Programmable Pull-up	General Purpose IO Port 3(1)
21	GPIO4	Digital I/O, Programmable Pull-up	General Purpose IO Port 4(1)
22	UART_TXD	Digital I/O, Programmable Pull-up	• Wi-Fi UART TXD output • Used only for debug development purposes • Adding a test point for this pin is recommended
23	UART_RXD	Digital I/O, Programmable Pull-up	• Wi-Fi UART RXD input • Used only for debug development purposes • Adding a test point for this pin is recommended
24	VBAT_BUCK	Power	Power supply pin for DC/DC converter
25	VSW	Power	Switching output of DC/DC Converter
26	VREG_BUCK	Power	Core power from DC/DC converter

.....continued

Pin #	Pin Name	Pin Type	Description
27	CHIP_EN	Analog	• PMU enable • High level enables the module • Low level enables the module in Power-Down mode • Connect to a host output that defaults low at power-up • If the host output is tri-stated, add a 1 MΩ pull-down resistor, if necessary, to ensure a low level at power-up
28	RTC_CLK	Digital I/O, Programmable Pull-up	• RTC clock input • Connect to a 32.768 kHz clock source
29	SD_CLK/GPIO_8	Digital I/O, Programmable Pull-up	SDIO clock line from the ATWILC3000A when the module is configured for SDIO
30	SD_CMD/SPI_SCK	Digital I/O, Programmable Pull-up	• SDIO CMD line from ATWILC3000A when the module is configured for SDIO • SPI clock from ATWILC3000A when the module is configured for SPI
31	SD_DAT0/SPI_MISO	Digital I/O, Programmable Pull-up	• SDIO Data Line 0 from the ATWILC3000A when the module is configured for SDIO • SPI MISO (Host In Client Out) pin from the ATWILC3000A when the module is configured for SPI
32	SD_DAT1/SPI_SSN	Digital I/O, Programmable Pull-up	• SDIO Data Line 1 from the ATWILC3000A when the module is configured for SDIO • Active-low SPI SSN (Client Select) pin from the ATWILC3000A when the module is configured for SPI
33	VDDIO_1	Power	Digital I/O power supply
34	SD_DAT2/SPI_MOSI	Digital I/O, Programmable Pull-up	• SDIO Data Line 2 from the ATWILC3000A when the module is configured for SDIO • SPI MOSI (Host Out Client In) pin from the ATWILC3000A when the module is configured for SPI
35	SD_DAT3/GPIO_7	Digital I/O, Programmable Pull-up	SDIO Data Line 3 from the ATWILC3000A when the module is configured for SDIO
36	GPIO17	Digital I/O, Programmable Pull-up	General Purpose I/O Port 17(1)
37	GPIO18	Digital I/O, Programmable Pull-up	General Purpose I/O Port 18(1)
38	GPIO19	Digital I/O, Programmable Pull-up	General Purpose I/O Port 19(1)
39	GPIO20	Digital I/O, Programmable Pull-up	General Purpose I/O Port 20(1)

.....continued			
Pin #	**Pin Name**	**Pin Type**	**Description**
40	IRQN	Digital I/O, Programmable Pull-up	• ATWILC3000A interrupt output • Connect to a host interrupt pin
41	GPIO21	Digital I/O, Programmable Pull-up	General Purpose I/O Port 21(1)
42	GPIO0	Digital I/O, Programmable Pull-up	General Purpose I/O Port 0(1)
43	XO_N	Analog	Crystal oscillator N
44	XO_P	Analog	Crystal oscillator P
45	VDD_SXDIG	Power	SX power supply
46	VDD_VCO	Power	VCO power supply
47	VDDIO_A	Power	Tuner VDDIO power supply
48	TP_P	Analog	Test pin/no connection
49	PADDLE VSS	Power	Connect to system board ground

Note:

1. Use of the GPIO functionality is not supported by the firmware. The data sheet will be updated once the support for this feature is added.

2.2.2 Package Description

The following table provides the ATWILC3000A QFN package information.

Table 2-2. ATWILC3000A QFN Package Information

Parameter	Value	Unit	Tolerance
QFN Pad Count	48	—	—
Package Size	6 x 6	mm	—
Total Thickness	0.85		+0.15/-0.05 mm
QFN Pad Pitch	0.40		—
Pad Width	0.20		—
Exposed Pad Size	4.70 x 4.70		—

3. Clocking

3.1 Crystal Oscillator

The following table provides the crystal oscillator parameters for the ATWILC3000A.

Table 3-1. Crystal Oscillator Parameters

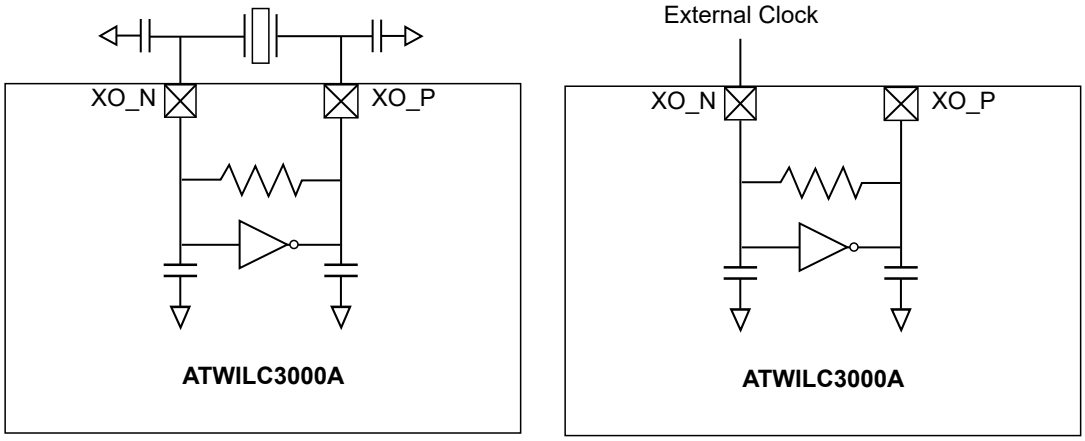
Parameter	Min.	Typ.	Max.	Unit
Crystal Resonant Frequency	—	26	—	MHz
Crystal Equivalent Series Resistance	—	50	150	Ω
Stability – Initial Offset(1)	-100	—	100	ppm
Stability – Temperature and Aging	-20	—	20	

Note:

1. Initial offset must be calibrated to maintain ±20 ppm in all operating conditions when including temperature and aging. This calibration is expected to be performed by the end user during their final production testing.

The block diagram in figure (a) shows how the internal crystal oscillator (XO) is connected to the external crystal. The XO has 5 pF internal capacitance on each terminal, XO_P and XO_N. To bypass the crystal oscillator with an external reference, an external signal capable of driving 5 pF can be applied to the XO_N terminal, as shown in figure (b).

Figure 3-1. Crystal Oscillator Connections



(a) Crystal Oscillator is used

(b) Crystal Oscillator is bypassed

The following table provides the electrical and performance requirements for the external clock.

Table 3-2. Bypass Clock Specification

Parameter	Min.	Typ.	Max.	Unit	Comments
Oscillation Frequency	—	26	—	MHz	Must be able to drive 5 pF load at desired frequency
Voltage Swing	0.5	—	1.2	V_{PP}	Must be AC coupled
Stability – Temperature and Aging	-20	—	+20	ppm	—
Phase Noise	—	—	-130	dBc/Hz	At 10 kHz offset
Jitter (RMS)	—	—	<1	psec	Based on integrated phase noise spectrum from 1 kHz to 1 MHz

3.2 Low-Power Clock

The ATWILC3000A requires an external 32.768 kHz clock to be used for Sleep operation, which is provided through pin 28. The frequency accuracy of this external clock must be within ±500 ppm.

4. CPU and Memory Subsystem

4.1 Processor

The ATWILC3000A has two Cortus APS3 32-bit processors, one is used for Wi-Fi® and the other is used for Bluetooth.

In IEEE 802.11 mode, the processor performs many of the MAC functions, including but not limited to: association, authentication, power management, security key management and MSDU aggregation/deaggregation. In addition, the processor provides flexibility for various modes of operation, such as Station (STA) and Access Point (AP) modes.

In Bluetooth mode, the processor handles multiple tasks of the Bluetooth protocol stack.

4.2 Memory Subsystem

The APS3 core uses a 256 KB instruction/boot ROM (160 KB for IEEE 802.11 and 96 KB for Bluetooth), along with a 420 KB instruction RAM (128 KB for IEEE 802.11 and 292 KB for Bluetooth) and a 128 KB data RAM (64 KB for IEEE 802.11 and 64 KB for Bluetooth). In addition, the device uses a 160 KB shared/exchange RAM (128 KB for IEEE 802.11 and 32 KB for Bluetooth), accessible by the processor and MAC, which allows the processor to perform various data management tasks on the Tx and Rx data packets.

4.3 Nonvolatile Memory (eFuse)

The ATWILC3000A devices have 768 bits of nonvolatile eFuse memory that can be read by the CPU after device Reset. The eFuse is partitioned into six 128-bit banks (Bank 0 – Bank 5). Each bank has the same bit map (see the following figure). The purpose of the first 108 bits in each bank is fixed and the remaining 20 bits are general purpose software-dependent bits or reserved for future use. Currently, the Bluetooth address is derived from the Wi-Fi MAC address, such that Bluetooth address = Wi-Fi MAC address + 1.

This nonvolatile one-time-programmable (OTP) memory can be used for storing the following customer-specific parameters:

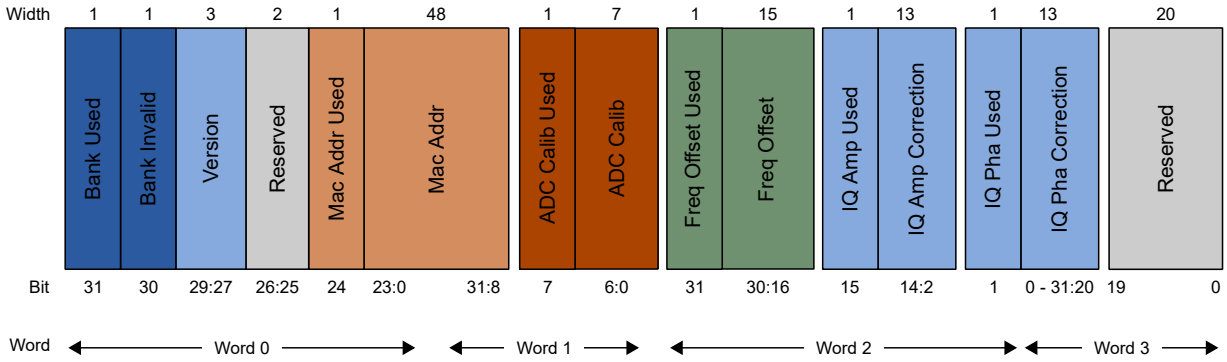
- MAC address.
- Calibration information. For example, crystal frequency offset.
- Other software-specific configuration parameters.

Each bank can be programmed independently, which allows for several updates of the device parameters following the initial programming. For example, if the MAC address is currently programmed in Bank 1 and the MAC address has to be changed, the following steps should be performed:

1. Invalidate the contents of Bank 1 by programming the Bank Invalid bit field of Bank 1.
2. Program Bank 2 with the new MAC address along with the values of ADC Calib (from Bank 1), Frequency Offset (from Bank 1), IQ Amp Correction (from Bank 1) and IQ Pha Correction (from Bank 1). The Used bit field for each corresponding value bit field should also be programmed.
3. Validate the contents of Bank 2 by programming the Bank Used bit field of Bank 2.

Each bit field (that is, MAC Addr, ADC Calib, Freq Offset, IQ Amp Correction and IQ Pha Correction) has its corresponding Used bit field. Each Used bit field is used to indicate to the firmware that the value in the related bit field is valid. A value of '0' in the Used bit field indicates that the following bit field is invalid, and a value of '1' programmed to the Used bit field indicates that the corresponding bit field is valid and can be used by the firmware. By default, all the ATWILC3000A devices are programmed with the ADC Calib, IQ Amp and IQ Phase fields of Bank 0. In IC variants where the MAC address is assigned, the MAC address bit field will be programmed in Bank 0. For more information on IC marking, refer to 1. Ordering Information and IC Marking.

Figure 4-1. Bitmap for ATWILC3000A eFuse Bank



Note: The bit map was updated with bit fields IQ Amp correction and IQ Pha correction fields from firmware version 15.3 for WILC Linux® and 4.5 for WILC RTOS onwards. Earlier, these bit fields were reserved for future use. For customers using firmware older than 15.3 for WILC Linux and 4.5 for WILC RTOS, IQ Amp correction and IQ Pha correction bit fields will not be used by the firmware.

The matrix table below provides details on how different versions of the firmware handle the IQ Amp Used, IQ Amp Correction, IQ Pha Used and IQ Pha Correction bit fields during Initialization.

Firmware Version	IQ Amp Used and IQ Pha Used Bit Status	
	Device with IQ Amp Used and IQ Pha Used Bit Fields with Value as '1'	Device with IQ Amp Used and IQ Pha Used Bit Fields with Value as '0'
15.3 or later for WILC Linux 4.5 or later for WILC RTOS	The firmware loads the IQ calibration values from the IQ Amp Correction and IQ Pha Correction bit fields of the corresponding eFuse bank and proceeds with Initialization.	The firmware ignores the values in the IQ Amp Correction and IQ Pha Correction bit fields and proceeds with Initialization.
Prior to 15.3 for WILC Linux Prior to 4.5 for WILC RTOS	The firmware does not check for the IQ Amp Used and IQ Pha Used bit fields and proceeds with Initialization.	

5. WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC), Physical Layer (PHY) and the radio.

5.1 MAC

The ATWILC3000A is designed to operate at low power, while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response, while providing the flexibility to accommodate evolving standards and future feature enhancements.

The dedicated datapath engines are used to implement datapath functions with heavy computational requirements. For example, a Frame Check Sequence (FCS) engine checks the Cyclic Redundancy Check (CRC) of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES and WPA2 Enterprise security requirements.

Control functions, which have real-time requirements, are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability through the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon TX control, interframe spacing and so on), protocol timer module (responsible for the Network Access vector, backoff timing, timing synchronization function and slot management), MAC Protocol Data Unit (MPDU) handling module, aggregation/deaggregation module, block ACK controller (implements the protocol requirements for burst block communication) and TX/RX control Finite State Machine (FSM) (coordinates data movement between PHY and MAC interface, cipher engine and the Direct Memory Access (DMA) interface to the TX/RX FIFOs).

The following are the characteristics of MAC functions implemented solely in software on the microprocessor:

- Functions with high memory requirements or complex data structures. Examples include association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples include authentication and association.
- Functions that require flexibility and upgradeability. Examples include Beacon frame processing and QoS scheduling.

Features

The ATWILC3000A MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate block Acknowledgment
  - Reduced Interframe Spacing (RIFS)
- IEEE 802.11i and WFA security with key management:
  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- WPA2 Enterprise
- Advanced power management:
  - Standard IEEE 802.11 Power Save mode
  - Wi-Fi alliance WMM-PS (U-APSD)
- RTS-CTS and CTS-to-Self support
- Either STA or AP mode in the infrastructure basic Service Set mode
- Concurrent mode of operation

- Independent Basic Service Set (IBSS)

5.2 PHY

The ATWILC3000A WLAN PHY is designed to achieve reliable and power-efficient physical layer communication, specified by IEEE 802.11 b/g/n, in Single Stream mode with 20 MHz bandwidth. The advanced algorithms are used to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions, such as Fast Fourier Transform (FFT), filtering, Forward Error Correction (FEC) that is a Viterbi decoder, frequency, timing acquisition and tracking, channel estimation and equalization, carrier sensing, clear channel assessment and automatic gain control.

Features

The IEEE 802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20 MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5 and 11 Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12, 18, 24, 36, 48 and 54 Mbps
- Supports IEEE 802.11n HT modulations, MCS0-7, 20 MHz, 800 and 400 ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0 and 72.2 Mbps(1)
- IEEE 802.11n Mixed mode operation
- Per packet Tx power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery and frame detection

Note:

1. Currently, short GI is not supported by firmware. The data sheet will be updated when the feature is supported.

5.3 Radio

This section presents information describing the properties and characteristics of the ATWILC3000A, and Wi-Fi radio transmit and receive performance capabilities of the device.

The performance measurements are taken at the RF pin assuming 50Ω impedance; the RF performance is assured for a room temperature of 25°C with a derating of 2-3 dB at boundary conditions.

Note: Measured after RF matching network.

Table 5-1. Features and Properties

Feature	Description
Part Number	ATWILC3000A
WLAN Standard	IEEE 802.11 b/g/n, Wi-Fi compliant
Host Interface	SPI, SDIO
Dimension	6.0 mm x 6.0 mm
Frequency Range	2.412 GHz ~ 2.472 GHz (2.4 GHz ISM Band)
Number of Channels	11 for North America, and 13 for Europe and Japan
Modulation	• 802.11b: DQPSK, DBPSK, CCK • 802.11g/n: OFDM/64-QAM, 16-QAM, QPSK, BPSK
Data Rate	802.11b: 1, 2, 5.5, 11 Mbps
	802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
Data Rate (20 MHz, normal GI, 800 ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65 Mbps

.....continued	
Feature	**Description**
Data Rate (20 MHz, short GI, 400 ns)[1]	802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65, 72.2 Mbps
Operating Temperature	-40 to +85°C

Note:

1. Currently, short GI is not supported by firmware. The data sheet will be updated when the feature is supported.

6. Bluetooth Subsystem

The Bluetooth Subsystem implements all the mission-critical real-time functions required for full compliance with the specification of the Bluetooth System, v5.0, Bluetooth SIG. The baseband controller consists of a modem and a Medium Access Controller (MAC), which encodes/decodes HCI packets, constructs baseband data packages, and manages and monitors connection status, slot usage, data flow, routing, segmentation and buffer control.

The Bluetooth Subsystem performs Link Control Layer management supporting the following states:

- Standby
- Connection
- Page and Page Scan
- Inquiry and Inquiry Scan
- Sniff

6.1 Bluetooth 5.0

Features:

- Extended Inquiry Response (EIR)
- Encryption Pause/Resume (EPR)
- Sniff Sub-Rating (SSR)
- Secure Simple Pairing (SSP)
- Link Supervision Timeout (LSTO)
- Link Management Protocol (LMP)
- Quality of Service (QOS)

6.2 Bluetooth Low Energy (BLE)

Supports BLE profiles allowing connection to advanced low energy applications such as:

- Smart Energy
- Consumer Wellness
- Home Automation
- Security
- Proximity Detection
- Entertainment
- Sports and Fitness
- Automotive

7. External Interfaces

The ATWILC3000A supports the following external interfaces:

- SPI Client and SDIO Client for IEEE 802.11 Control and Data Transfer
- BT UART for Bluetooth Control and Data Transfer
- I^2C Client for Debug
- Wi-Fi UART for IEEE 802.11 Debug Logs
- General Purpose Input/Output (GPIO) Pins(1)

Note:

1. Use of the GPIO functionality is not supported by the firmware. The data sheet will be updated once the support for this feature is added.

7.1 Interfacing with Host Microcontroller

This section describes how to interface the ATWILC3000A with the host microcontroller. The interface comprises of a Client SPI/SDIO and additional control signals, as shown in Figure 7-1. Additional control signals are connected to the GPIO/IRQ interface of the microcontroller.

Figure 7-1. Interfacing with the Host Microcontroller

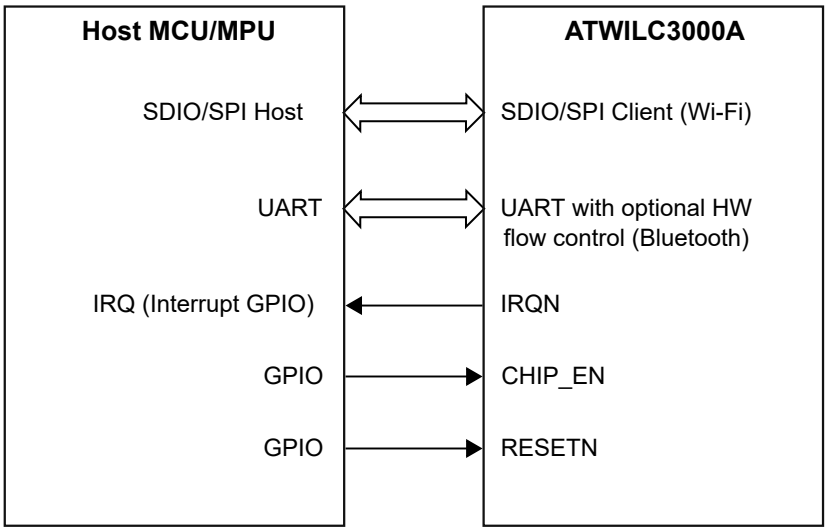


Table 7-1. Host Microcontroller Interface Pins

IC Pin#	Function(1)
13	RESETN
14	BT_TXD
15	BT_RXD
16	BT_RTS
17	BT_CTS
27	CHIP_EN
29	SD_CLK
30	SD_CMD/SPI_SCK
31	SD_DAT0/SPI_TXD
32	SD_DAT1/SPI_SSN
34	SD_DAT2/SPI_RXD
35	SD_DAT3
40	IRQN

Notes:

1. Logic input for IC pin SDIO_SPI_CFG(#12) determines whether SDIO or SPI Client interface is enabled.
   - Connect SDIO_SPI_CFG to VDDIO through a 1 MΩ resistor to enable the SPI interface.
   - Connect SDIO_SPI_CFG to ground to enable the SDIO interface.
2. Adding test points for the IC pins BT_TXD (#14), BT_RXD (#15), BT_RTS (#16), BT_CTS (#17), UART_TXD (#22) and UART_RXD (#23) in the design is recommended.

7.2 I²C Client Interface

The I²C Client interface is a two-wire serial interface consisting of a Serial Data Line (SDA) on pin #16 and a Serial Clock Line (SCL) on pin #17. This interface is used for debugging of the ATWILC3000A.

I²C Client responds to the 7-bit address value 0x60. The ATWILC3000A I²C supports I²C bus Version 2.1 - 2000 and can operate in following modes:

- Standard mode (with data rates up to 100 kbps)
- Fast mode (with data rates up to 400 kbps)

Note: For specific information on the I²C bus, refer to the Philips Specification entitled, *"The I²C-Bus Specification, Version 2.1"*.

The I²C Client is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for Stop, Start and Restart conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400 pF. Data are transmitted in byte packages.

7.3 SPI Client Interface

The ATWILC3000A provides a Serial Peripheral Interface (SPI) that operates as an SPI Client. The SPI Client interface can be used for control and for serial I/O of IEEE 802.11 data. The SPI Client pins are mapped as shown in the following table. The RXD pin is the same as the Host Output, Client Input (MOSI) and the TXD pin is the same as the Host Input, Client Output (MISO). The SPI Client is a full-duplex, client-synchronous serial interface that is available immediately following Reset when pin 12 (SDIO_SPI_CFG) is connected to VDDIO.

Table 7-2. SPI Client Interface Pin Mapping

Pin #	SPI Function
12	CFG: Must be connected to VDDIO
30	SCK: Serial Clock
31	TXD: Serial Data Transmit (MISO)
32	SSN: Active-Low Client Select
34	RXD: Serial Data Receive (MOSI)

When the SPI is not selected, that is, when SSN is high, the SPI interface will not interfere with data transfers between the serial host and other serial client devices. When the serial Client is not selected, its transmitted data output is buffered, resulting in a high-impedance drive onto the serial Host receive line.

The SPI Client interface responds to a protocol that allows an external Host to read or write any register in the chip and initiate DMA data transfers.

The SPI Client interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in the following table.

Table 7-3. SPI Client Modes

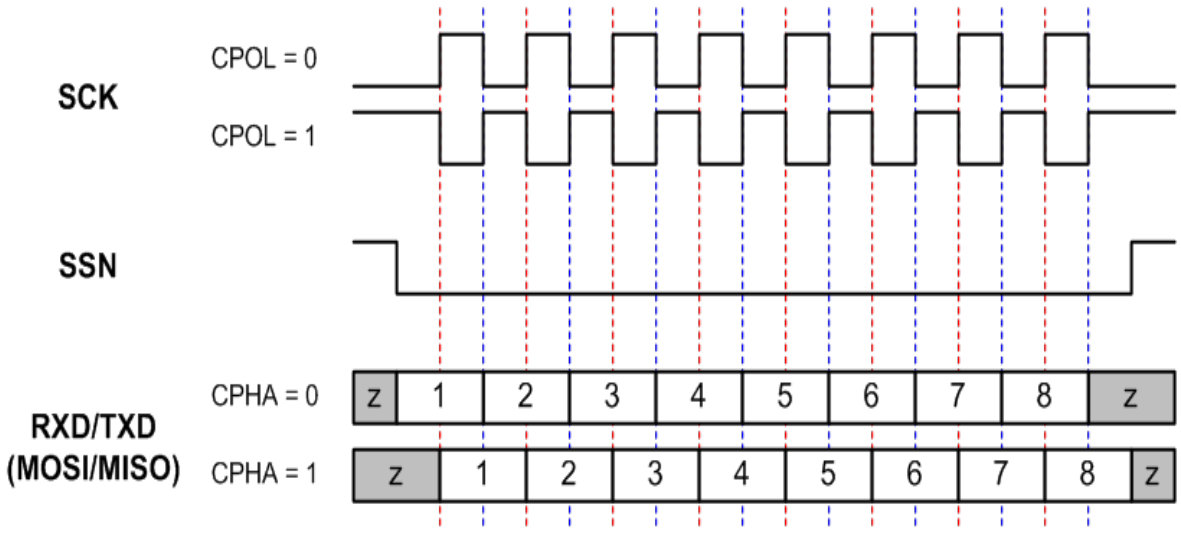
Mode	CPOL	CPHA
0(1)	0	0
1	0	1
2	1	0
3	1	1

Note:

1. The ATWILC3000A firmware uses “SPI Mode 0” to communicate with the host.

The red lines in the following figure correspond to the Clock Phase at 0 and the blue lines correspond to the Clock Phase at 1.

Figure 7-2. SPI Client Clock Polarity and Clock Phase Timing



7.4 SDIO Client Interface

The ATWILC3000A SDIO Client is a full-speed interface. This interface supports the 1-bit/4-bit SD Transfer mode at the clock range of 0-50 MHz. The Host can use this interface to read and write from any register within the chip, and configure the ATWILC3000A for DMA data transfer. To use this interface, pin 12 (SDIO_SPI_CFG) must be connected to ground. The following table provides mapping of the SDIO Client pins in the ATWILC3000A.

Table 7-4. SDIO Interface Pin Mapping

Pin #	SPI Function
12	CFG: Must be connected to ground
29	CLK: Clock
30	CMD: Command
31	DAT0: Data 0
32	DAT1: Data 1
34	DAT2: Data 2
35	DAT3: Data 3

When the SDIO card is inserted into an SDIO aware Host, the detection of the card is through the means described in the SDIO specification. During the normal initialization and interrogation of the card by the Host, the card identifies itself as an SDIO device. The Host software obtains the card information in a tuple (linked list) format and determines if that card's I/O function(s) are acceptable to activate. If the card is acceptable, it is allowed to power up fully and start the I/O function(s) built into it.

The SD memory card communication is based on an advanced 9-pin interface (clock, command, four data lines and three power lines) designed to operate at a maximum operating frequency of 50 MHz.

Features

- Supports SDIO card specification version 2.0
- Host clock rate is variable, between 0 and 50 MHz
- Supports 1-bit/4-bit SD Bus modes
- Allows card to interrupt Host
- Responds to direct read/write (IO52) and extended read/write (IO53) transactions
- Supports suspend/resume operation

7.5 UART Debug Interface

The ATWILC3000A provides Universal Asynchronous Receiver/Transmitter (UART) interfaces for serial communication in both IEEE 802.11 and Bluetooth subsystems.

- The Bluetooth subsystem has one 4-pin UART interface (BT UART), which can be used for control and data transfer.
- The IEEE 802.11 subsystem has one 2-pin UART interface (Wi-Fi UART), which can be used for debugging.

The UART interfaces are compatible with the RS-232 standard, where the ATWILC3000A operates as a Data Terminal Equipment (DTE) type device. The 2-pin UART uses receive and transmit pins (RXD and TXD). The 4-pin UART uses two pins for data (TXD and RXD) and two pins for flow control/handshaking: Request-to-Send (RTS) and Clear-to-Send (CTS).

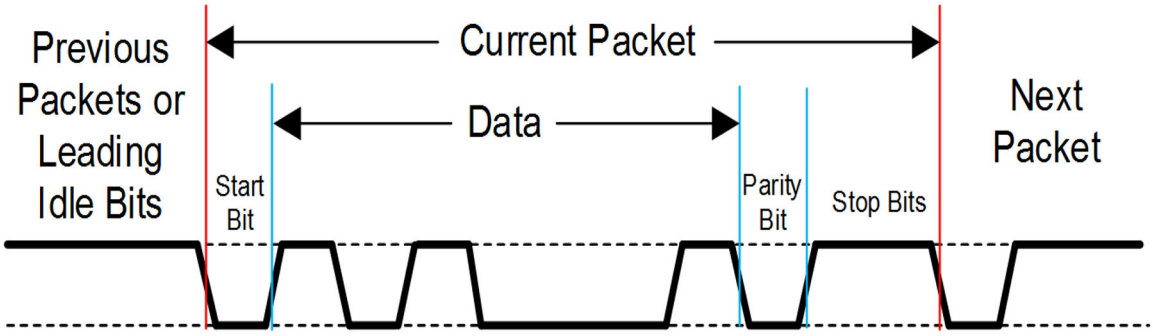
Bluetooth UART is available in pins #14 (BT_TXD), #15 (BT_RXD), #16 (BT_RTS) and #17 (BT_CTS). Wi-Fi UART is available in pins #22 (UART_TXD) and #23 (UART_RXD). The following is the default configuration for the Wi-Fi UART interface of the ATWILC3000A:

- Baud rate: 115200
- Data: 8-bit
- Parity: None
- Stop bit: 1-bit
- Flow control: None

Important: The UART RTS and UART CTS pins are used for hardware flow control. These pins must be connected to the Host MCU UART and enabled for the UART interface to be functional.

An example of UART receiving or transmitting a single packet is shown in following figure. This example shows 7-bit data (0x45), odd parity and two Stop bits.

Figure 7-3. Example of UART Rx or Tx Packet



7.6 GPIOs

Ten General Purpose Input/Output (GPIO) pins, labeled GPIO 0, GPIO 3-4, GPIO 7-8 and GPIO 17-21, are allowed to perform specific functions of an application. Each GPIO pin can be programmed as an input (the value of the pin can be read by the Host or internal processor) or as an output (the output values can be programmed by the Host or internal processor), where the default mode after power-up is input. GPIOs 7 and 8 are only available when the Host does not use the SDIO interface, which shares two of its pins with these GPIOs. Therefore, for SDIO-based applications, six GPIOs (0, 3-4 and 17-21) are available.

Note: Usage of the GPIO functionality is not supported by the firmware. The data sheet will be updated once the support for this feature is added.

7.7 Internal Pull-up Resistors

The ATWILC3000A provides programmable pull-up resistors on various pins. The purpose of these resistors is to keep any unused input pins from floating, which can cause excess current to flow through the input buffer from the VDDIO supply. Any unused pin on the device should leave these pull-up resistors enabled in order to avoid the pin floating.

The default state at power-up should be enabled for the pull-up resistor. However, any pin which is used should have the pull-up resistor disabled. The reason is that if any pins are driven to a low level while the device is in the low-power Sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module.

Since the value of the pull-up resistor is approximately 100 kΩ, the current through any pull-up resistor that is being driven low will be VDDIO/100k. For VDDIO = 3.3V, the current would be approximately 33 µA. Pins which are used and have had the programmable pull-up resistor disabled should always be actively driven to either a high or low level and not be allowed to float.

8. Power Management

8.1 Power Architecture

The ATWILC3000A uses an innovative power architecture to eliminate the requirement for external regulators and reduce the number of off-chip components. This architecture is shown in the following figure. The Power Management Unit (PMU) has a DC/DC converter that converts VBAT to the core supply used by the digital and RF/AMS blocks. The typical values for the digital and RF/AMS core voltages are shown in the following table. The PA and eFuse are supplied by dedicated LDOs, and the VCO is supplied by a separate LDO structure.

Figure 8-1. Power Architecture

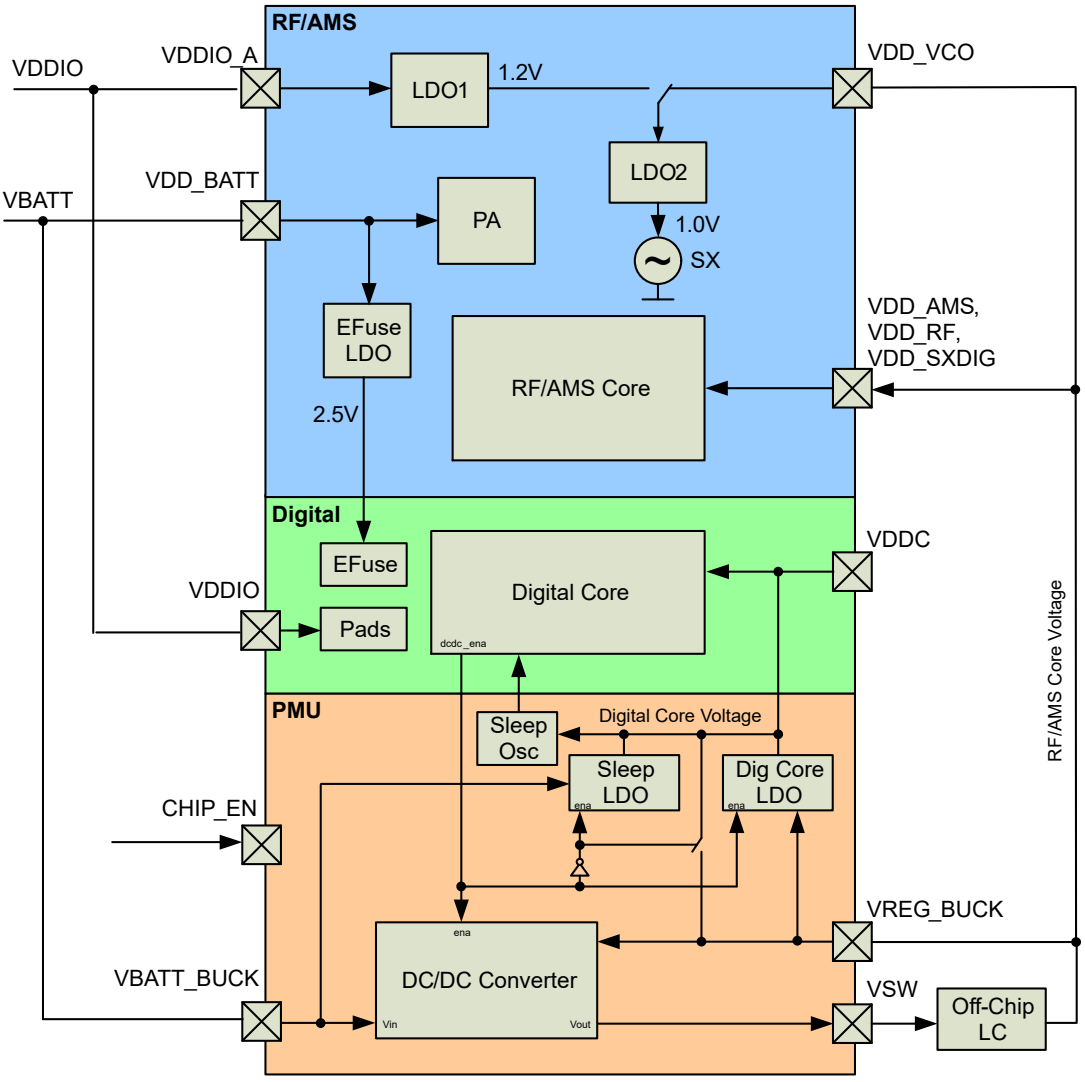


Table 8-1. PMU Output Voltages

Parameter	Typical
RF/AMS Core Voltage (VREG_BUCK)	1.3V
Digital Core Voltage (VDDC)	1.1V

The power connections shown provide a conceptual framework for understanding the ATWILC3000A power architecture. Refer to the reference design for an example of power supply connections, including proper isolation of the supplies used by the digital and RF/AMS blocks.

8.2 Power Consumption

8.2.1 Device States

The ATWILC3000A has multiple device states based on the state of the IEEE 802.11 and Bluetooth subsystems.

- ON_WiFi_Transmit – Device actively transmits IEEE 802.11 signal
- ON_WiFi_Receive – Device actively receives IEEE 802.11 signal
- ON_BT_Transmit – Device actively transmits Bluetooth signal
- ON_BT_Receive – Device actively receives Bluetooth signal
- ON_Doze – Device is powered on but it does not actively transmit or receive data
- Power_Down – Device core supply is powered off (leakage)

The following table shows different device states and its power consumption. The device states can be switched using the following:

- CHIP_EN – Device pin (pin 27) enables or disables the DC/DC converter
- VDDIO – I/O supply voltage from external supply

In the ON states, VDDIO is on and CHIP_EN is high (at VDDIO voltage level). To switch between the ON states and Power_Down state, the CHIP_EN has to change between high and low (GND) voltage. When VDDIO is off and CHIP_EN is low, the chip is powered off with minimal leakage (see 8.2.3 Restrictions for Power States).

8.2.2 Current Consumption in Various Device States

The following table shows different device states and their power consumption for the ATWILC3000A. The device states can be switched using the following:

- CHIP_EN – Module pin (pin 19) enables or disables the DC/DC converter
- VDDIO – I/O supply voltage from external supply

In the ON states, VDDIO is on and CHIP_EN is high (at VDDIO voltage level). To change from the ON states to Power_Down state, connect the RESETN and CHIP_EN pin to logic low (GND) by following the power-down sequence mentioned in 8.3 Power-up/Down Sequence. When VDDIO is off and CHIP_EN is low, the chip is powered off with no leakage.

Table 8-2. Device States Current Consumption

Device State	Code Rate	Output Power (dBm)	Current Consumption(1)	
			I_{VBAT}	I_{VDDIO}
ON_WiFi_Transmit	802.11b 1 Mbps	17.0	272 mA	23.9 mA
	802.11b 11 Mbps	18.5	269 mA	23.9 mA
	802.11g 6 Mbps	17.5	281 mA	23.9 mA
	802.11g 54 Mbps	16.0	234 mA	23.9 mA
	802.11n MCS 0	17.0	280 mA	23.9 mA
	802.11n MCS 7	13.0	229 mA	23.9 mA
ON_WiFi_Receive	802.11b 1 Mbps	—	60.5 mA	23.6 mA
	802.11b 11 Mbps	—	60.5 mA	23.6 mA
	802.11g 6 Mbps	—	60.5 mA	23.6 mA
	802.11g 54 Mbps	—	60.5 mA	23.6 mA
	802.11n MCS 0	—	60.5 mA	23.6 mA
	802.11n MCS 7	—	60.5 mA	23.6 mA
ON_BT_Transmit	BLE 1 Mbps	1.5	98.6 mA	2.5 mA
ON_BT_Receive	BLE 1 Mbps	—	69.1 mA	2.5 mA
Doze (Bluetooth® Low Energy Low Power)	—	—	1.4 mA(2)	
Power_Down	—	—	1.25 µA(2)	

Notes:

1. Conditions: VBAT = 3.3V, VDDIO = 3.3V at 25°C.
2. The current consumption mentioned for these states is the sum of the current consumed in the VDDIO and VBAT voltage rails.

When power is not supplied to the device (DC/DC converter output and VDDIO are off at ground potential), voltage cannot be applied to the ATWILC3000A pins because each pin contains an ESD diode from the pin to supply. This diode turns on when voltage higher than one diode drop is supplied to the pin.

If voltage must be applied to the signal pads when the chip is in a low-power state, the VDDIO supply must be on, so the Power_Down state must be used. Similarly, to prevent the pin-to-ground diode from turning on, do not apply voltage that is more than one diode drop below the ground to any pin.

8.2.3 Restrictions for Power States

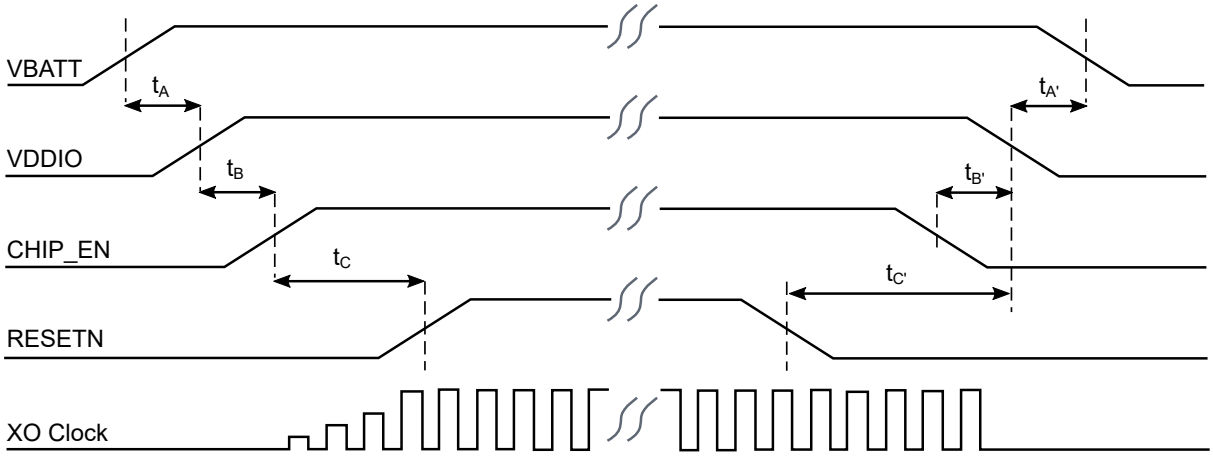
When power is not supplied to the device (DC/DC converter output and VDDIO are off at ground potential), voltage cannot be applied to the ATWILC3000A pins because each pin contains an ESD diode from the pin to supply. This diode turns on when voltage higher than one diode drop is supplied to the pin.

If voltage must be applied to the signal pads when the chip is in a low-power state, the VDDIO supply must be on, so the Power_Down state must be used. Similarly, to prevent the pin-to-ground diode from turning on, do not apply voltage that is more than one diode drop below the ground to any pin.

8.3 Power-up/Down Sequence

The following figure illustrates the power-up/down sequence for the ATWILC3000A.

Figure 8-2. Power-up/Down Sequence



The following table provides power-up/down sequence timing parameters.

Table 8-3. Power-up/Down Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_A	0	—	ms	VBAT rise to VDDIO rise	VBAT and VDDIO can rise simultaneously or be connected together. VDDIO must not rise before VBAT.
t_B	0	—	ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low and must not be left floating.
t_C	5	—	ms	CHIP_EN rise to RESETN rise	This delay is required to stabilize the XO clock before RESETN removal. RESETN must be driven high or low and must not be left floating.
$t_{A'}$	0	—	ms	VDDIO fall to VBAT fall	VBAT and VDDIO fall simultaneously or are connected together. VBAT must not fall before VDDIO.
$t_{B'}$	0	—	ms	CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN must fall simultaneously.
$t_{C'}$	0	—	ms	RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN fall simultaneously.

8.4 Digital I/O Pin Behavior During Power-up Sequences

The following table represents the digital I/O pin states corresponding to the device power modes.

Table 8-4. Digital I/O Pin Behavior in Different Device States

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input Driver	Pull-up/Down Resistor (96 kΩ)
Power_Down: Core Supply Off	High	Low	Low	Disabled (High-Z)	Disabled	Disabled
Power-on Reset: Core Supply and HardReset On	High	High	Low	Disabled (High-Z)	Disabled	Enabled
Power-on Default: Core Supply On, Device Out of Reset and Not Programmed	High	High	High	Disabled (High-Z)	Enabled	Enabled
On_Doze/On_Transmit/ On_Receive: Core Supply On, Device Programmed by Firmware	High	High	High	Programmed by Firmware for Each Pin: Enabled or Disabled	Opposite of Output Driver State	Programmed by Firmware for Each Pin: Enabled or Disabled

9. Electrical Characteristics

This chapter provides an overview of the electrical characteristics of the ATWILC3000A.

9.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings for the ATWILC3000A.

Table 9-1. ATWILC3000A Absolute Maximum Ratings

Characteristic	Symbol	Min.	Max.	Unit
Core Supply Voltage	VDDC	-0.3	1.5	V
I/O Supply Voltage	VDDIO	-0.3	5.0	
Battery Supply Voltage	VBAT	-0.3	5.0	
Digital Input Voltage	V_{IN}(1)	-0.3	VDDIO	
Analog Input Voltage	V_{AIN}(2)	-0.3	1.5	
ESD Human Body Model	V_{ESDHBM}(3)	-1000, -2000 (see notes below)	+1000, +2000 (see notes below)	
Storage Temperature	T_A	-65	150	ºC
Junction Temperature	—	—	125	
RF Input Power Max.	—	—	23	dBm

Notes:

1. V_{IN} corresponds to all the digital pins.
2. V_{AIN} corresponds to the following analog pins: VDD_RF_RX, VDD_RF_TX, VDD_AMS, RFIOP, RFION, XO_N, XO_P, VDD_SXDIG and VDD_VCO.
3. For V_{ESDHBM}, each pin is classified as Class 1 or Class 2, or both:
   - 3.1. The Class 1 pins include all the pins (both analog and digital).
   - 3.2. The Class 2 pins include all digital pins only.
   - 3.3. V_{ESDHBM} is ±1 kV for Class 1 pins. V_{ESDHBM} is ± 2kV for Class 2 pins.

⚠ CAUTION Stresses beyond those listed under “Absolute Maximum Ratings” cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods affects the device reliability.

9.2 Recommended Operating Conditions

The following table provides the recommended operating conditions for the ATWILC3000A.

Table 9-2. ATWILC3000A Recommended Operating Conditions

Characteristic	Symbol	Min.	Typ.	Max.	Units
I/O Supply Voltage Low Range	$VDDIO_L$(2)	1.62	1.80	2.00	V
I/O Supply Voltage Mid-Range	$VDDIO_M$(2)	2.00	2.50	3.00	
I/O Supply Voltage High Range	$VDDIO_H$(2)	3.00	3.30	3.60	
Battery Supply Voltage	VBAT	2.5(3)	3.30	4.20	
Operating Temperature	—	-40	—	85	°C

Notes:

1. Battery supply voltage is applied to the VBAT pin.
2. I/O supply voltage is applied to the VDDIO pin.
3. The ATWILC3000A is functional across this range of voltages; however, optimal RF performance is assured for VBAT in the range ≥ 3.0V VBAT ≤ 4.2V.

9.3 DC Characteristics

The following table provides the DC characteristics for the ATWILC3000A digital pads.

Table 9-3. DC Electrical Characteristics

VDDIO Condition	Characteristic	Min.	Typ.	Max.	Unit
$VDDIO_L$	Input Low Voltage (V_{IL})	-0.30	—	0.60	V
	Input High Voltage (V_{IH})	VDDIO – 0.60	—	VDDIO + 0.30	
	Output Low Voltage (V_{OL})	—	—	0.45	
	Output High Voltage (V_{OH})	VDDIO – 0.50	—	—	
$VDDIO_M$	Input Low Voltage (V_{IL})	-0.30	—	0.63	
	Input High Voltage (V_{IH})	VDDIO – 0.60	—	VDDIO + 0.30	
	Output Low Voltage (V_{OL})	—	—	0.45	
	Output High Voltage (V_{OH})	VDDIO – 0.50	—	—	
$VDDIO_H$	Input Low Voltage (V_{IL})	-0.30	—	0.65	
	Input High Voltage (V_{IH})	VDDION – 0.60	—	VDDIO + 0.30 (up to 3.60)	
	Output Low Voltage (V_{OL})	—	—	0.45	
	Output High Voltage (V_{OH})	VDDIO – 0.50	—	—	
All	Output Loading	—	—	20	pF
	Digital Input Load	—	—	6	
$VDDIO_L$	Pad Driver Strength	1.7	2.4	—	mA
$VDDIO_M$	Pad Driver Strength	3.4	6.5	—	
$VDDIO_H$	Pad Driver Strength	10.6	13.5	—	

9.4 IEEE 802.11 b/g/n Radio Performance

9.4.1 IEEE 802.11 Receiver Performance

The receiver performance under nominal conditions are:

- VBAT = 3.3V
- VDDIO = 3.3V
- Temp = 25°C
- Measured after DC blocking capacitor (C19) as in 10. Reference Design

The following table provides the receiver performance characteristics for the ATWILC3000A.

Table 9-4. IEEE 802.11 Receiver Performance Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	—	2,412	—	2,742	MHz
Sensitivity 802.11b	1 Mbps DSSS	—	-95.0	—	dBm
	2 Mbps DSSS	—	-93.5	—	
	5.5 Mbps DSSS	—	-90.0	—	
	11 Mbps DSSS	—	-86.0	—	
Sensitivity 802.11g	6 Mbps OFDM	—	-90.0	—	dBm
	9 Mbps OFDM	—	-88.5	—	
	12 Mbps OFDM	—	-86.0	—	
	18 Mbps OFDM	—	-84.5	—	
	24 Mbps OFDM	—	-82.0	—	
	36 Mbps OFDM	—	-78.5	—	
	48 Mbps OFDM	—	-74.5	—	
	54 Mbps OFDM	—	-73.0	—	
Sensitivity 802.11n (BW = 20 MHz)	MCS 0	—	-89.0	—	dBm
	MCS 1	—	-87.0	—	
	MCS 2	—	-84.0	—	
	MCS 3	—	-81.5	—	
	MCS 4	—	-78.0	—	
	MCS 5	—	-74.0	—	
	MCS 6	—	-72.0	—	
	MCS 7	—	-70.0	—	
Maximum Receive Signal Level	1-11 Mbps DSSS	—	0	—	dBm
	6-54 Mbps OFDM	—	0	—	
	MCS 0 – 7 (800 ns GI)	—	0	—	

.....continued					
Parameter	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**
Adjacent Channel Rejection	1 Mbps DSSS (30 MHz offset)	—	50	—	dB
	11 Mbps DSSS (25 MHz offset)	—	43	—	
	6 Mbps OFDM (25 MHz offset)	—	40	—	
	54 Mbps OFDM (25 MHz offset)	—	25	—	
	MCS 0 – 20 MHz BW (25 MHz offset)	—	40	—	
	MCS 7 – 20 MHz BW (25 MHz offset)	—	20	—	

9.4.2 IEEE 802.11 Transmitter Performance

The transmitter performance under nominal conditions are:

- VBAT = 3.3V
- VDDIO = 3.3V
- Temp = 25°C
- Measured after DC blocking capacitor (C19) as in 10. Reference Design

The following table provides the transmitter performance characteristics for the ATWILC3000A.

Table 9-5. IEEE 802.11 Transmitter Performance Characteristics(3,5)

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	—	2,412	—	2,472	MHz
Output Power	802.11b 1 Mbps	—	15.5(1)	—	dBm
	802.11b 11 Mbps	—	16.5(1)	—	
	802.11g OFDM 6 Mbps	—	17.0(1)	—	
	802.11g OFDM 54 Mbps	—	14.0(1)	—	
	802.11n HT20 MCS 0 (800 ns GI)	—	17.0	—	
	802.11n MCS 7 (800 ns GI)	—	10.5(1)	—	
Tx Power Accuracy(4)	—	—	±1.5(2)	—	dB
Carrier Suppression	—	—	30.0	—	dBc
Harmonic Output Power (Radiated, Regulatory mode)	2nd Harmonics	—	—	-41	dBm/MHz
Harmonic Output Power (Radiated, Regulatory mode)	3rd Harmonics	—	—	-41	

Notes:

1. Measured at IEEE 802.11 specification compliant EVM/Spectral mask.
2. Measured after DC blocking capacitor (C19) as in 10. Reference Design.
3. Operating temperature range is -40°C to +85°C. RF performance is assured at a room temperature of 25°C with a 2-3 dB change at boundary conditions.
4. With respect to TX power, different (higher/lower) RF output power settings may be used for specific antennas and/or enclosures, in which case, recertification may be required.
5. The availability of some specific channels and/or operational frequency bands are country-dependent and should be programmed at the host product factory to match the intended destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via Host implementation.

9.5 Bluetooth Radio Performance

9.5.1 Receiver Performance

The receiver performance under nominal conditions are:

- VBAT = 3.3V
- VDDIO = 3.3V
- Temp: 25°C
- Measured after the DC blocking capacitor (C19) as in 10. Reference Design

The following table provides the Bluetooth receiver performance characteristics for the ATWILC3000A.

Table 9-6. Bluetooth Receiver Performance Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	—	2,402	—	2,480	MHz
Sensitivity Ideal TX	GFSK 1 Mbps – Basic Rate(1)	—	-91.5	—	dBm
	π/4 DQPSK 2 Mbps(1)	—	-89.0	—	
	8DPSK 3 Mbps(1)	—	-86.0	—	
	BLE (GFSK)	—	-92.5	—	
Maximum Receive Signal Level	BLE (GFSK)	—	0	—	dBm
Interference Performance (BLE)	Co-channel	—	9	—	dB
	adjacent + 1 MHz	—	-3	—	
	adjacent – 1 MHz	—	0	—	
	adjacent + 2 MHz (image frequency)	—	-28	—	
	adjacent – 2 MHz	—	-44	—	
	adjacent + 3 MHz (adjacent to image)	—	-38	—	
	adjacent – 3 MHz	—	-38	—	
	adjacent + 4 MHz	—	-48	—	
	adjacent – 4 MHz	—	-33	—	
	adjacent +5 MHz	—	-37	—	
	adjacent – 5 MHz	—	-33	—	

Note:

1. The data are preliminary.

9.5.2 Transmitter Performance

The transmitter performance under nominal conditions are:

- VBAT = 3.3V
- VDDIO = 3.3V
- Temp = 25°C
- Measured after the DC blocking capacitor (C19) as in 10. Reference Design

The following table provides the Bluetooth transmitter performance characteristics for the ATWILC3000A.

Table 9-7. Bluetooth Transmitter Performance Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	—	2,402	—	2,480	MHz
Sensitivity Ideal TX	GFSK 1 Mbps – Basic Rate(1)	—	1.8	—	dBm
	π/4 DQPSK 2 Mbps(1)	—	1.8	—	
	8DPSK 3 Mbps(1)	—	1.8	—	
	BLE (GFSK)	—	1.5	—	
In-Band Spurious Emission (Bluetooth Low Energy)	N+2 (Image Frequency)	—	-32	—	dB
	N+3 (Adjacent to Image Frequency)	—	-36	—	
	N-2	—	-52	—	
	N-3	—	-54	—	

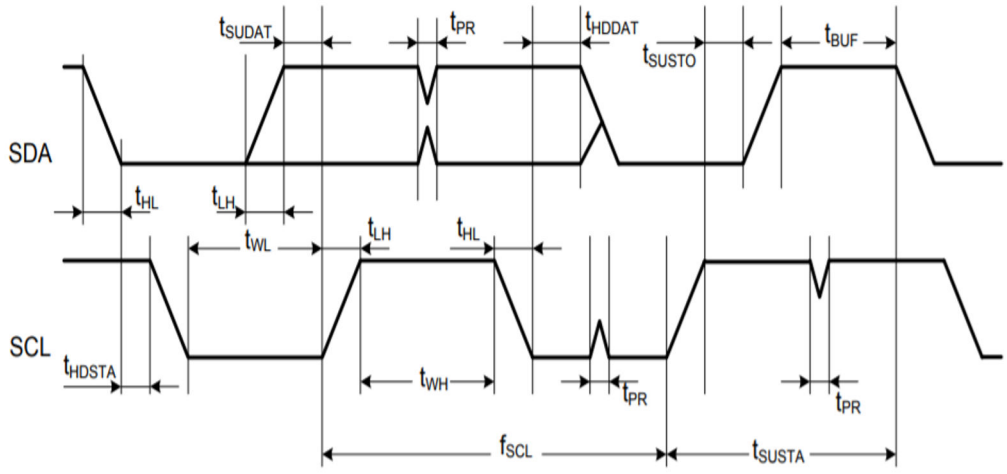
Note:
1. The data are preliminary.

9.6 Timing Characteristics

9.6.1 I²C Client Interface Timing Diagram

The I²C Client timing diagram for the ATWILC3000A is shown in the following figure.

Figure 9-1. I²C Client Timing Diagram



The following table provides the I^2C Client timing parameters for the ATWILC3000A.

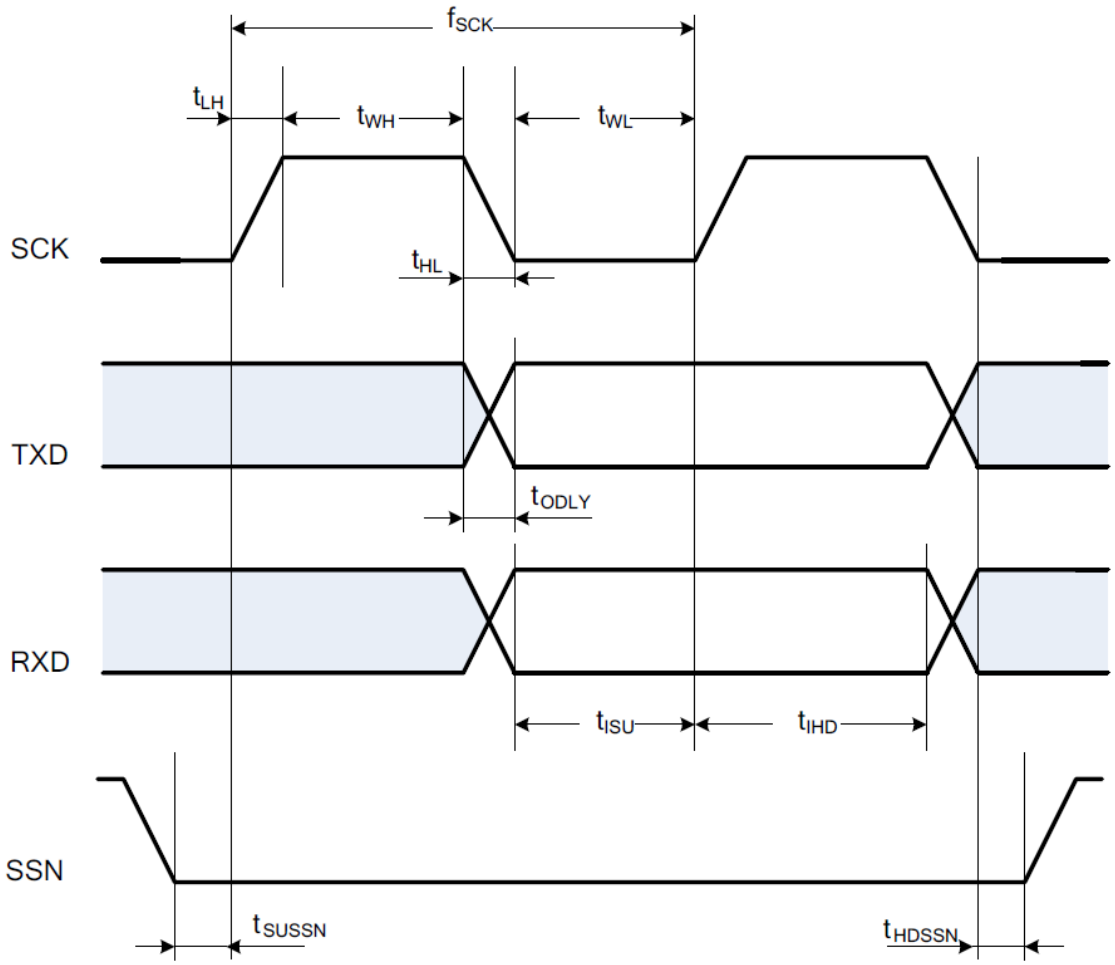
Table 9-8. I^2C Client Timing Parameters

Parameter	Symbol	Min.	Max.	Units	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHz	—
SCL Low Pulse Width	t_{WL}	1.3	—	µs	—
SCL High Pulse Width	t_{WH}	0.6	—		—
SCL, SDA Fall Time	t_{HL}	—	300	ns	—
SCL, SDA Rise Time	t_{LH}	—	300		This is dictated by external components
Start Setup Time	t_{SUSTA}	0.6	—	µs	—
Start Hold Time	t_{HDSTA}	0.6	—		—
SDA Setup Time	t_{SUDAT}	100	—	ns	—
SDA Hold Time	t_{HDDAT}	0	—	ns	Client and Host default
		40	—	µs	Host programming option
Stop Setup Time	t_{SUSTO}	0.6	—	µs	—
Bus Free Time between Stop and Start	t_{BUF}	1.3	—		—
Glitch Pulse Reject	t_{PR}	0	50	ns	—

9.6.2 SPI Client Interface Timing Diagram

The following figure provides the SPI Client timing for the ATWILC3000A.

Figure 9-2. SPI Client Timing Diagram



The following table provides the SPI Client timing parameters for the ATWILC3000A.

Table 9-9. SPI Client Timing Parameters(1)

Parameter	Symbol	Min.	Max.	Unit
Clock Input Frequency(2)	f_{SCK}	—	48	MHz
Clock Low Pulse Width	t_{WL}	6	—	ns
Clock High Pulse Width	t_{WH}	4	—	
Clock Rise Time	t_{LH}	0	7	
Clock Fall Time	t_{HL}	0	7	
TXD Output Delay(3)	t_{ODLY}	3	9 from SCK fall	
RXD Input Setup Time	t_{ISU}	3	—	
RXD Input Hold Time	t_{IHD}	5	—	
SSN Input Setup Time	t_{SUSSN}	5	—	
SSN Input Hold Time	t_{HDSSN}	5	—	

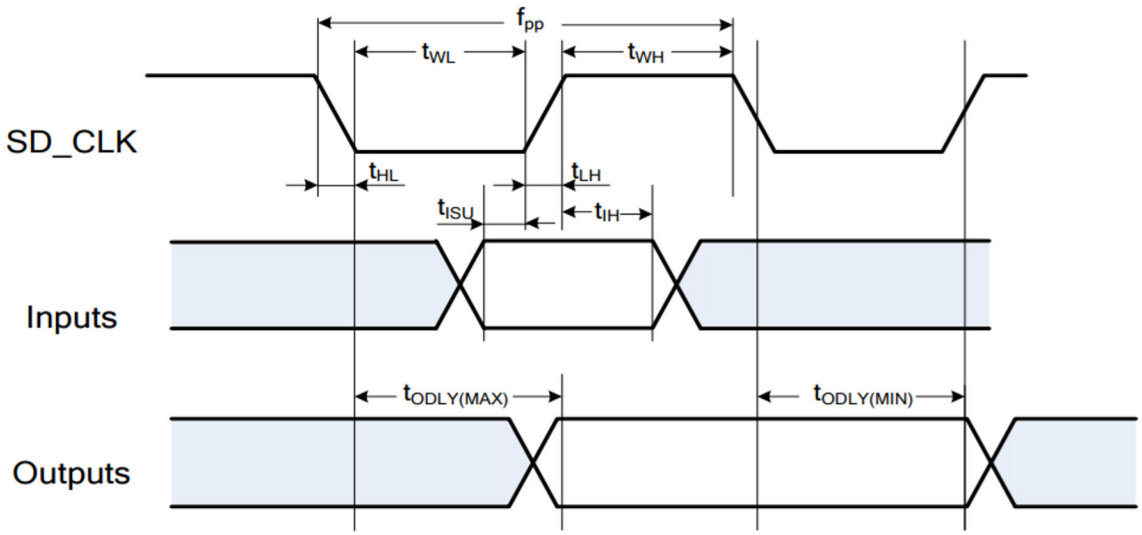
Notes:

1. The timing is applicable to all SPI modes.
2. The maximum clock frequency specified is limited by the SPI Client interface internal design; the actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. The timing is based on 15 pF output loading. Under all conditions, $t_{LH} + t_{WH} + t_{HL} + t_{WL}$ must be less than or equal to $1/ f_{SCK}$.

9.6.3 SDIO Client Interface Timing Diagram

The SDIO Client interface timing for ATWILC3000A is shown in the following figure.

Figure 9-3. SDIO Client Timing Diagram



The following table provides the SDIO Client timing parameters for the ATWILC3000A.

Table 9-10. SDIO Client Timing Parameters

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency(1)	f_{PP}	—	50	MHz
Clock Low Pulse Width	t_{WL}	6	—	ns
Clock High Pulse Width	t_{WH}	7	—	
Clock Rise Time	t_{LH}	0	5	
Clock Fall Time	t_{HL}	0	5	
Input Setup Time	t_{ISU}	6	—	
Input Hold Time	t_{IH}	8	—	
Output Delay(2)	t_{ODLY}	3	11	

Notes:

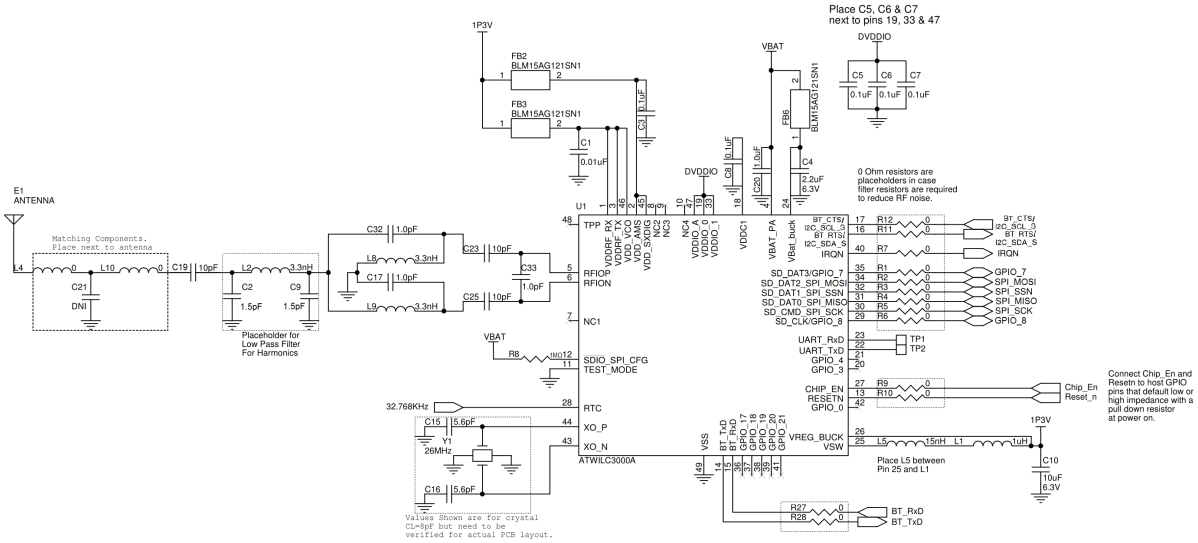
1. Maximum clock frequency specified is limited by the SDIO Client interface internal design; actual maximum clock frequency can be lower and depends on the specific PCB layout.
2. Timing based on 15 pF output loading.

10. Reference Design

The ATWILC3000A application schematics for the different supported Host interfaces are shown in this chapter.

10.1 Host Interface – SPI Reference Schematic

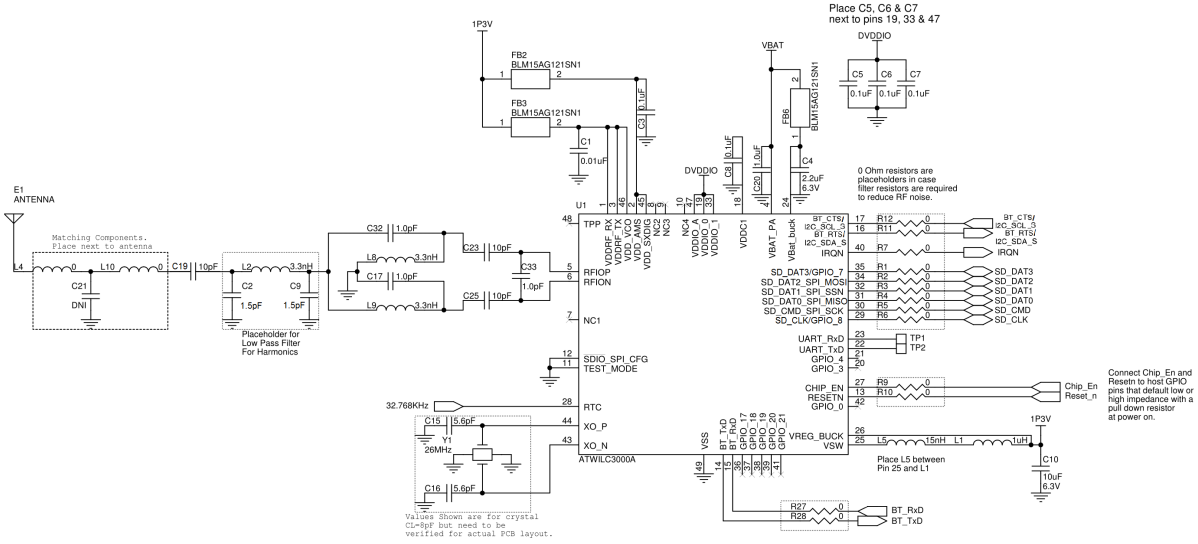
Figure 10-1. ATWILC3000A Reference Schematic for SPI Operation



Note: It is recommended to add test points for pins 14, 15, 16, 17, 22, 23 and 26 in the design.

10.2 Host Interface – SDIO Reference Schematic

Figure 10-2. ATWILC3000A Reference Schematic for SDIO Operation



Note: It is recommended to add test points for pins 14, 15, 16, 17, 22, 23 and 26 in the design.

10.3 Bill of Materials (BoM)

The following table provides the Bill of Materials for the application schematic. The BoM is the same for both the Host interfaces, except for the pull-up resistor R8.

Table 10-1. Bill of Materials

Item	Quantity	Reference	Value	Description	Manufacturer	Part Number
1	15	R1, R2, R3, R4, R5, R6, R7, R9, R10, R11, R12, R27, R28, L4, L10	0Ω	Resistor,Thick Film, 0Ω, 0201	Panasonic®	ERJ-1GN0R00C
2	1	R8	1M	Resistor,Thick Film, 1 MΩ, 0201	Panasonic	ERJ-1GEJ105C
3	1	C1	0.01 µF	Capacitor MC, SMD, 10V, 0.01 µF, K X7R 0201	Yageo Corporation	CC0201KRX7R6BB103
4	5	C3, C5, C6, C7, C8	0.1 µF	Capacitor MC, SMD, 6.3V, 0.1 µF, K X5R 0201	Yageo Corporation	CC0201KRX5R5BB104
5	1	C20	1 µF	Capacitor MC, SMD, 6.3V, 1 µF, K X5R 0402 0.56	Yageo Corporation	CC0402KRX5R5BB105
6	1	C4	2.2 µF	Capacitor MC, SMD, 6.3V, 2.2 µF, M X5R 0402 0.5	Taiyo Yuden	JMK105BJ225MV-F
7	1	C10	10 µF	Capacitor MC, SMD, 6.3V, 10 µF, M X5R 0402 0.5	Murata Electronics®	GRM155R60J106M
8	2	C15, C16	5.6 pF	Capacitor MC, SMD, 25V, 5.6 pF, D C0G 0201 0.3	Walsin Technology Corp.	0201N5R6D250CT
9	3	C19, C23, C25	10 pF	Capacitor MC, SMD, 25V, 10 pF, J C0G 0201 0.3	Murata Electronics	GRM0335C1E100JA01D
10	3	C17, C32, C33	1.0 pF	Capacitor MC, SMD, 25V, 1 pF, B C0G 0201 0.3	Murata Electronics	GRM0335C1E1R0BA01D
11	2	C2, C9	1.5 pF	Capacitor Ceramic, 1.5 pF, 0.25 pF, C0G, 0201, 25V, -55-125°C	Murata Electronics	GRM0335C1H1R5CA01
12	1	L1	1 µH	Inductor, 1 µH, M, 950 mA, 0603	Murata Electronics	LQM18PN1R0MFRL
13	1	L5	15 nH	Inductor, 15 nH, J, 300 mA, 0402	Murata Electronics	LQG15HS15NJ02D

.....continued

Item	Quantity	Reference	Value	Description	Manufacturer	Part Number
14	3	L2, L8, L9	3.3 nH	Inductor, 3.3 nH, 0.2 nH, Q = 14@500 MHz, SRF = 8 GHz, 0201, -55-125°C	Murata Electronics	LQP03TN3N3C02D
15	3	FB2, FB3, FB6	BLM15AG121SN1	Bead, CH, 120Ω, 550 mA, 0402	Murata Electronics	BLM15AG121SN1
16	1	Y1	26 MHz	Crystal, 26 MHz, 50 PPM, 8 pF, SMD-4P, 2.55 * 2.05	Taitien Electronics Co., Ltd.	A0183-X-001-3
17	2	TP1, TP2	Non-component	Test Point, Surface Mount, 0.040” sw w/ 0.25” Hole	—	—
18	1	U1	ATWILC3000A	Single Chip, IEEE 802.11 b/g/n, Link Controller with Integrated Bluetooth®	Microchip Technology Inc.	**ATWILC3000A-MU-T**
19	1	E1	ANTENNA	Antenna, 2.4-2.5 GHz, 50Ω, -40 to +85°C	—	—

11. Design Considerations

11.1 Placement and Routing Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

- The board should have a solid ground plane. The center ground pad of the device must be solidly connected to the ground plane by using a 3 x 3 grid of vias.
- To avoid electromagnetic field blocking, keep any large metal objects as far away from the antenna as possible.
- Do not enclose the antenna within a metal shield.
- Keep any components, which may radiate noise or signals, within the 2.4 GHz to 2.5 GHz frequency band away from the antenna, and shield those components if possible. Any noise radiated from the Host board in this frequency band degrades the sensitivity of the chip.

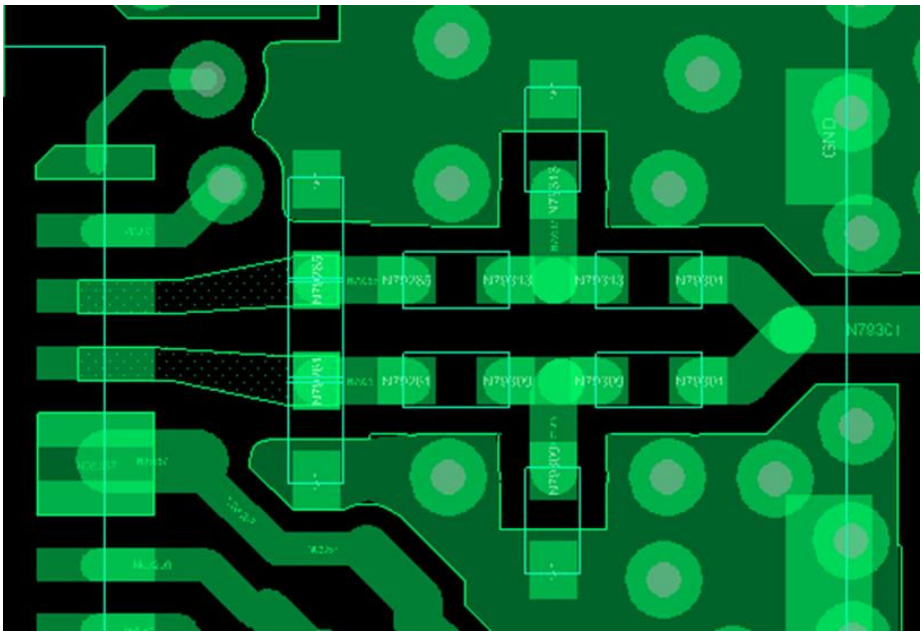
11.1.1 Power and Ground

- Dedicate the layer immediately below the layer containing the RF traces from the ATWILC3000A for ground. Make sure that this ground plane does not get broken up by routes.
- Power traces can be routed on all layers except the ground layer.
- Power supply routes must be heavy copper fill planes to insure low inductance.
- The power pins of the ATWILC3000A must have a via directly to the power plane, close to the power pin.
- Decoupling capacitors must have a via next to the capacitor pin and this via must be directly connected to the power plane. Avoid long trace for this connection.
- The ground pad of the decoupling capacitor must have a via directly to the ground plane.
- Each decoupling capacitor must have its own via directly to the ground plane and directly to the power plane next to the pad.
- The decoupling capacitors must be placed as close as possible to the pin that it is filtering.

11.1.2 RF Traces and Components

- The RF trace from RFIOP (Pin #5) and RFION (Pin #6) of the ATWILC3000A to the balun must be 50Ω differential controlled impedance. The route from the balun to the antenna connector must be a 50Ω controlled impedance trace. This trace must be routed in reference to the ground plane. This ground reference plane must extend entirely under the ATWILC3000A QFN package and to the sides of the these routes.
- Discuss with the PCB vendor to get the available PCB stack-ups and determine the trace dimensions for achieving 50Ω single-ended controlled impedance.
- Do not have any signal traces below/adjacent to the RF trace in the PCB.
- Be sure that the RF traces from ATWILC3000A to the antenna are as short as possible to reduce path losses and to mitigate the trace from picking up noise.
- Place guard ground vias on either side of the RF trace, running from module to the antenna feed point, in the PCB.
- Do not use thermal relief pads for the ground pads of all components in the RF path. These component pads must be completely filled with GND copper polygon. Place individual vias to the GND pads of these components.
- It is recommended to have a 3x3 grid of ground vias solidly connecting the exposed ground paddle of the ATWILC3000A to the ground plane on the inner/other layers of the PCB. This will act as a good ground and thermal conduction path for the ATWILC3000A.
- Make sure that all digital signals that may be toggling while the ATWILC3000A is active are placed as far away from the antenna as possible.
- Be sure to place the matching components and balun as close to the RFIOP and RFION pins as possible (these are C33, C23, C25, C17, C32, L8 and L9 in the reference schematic). The following figure shows the placement and routing of these components.

Figure 11-1. Placement and Routing of Balun and Matching Components

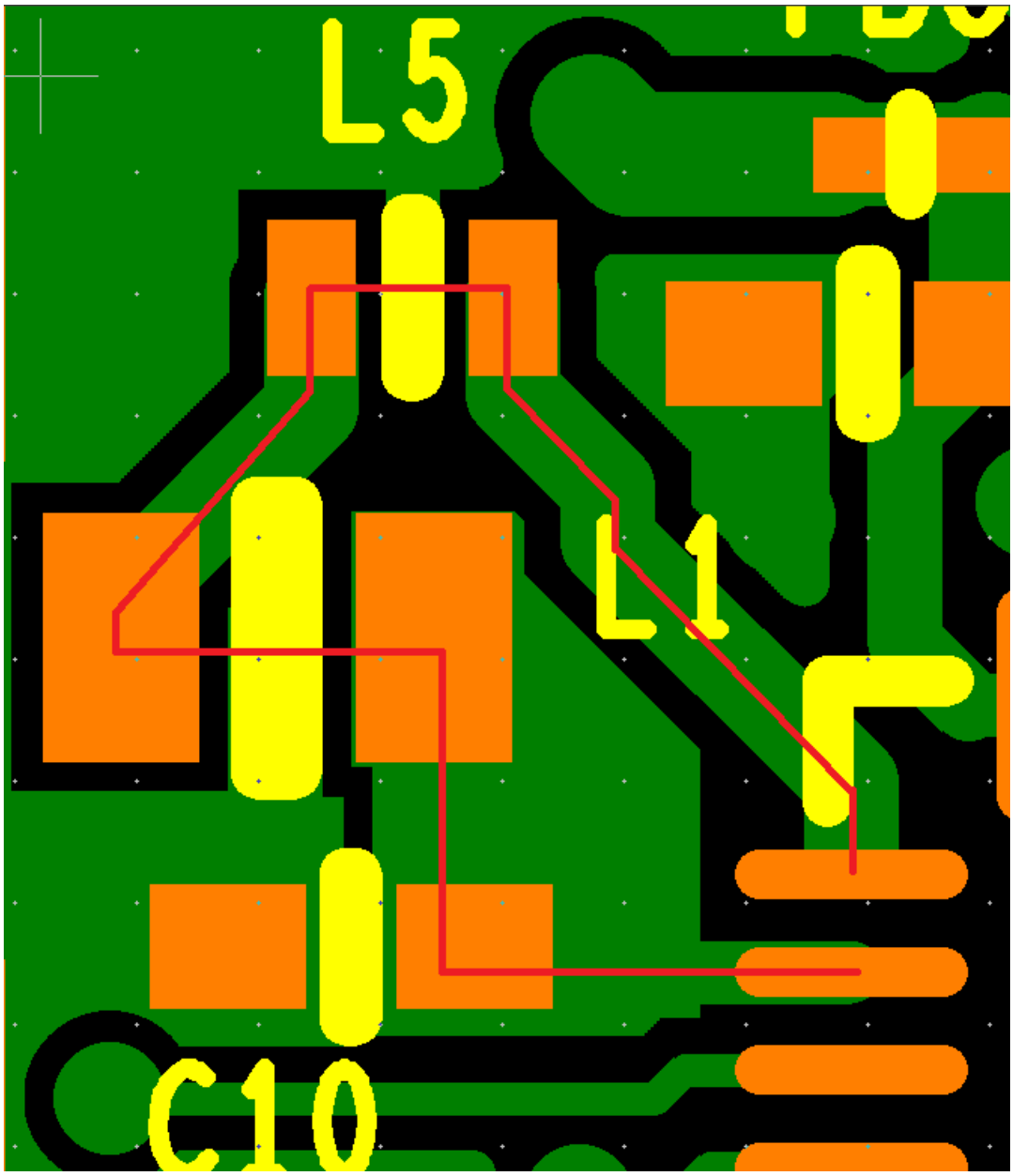


11.1.3 Power Management Unit

The ATWILC3000A contains an on-chip switching regulator, which regulates the VBAT supply for supplying to the rest of the device. It is crucial to place and route the components associated with this circuit correctly to ensure proper operation and especially to reduce any radiated noise, which can be picked up by the antenna and can severely reduce the receiver sensitivity. The external components for the PMU consist of two inductors, L5 = 15 nH and L1 = 1 µH and a capacitor, C10 = 10 µF. These components must be placed as close as possible to ATWILC3000A pin #25. The smaller inductor, L5, must be placed closest to pin #25. Current will flow from pin #25, through L5, then L1, and then through C10 to ground and back to the center ground paddle of the ATWILC3000A package.

Place components to have a current loop that is as small as possible. Make sure that there is a ground via to the inner ground plane right next to the ground pin of C10. The ground return path must be extremely low inductance. Failure to provide a short, heavy ground return between the capacitor and the ATWILC3000A ground pad will result in incorrect operation of the on-chip switching regulator. The following figure shows an example placement and routing of these components. In the following figure, the trace which creates the loop is highlighted in red.

Figure 11-2. Placement and Routing of PMU Components



11.1.4 Ground

The center ground pad of the device must be solidly connected to the ground plane by using a 3 x 3 grid of vias. These ground vias must surround the perimeter of the pad. One of these ground vias must be in the center pad as close as possible to pins #5 (RFIOP) and #6 (RFION). This Ground via serves as the RF ground return path. Also, there must be a ground via in the center pad as close as possible to pin #25 (VSW). This is the ground return for the PMU.

11.1.5 Sensitive Traces

11.1.5.1 Signals

The following signals are very sensitive to noise and the user must take care to keep them as short as possible, and keep them isolated from all other signals by routing them far away from other traces or using ground to shield them. Be sure that they are also isolated from noisy traces on the layers above them and below them:

- XO_N
- XO_P
- RFIOP
- RFION

11.1.5.2 Supplies

The following power supply pins for the ATWILC3000A are sensitive to noise and care should be taken to isolate the routes to these pins from other noisy signals, both on the same layer as the route, and on layers above and below. Use ground between these sensitive signals to isolate them from other signals. It is important that the decoupling capacitors for these supplies are placed as close to the ATWILC3000A pin as possible. This is necessary to reduce the trace inductance between the capacitor and the ATWILC3000A power pin to an absolute minimum:

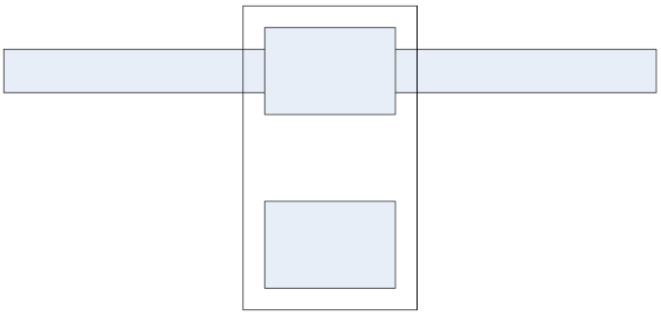
- VDDRF_RX (pin #1)
- VDDRF_TX (pin #3)
- VDD_AMS (pin #2)
- VDD_SXDIG (pin #45)
- VDD_VCO (pin #46)

Additionally, while the VDDC (pin #18) and VBAT_BUCK (pin #24) supplies are not sensitive to picking up noise, they are noise generating supplies. Therefore, be sure to keep the decoupling capacitors for these supply pins as close as possible to the VDDC and VBAT_BUCK pins, and make sure that the routes for these supplies stay far away from sensitive pins and supplies.

11.1.6 Additional Suggestions

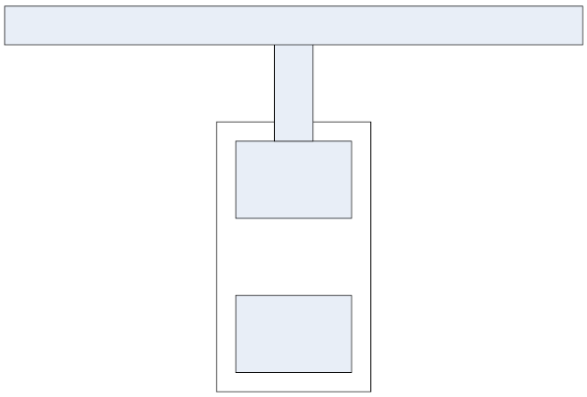
Make sure that traces route directly through the pads of all filter capacitors and not by a stub route. The following figure shows the correct way to route through a capacitor pad.

Figure 11-3. Correct Routing Through Capacitor Pad



The following figure shows a stub route to the capacitor pad. This should be avoided as it adds additional impedance in series with the capacitor.

Figure 11-4. Incorrect Stub Route to Capacitor Pad



11.1.7 Interferers

One of the biggest problems with RF receivers is poor performance due to interferers on the board radiating noise into the antenna or coupling into the RF traces going to input LNA. Care must be taken to make sure that there is no noisy circuitry placed anywhere near the antenna or the RF traces. All noise generating circuits should also be shielded so they do not radiate noise that is picked up by the antenna. Also, make sure that no traces route underneath the RF portion of the ATWILC3000A. Also, make sure that no traces route underneath any of the RF traces from the antenna to the ATWILC3000A input; this applies to all layers. Even if there is a ground plane on a layer between the RF route and another signal, the ground return current will flow on the ground plane and couple into the RF traces.

11.1.8 Antenna

Be sure to choose an antenna that covers the frequency band, 2.400 GHz to 2.500 GHz, and is designed for a 50Ω feed point. Follow the antenna vendor's recommendations for pad dimensions, the spacing from the pad to the ground reference plane and the spacing from the edges of the pad to the ground fill on the same layer as the pad. Finally, make sure that the antenna matching components are placed as close as to the antenna pad as possible.

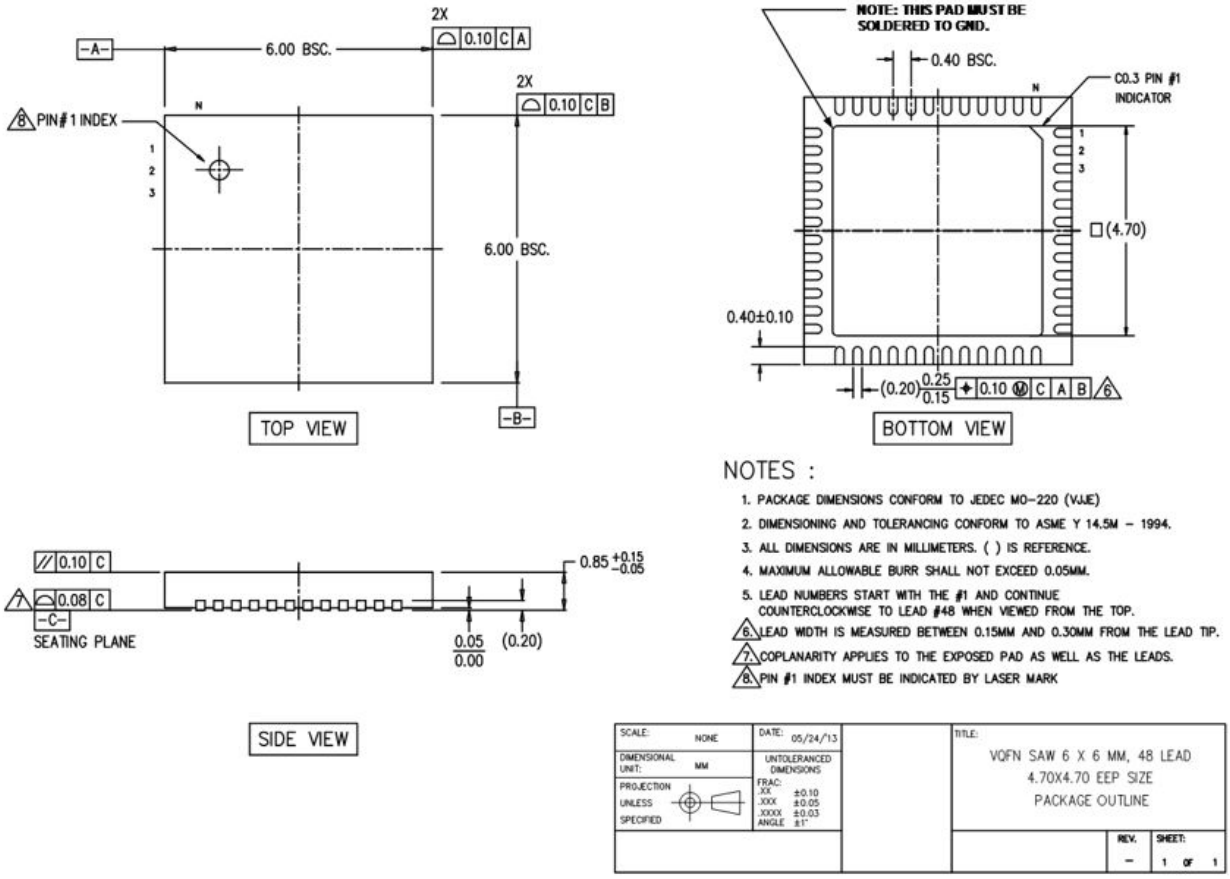
11.2 Reflow Profile Information

For information on reflow process guidelines, refer to the *"*Solder Reflow Recommendation *Application Note"* (DS00233).

12. Package Outline Drawing

The ATWILC3000A 48-pin QFN package is shown in the following figure.

Figure 12-1. ATWILC3000A QFN Package Outline Drawings – Top, Bottom and Side View



13. Reference Documentation

The following table provides the set of collateral documents to ease integration and device ramp.

Table 13-1. Reference Documents

Document Title	Content
"ATWILC1000/ATWILC3000 – Wi-Fi® Link Controller Linux® User's Guide"	This user's guide describes how to run Wi-Fi on the ATWILC1000 SD card and to run Wi-Fi/BLE on the ATWILC3000 Shield board on the SAMA5D4 Xplained Ultra running with the Linux kernel 4.9.
"ATWILC1000/ATWILC3000 – ATWILC Devices Linux® Porting Guide"	This user's guide describes how to port the ATWILC1000 and ATWILC3000 Linux drivers to another platform, and contains all the required modifications for driver porting.
"ATWILC1000/ATWILC3000 – Baremetal Wi-Fi®/BLE Link Controller Software Design Guide"	This design guide helps the user in integrating ATWILC1000/ ATWILC3000 in the application using RTOS from Advanced Software Framework (ASF).
"ATWINC/ATWILC/ATSAMB/ ATBTLC – MCHPRT2 User's Guide"	This document provides detailed information about the MCHPRT2 tool, which allows the user to configure, evaluate and test an RF system, based on the ATWILC3000 amongst other devices.
"ATWILC3000A/ATWILC3000-MR110xA Errata"	This document details the anomalies identified in the ATWILC3000 family of devices.
"ATWILC3000A Reference Design Package" (available in the ATWILC3000A Reference Design Package on ATWILC3000-IC webpage under Supporting Collateral)	This reference design package contains the design collateral (Schematics, Bill of Materials, PCB design source files, Gerber) of the module, evaluation boards and its associated boards for the ATWILC3000A, which should help a user to get started with their design.
"ATWILC3000A – Deriving Application Gain Table Application Note" (available as a part of the ATWILC3000A Reference Design Package on ATWILC3000-IC webpage)	This application note describes the Wi-Fi and BLE gain table structure and procedure to derive the application gain table. This document provides further details on the steps to update the device with the gain table.

Note: For a complete listing of development support tools and documentation, visit www.microchip.com/wwwproducts/en/ATWILC3000 or refer to the customer support section on options to the nearest Microchip field representative.

14. Document Revision History

Revision	Date	Section	Description
B	05/2021	Document	Replaced the Master/Slave terminologies. For more details, see the following note.
		Introduction	Updated peripheral details
		Features	Added operating conditions
		1. Ordering Information and IC Marking	Updated with additional ordering code and description in the Table 1-1
		4. CPU and Memory Subsystem	Errors in description fixed and added additional information in 4.3 Nonvolatile Memory (eFuse)
		13. Reference Documentation	Added Deriving a Gain Table App Note to the Table 13-1
A	06/2020	Document	• Updated from Atmel to Microchip template. • Assigned a new Microchip document number. Previous version is Atmel 42390 revision D. • ISBN number added.
		2. Functional Overview	• Rearranged sections under this chapter • Updated Figure 2-1 • Updated descriptions of the pins in 2.2.1 Pinout Details • Updated pad width in Table 2-2
		4.3 Nonvolatile Memory (eFuse)	Updated with new information and Figure 4-1
		5. WLAN Subsystem	• Added a note for firmware support of Short GI • Updated Table 5-1
		7. External Interfaces	• Updated lead sentence • Minor edits • Added 7.1 Interfacing with Host Microcontroller
		9. Electrical Characteristics	Updated Table 9-9
		10. Reference Design	• Updated Figure 10-1 and Figure 10-2 • Added Table 10-1 and updated contents
		11. Design Considerations	Added a new chapter
		13. Reference Documentation	Updated Table 13-1

Note: *Microchip is aware that some terminologies used in the technical documents and existing software codes of this product are outdated and unsuitable. This document may use these new terminologies, which may or may not reflect on the source codes, software GUIs, and the documents referenced within this document. The following table shows the relevant terminology changes made in this document.*

Table 14-1. Terminology Related Changes

Old Terminology	New Terminology	Description
Master	Host	The following sections are updated with new terminology: • 2.2.1 Pinout Details • 7. External Interfaces • 7.1 Interfacing with Host Microcontroller • 7.2 I2C Client Interface • 7.3 SPI Client Interface • 7.4 SDIO Client Interface • 9.6.1 I2C Client Interface Timing Diagram • 9.6.2 SPI Client Interface Timing Diagram • 9.6.3 SDIO Client Interface Timing Diagram
Slave	Client	

14.1 Atmel Revision History

Rev D – 05/2016

Section	Changes
Document	• Updated Features, Bluetooth® to say Bluetooth 4.0 (Basic Rate, Enhanced Rate and BLE). Added Bluetooth Certifications. • Replaced VBATT with VBAT to match schematics. • Revised Package information in Table 3-2. • Revised PPM values from 200 to 500 ppm in Chapter 5. • Revised Table 7-2 transmitter performance values and Note 2. • Revised the values and note in Table 8-2. • Revised SPI Slave Timing parameters in Table 9-6. • Revised SPI Master Timing parameters in Table 9-8. • Revised SDIO Slave Timing parameters in Table 9-10. • Added text in Section 9.6 regarding flow control usage. • Revised Current consumption values in Table 10-2. • Updated Package drawing to include solder paddle pad in Figure 3-2. • Added Reflow profile in Chapter 13. • Revised tolerance for thickness in Table 3-2 for QFN package information. • Added footnote for Pull-up/Pull-Down Ohm value in Table 10-4.

Rev C - 07/2015

Section	Changes
Document	• Modified sections 10.2.1 and 10.2.2 to add new current consumption numbers, update state names and correct some typos. • Fixed typos for SPI Slave interface timing in Table 9-6. • Fixed typos for battery supply name: changed from VBAT to VBATT. • Corrected PMU output voltages in Table 10-1. • Updated reference schematic drawing in Section 11. • Added comment regarding resistors on SDIO pins in Section 12. • Updated power architecture drawing in Section 10.1. • Added pad drive strength in Table 4-3 and removed the note under Table 3-1. • Updated operating temperature in the feature list. • Corrected current in Power_Down state in Table 10-2. • Miscellaneous minor formatting and content corrections.

Rev B - 03/2015

Section	Changes
Document	DS update new Atmel format.

Rev A - 01/2015

Section	Changes
Document	Initial Release

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ISBN: 978-1-5224-8257-4

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